# SIEMENS

# ICs for Communications

Digital Answering Machine with Full Duplex Speakerphone SAM EC PSB 4860 Version 2.1

Delta Sheet 07.97

T4860-XV21-L1-7600

Previous Version:

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### Digital Answering Machine with Full Duplex Speakerphone SAM EC

**PSB 4860** 

#### **Delta Sheet for Target Specification 03.97**

This Delta Sheet describes modifications of the PSB 4860 Version 2.1 as described by the Target Specification 03.97. The next Target Specification for the PSB 4860 Version 2.1 will incorporate the modifications described in this document.

#### 1 Supported Memory Devices

The following memory devices are no longer supported:

- KM29N32000 (32 MBit flash)
- Intel type.

Therfore table 69 (page 88) must read as follows:

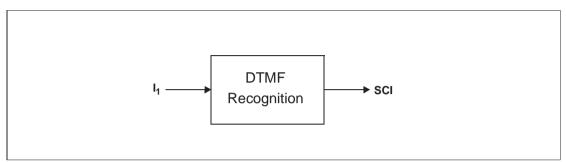
#### Table 69

Mbit	Туре	Bank 0 (D <sub>0</sub> -D <sub>3</sub> )	Bank 1 (D <sub>4</sub> -D <sub>7</sub> )	Comment
1	ARAM/DRAM	256kx4		
2	ARAM/DRAM	256kx4	256kx4	
4	ARAM/DRAM	1Mx4	-	
4	ARAM/DRAM	512	2kx8	
8	ARAM/DRAM	1Mx4	1Mx4	
16	ARAM/DRAM	4Mx4	-	2k or 4k refresh
16	ARAM/DRAM	2Mx8		2k refresh
32	ARAM/DRAM	4Mx4	4Mx4	2k or 4k refresh
32	ARAM/DRAM	2x2	Mx8	2k refresh
64	ARAM/DRAM	16Mx4	-	4k or 8k refresh
64	ARAM/DRAM	A8	lx8	4k or 8k refresh
128	ARAM/DRAM	16Mx4	16Mx4	4k or 8k refresh
4-128	FLASH	512kx8 devices		KM29N040
8-128	FLASH	1Mx8	KM29W8000	
16-128	FLASH	2Mx8	KM29N16000	

Please refer to section 6 for an updated description of register CCTL.

#### 2 DTMF Detector

The dial tone filter has been removed. Therefore the block diagram of the DTMF detector (figure 22, page 40) is replaced by the following figure:



### Figure 22 DTMF Detector - Block Diagram

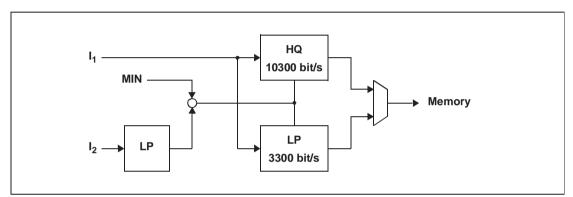
As the dial tone filter has been removed the bit ENF (Dial tone filter enable) in register DDCTL no longer exists.

Note: The performance of the DTMF receiver is not affected by the deletion of the dial tone filter.

### 3 Audio Data over SCI

According to the Target Specification 03.97 the microcontroller can send compressed audio data to the decoder over the serial control interface (SCI). Furthermore the coder can send compressed audio data to the microcontroller over the serial control interface. This option is no longer present. Therefore both the coder and the decoder have only an interface to the memory connected to the PSB 4860.

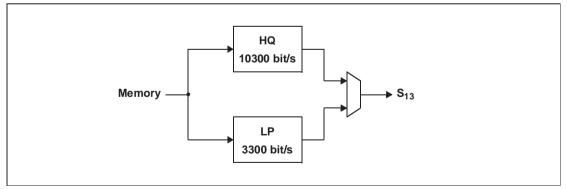
The block diagram of the coder (figure 29, page 49) must be replaced by the following figure:



#### Figure 29 Speech Coder - Block Diagram

The register SCDATA and the bit DST in register SCCTL do not exist any more.

The block diagram of the decoder (figure 30, page 51) must be replaced by the following figure:



#### Figure 30 Speech Decoder - Block Diagram

The register SDDATA and the bit SRC in register SDCTL do not exist any more.

#### 4 Direct Memory Access

In addition to the file commands already described in the Target Specification 03.97 four new commands have been defined for direct memory access. These commands are:

- 1. Set Address
- 2. DMA Read
- 3. DMA Write
- 4. Erase Block (flash memory only)

These commands can be used only when no file is open. With these commands the microcontroller can access any location of the memory connected to the PSB 4860 Version 2.1. As an example the microcontroller can upload a phrase file (for voice prompt generation) into a flash memory from some ROM connected to the microcontroller.

#### 4.1 Set Address

This command sets the 24 bit address pointer APTR. Only the address bits  $A_8$ - $A_{23}$  are set, the address bits  $A_0$ - $A_7$  are automatically cleared. Table 1 shows the parameters for this command.

### Table 1

#### **Set Address Parameters**

Register	# of Bits	Name	Comment
FCMD	5	CMD	Set Address command code
FDATA	16	ADR	Address bits A <sub>8</sub> -A <sub>23</sub> of adress pointer APTR

Possible error conditions:

• file open

#### 4.2 DMA Read

This command reads a single word adressed by APTR. After the read access APTR is automatically incremented by one. Table 2 shows the parameters for this command.

#### Table 2 DMA Read Parameters

Register	# of Bits	Name	Comment			
FCMD	5	CMD	DMA Read command code			

#### Table 3 DMA Read Results

Register	# of Bits	Name	Comment
FDATA	16	DATA	Data read from address APTR.

Possible error conditions:

• file open

### 4.3 DMA Write

This command writes a single word to the location addressed by APTR. After the write access APTR is automatically incremented by one. Table 4 shows the parameters for this command.

#### Table 4 DMA Write Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	DMA Write command code
FDATA	16	DATA	Data to be written to APTR

Possible error conditions:

• file open

### 4.4 Block Erase

This command erases the physical block which includes the address given by APTR. The actual amount of memory erased by this command depends on the block size of the flash device. Table 5 shows the parameters for this command.

# Table 5Block Erase Parameters

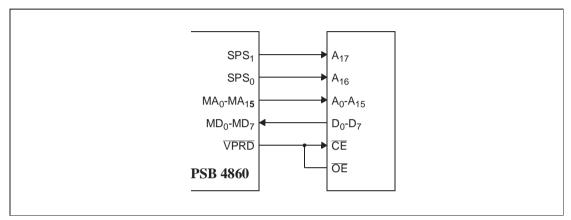
Register	# of Bits	Name	Comment
FCMD	5	CMD	Block Erase command code

Possible error conditions:

• file open

#### 5 Voice Prompt EPROM

According to the Target Specification 03.97 the maximum size of the voice prompt EPROM is 512kBit (64kx8). The PSB 4860 Version 2.1 can now support up to 2MBit (256kx8). The necessary address lines  $A_{16}$  and  $A_{17}$  are provided by the pins SPS<sub>0</sub> and SPS<sub>1</sub>. The EPROM interface (figure 61, page 93) should be replaced by the following figure:



#### Figure 61 EPROM Interface - Connection Diagram

In order to enable this feature an additional mode has been defined for the SPS pins. Please refer to section 7 for programming details.

### 6 Register CCTL (Chip Control)

The corrected description of this register is given below. Bit RFM has changed position, bit CS9 is flipped, bit MQ is now described and the Intel type flash has been removed.

15														0
0	0	0	0	MV	0	0	PD	0	0	RFM	MQ	MT	CS9	SAS
ΜV	0:	Voice Prompt EPROM 0: not available 1: available												
PD	0:	Power Down0: PSB 4860 is in active mode1: enter power-down mode												
RFM	0:	Refresh Mode 0: normal 1: battery backup												
MQ	0:	Memory Quality 0: ARAM 1: DRAM												
МТ	M	Memory Type												
	_	3	2	Descrip	tion									
		0	0	ARAM/D	RAM									
	_	1 1 Samsung flash memory												
CS9	0:	CAS selection 0: other memory 1: 256kx4 or 512kx8 memory												

#### SAS Split Address Space

- 0: other ARAM/DRAM
- 1: two 2Mx8 devices

#### 7 Register SPSCTL

The correct description of this register is given below. A new mode for expanded voice EPROM addressing has been added.

15										0	
POS	0	0	0	0	0	0	0	MODE	SP1	SP0	

#### POS Position of Status Register Window

15	14	13	12	SPS0	SPS <sub>1</sub>
0	0	0	0	Bit 0	Bit 1
0	0	0	1	Bit 1	Bit 2
1	1	1	0	Bit 14	Bit 15

#### MODE Mode of SPS Interface

4	3	2	Description
0	0	0	Disabled (SPS <sub>0</sub> and SPS <sub>1</sub> zero)
0	0	1	Output of SP1 and SP0
1	0	1	Expanded address output
1	1	0	Output of STATUS register

#### SP1 Direct Control for SPS<sub>1</sub>

- 0: SPS<sub>1</sub> set to 0
- 1: SPS<sub>1</sub> set to 1

#### SP0 Direct Control for SPS<sub>0</sub>

- 0: SPS<sub>0</sub> set to 0
- 1: SPS<sub>0</sub> set to 1