SIEMENS

ICs for Communications

Analog Front End for Telephone Systems

SAM AFE

PSB 4851 Version 1.1

Data Sheet 11.97

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Previous Version:		Preliminary Data Sheet 06.97 (V1.1)
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)

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1 Overview

The PSB 4851 integrates all amplifiers to directly connect the transducers to the chip. It features two completely independent channels. An integrated analog multiplexer allows the connection of three signal sources (handset microphone, speakerphone microphone, analog line) to the two channels.

Furthermore the PSB 4851 supports a sophisticated power management and a loop mode in the analog domain. These features can be used to implement a line powered mode for emergency operation of the phone.

The chip is programmed by a simple four wire serial control interface.

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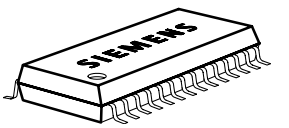
Analog Front End for Telephone Systems **PSB 4851**
SAM AFE

Version 1.1 **BICMOS**

1.1 Features



P-DSO-28-1

- direct connection to handset
- direct connection to microphone
- direct connection to loudspeaker (50 Ω)
- low power emergency operation
- serial control interface for programming
- 2.4 V reference voltage
- two differential inputs
- support for controlled loudhearing
- compliant to G.712

Type	Package
PSB 4851	P-DSO-28-1

1.2 Pin Configuration

(top view)

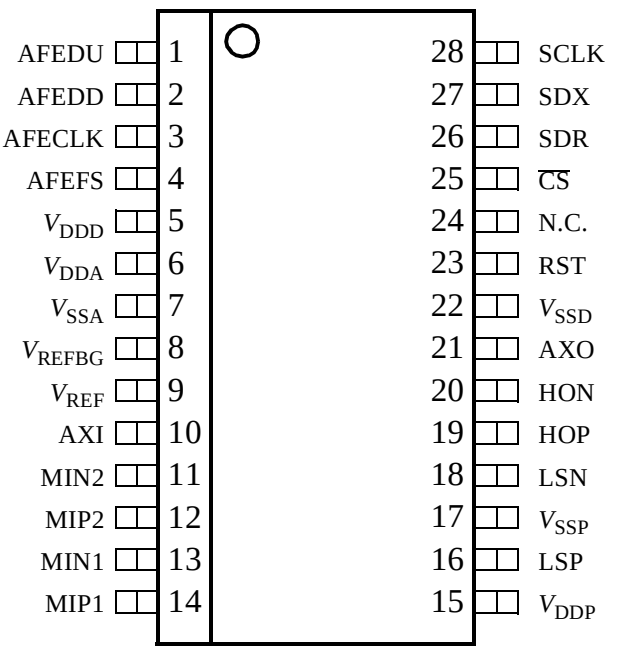


Figure 1
Pin Configuration

1.3 Pin Definitions and Functions

Pin Definitions and Functions

Pin No. P-DSO-28-1	Symbol	Dir.	Reset	Function
5	V_{DDD}	-	-	**Power supply (5V ±5 %)** Power supply for digital parts.
6	V_{DDA}	-	-	**Power supply (5V ±5 %)** Power supply for analog parts.
15	V_{DDP}	-	-	**Power supply (5V ±5 %)** Power supply for loudspeaker amplifier.
22	V_{SSD}	-	-	**Power supply (0 V)** Ground for digital parts.
7	V_{SSA}	-	-	**Power supply (0 V)** Ground for analog parts.
17	V_{SSP}	-	-	**Power supply (0 V)** Ground for loudspeaker amplifier.
1	AFEDU	O	L	**Data Upstream:** Data output to PSB 4860.
2	AFEDD	I	-	**Data Downstream:** Data input from PSB 4860.
3	AFECLK	I	-	**Data Clock:** 6.912 MHz clock.
4	AFEFS	I	-	**Frame Synchronization:** 8kHz frame synchronization from PSB 4860.
28	SCLK	I	-	**Serial Clock:** Clock for serial control interface (SCI).
27	SDX	OD	H	**Serial Data Transmit:** Data output for serial control interface (SCI).
26	SDR	I	-	**Serial Data Receive:** Data input for serial control interface (SCI).
25	$\overline{CS}$	I	-	**Chip Select:** Select signal for serial control interface (SCI).
23	RST	I	-	**Reset:** Active high reset signal.
10	AXI	I	-	**Auxiliary Input:** Single ended analog input (e.g. line in).

Pin Definitions and Functions

Pin No. P-DSO-28-1	Symbol	Dir.	Reset	Function
13 14	MIN1 MIP1	I I	-	**Microphone Input 1:** This input provides a highly symmetrical differential input for commonly used telephone microphones.
11 12	MIN2 MIP2	I I	-	**Microphone Input 2:** This input provides a highly symmetrical differential input for commonly used telephone microphones.
21	AXO	O	0 V	**Auxiliary Output:** Single ended analog output (e.g line out).
19 20	HOP HON	O O	0 V 0 V	**Handset Earpiece Output:** Differential outputs which can drive common handset earpiece transducers directly.
16 18	LSP LSN	O	0 V 0 V	**Loudspeaker Output:** Differential outputs which can drive a 50Ω loudspeaker directly. A piezo transducer can also be used for ringing signal instead of the loudspeaker.
8	V_{REFBG}	O	0 V	**Reference Bandgap Voltage**
9	V_{REF}	O	0 V	**Reference Voltage (2.4 V):** Output for biasing external circuitry, e.g. electret microphone.

1.4 Logic Symbol

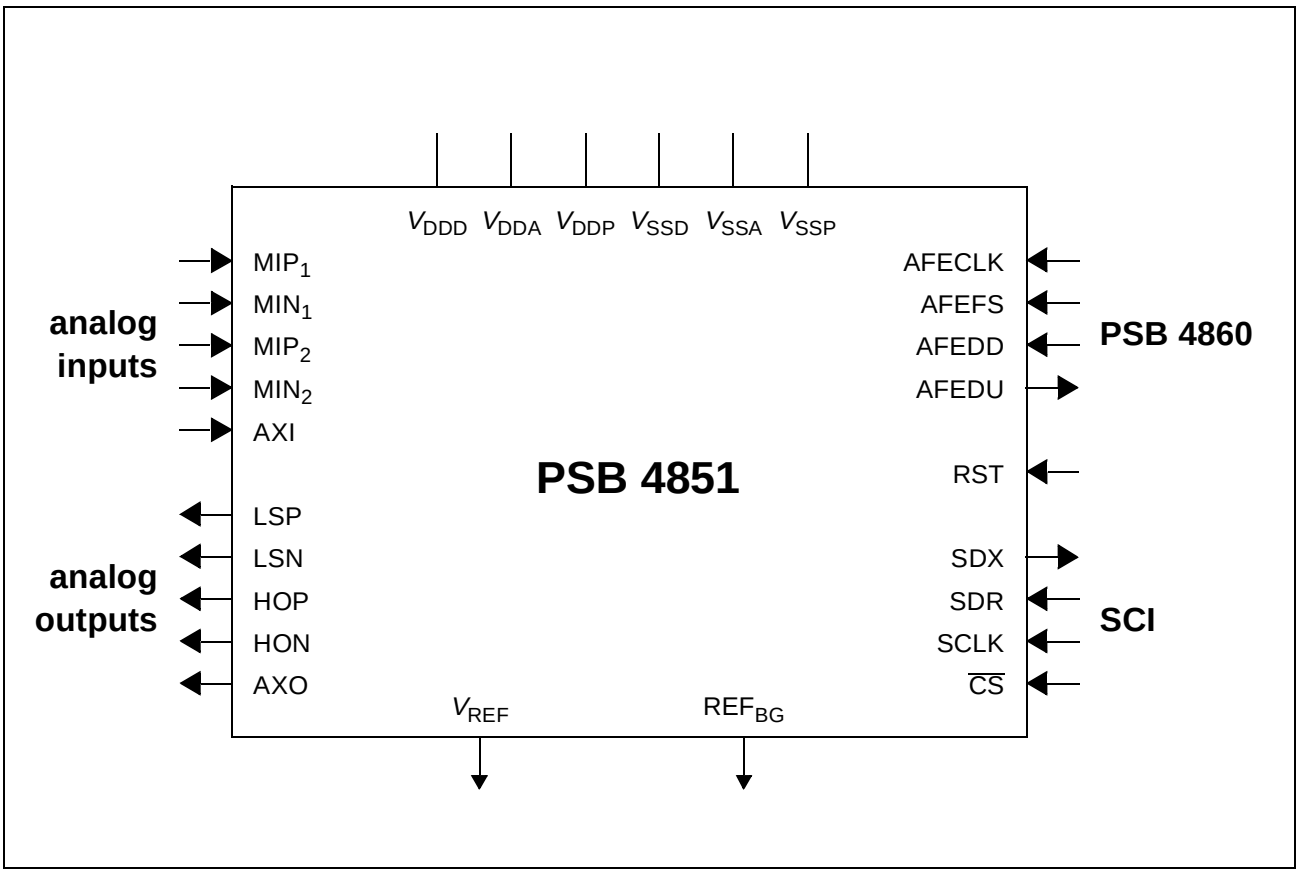


Figure 2
Logic Symbol of PSB 4851

1.5 Functional Block Diagram

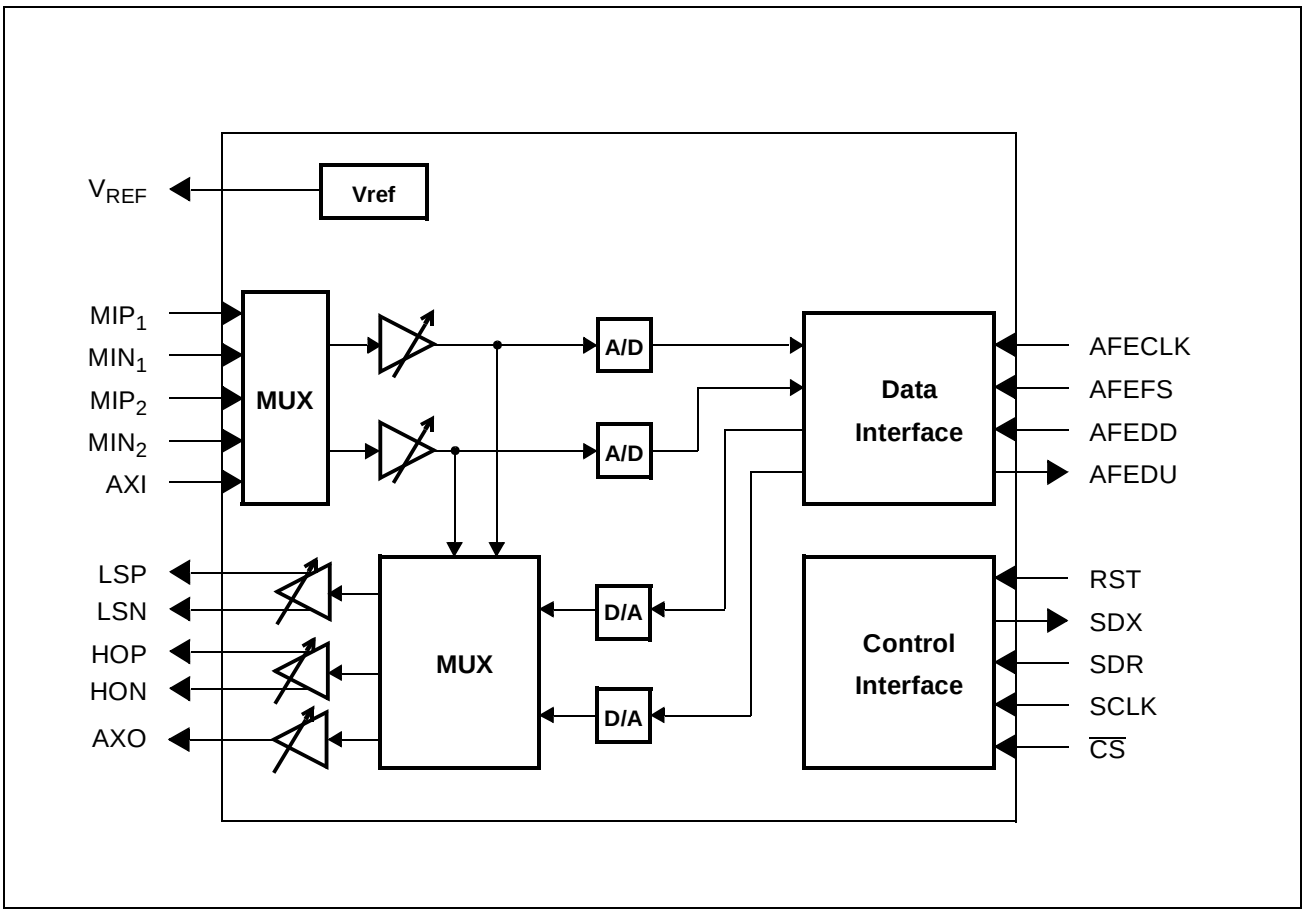


Figure 3
Block Diagram of PSB 4851

1.6 System Integration

The PSB 4851 is the standard analog interface for several digital telecommunication ICs such as:

- PSB 4860 (digital answering machine)
- PSB 2170 (acoustic echo canceller)

The PSB 4851 is especially suited for applications that need two independent analog channels where one codec interfaces to a loudspeaker/microphone combination while the other codec serves the line.

1.6.1 Analog Featurephone with Digital Answering Machine

Figure 4 shows an example of an analog telephone system. The telephone can operate during power failure by line powering. In this case only the handset is active. All other parts of the chipset are shut down leaving enough power for the external microcontroller to perform basic tasks like keyboard monitoring.

For answering machine operation the voice data is stored in ARAM or Flash Memory devices and voice prompts can be played back from an optional voice prompt EPROM. If Flash Memory is used the functionality of the voice EPROM can be realized by the Flash Memory devices.

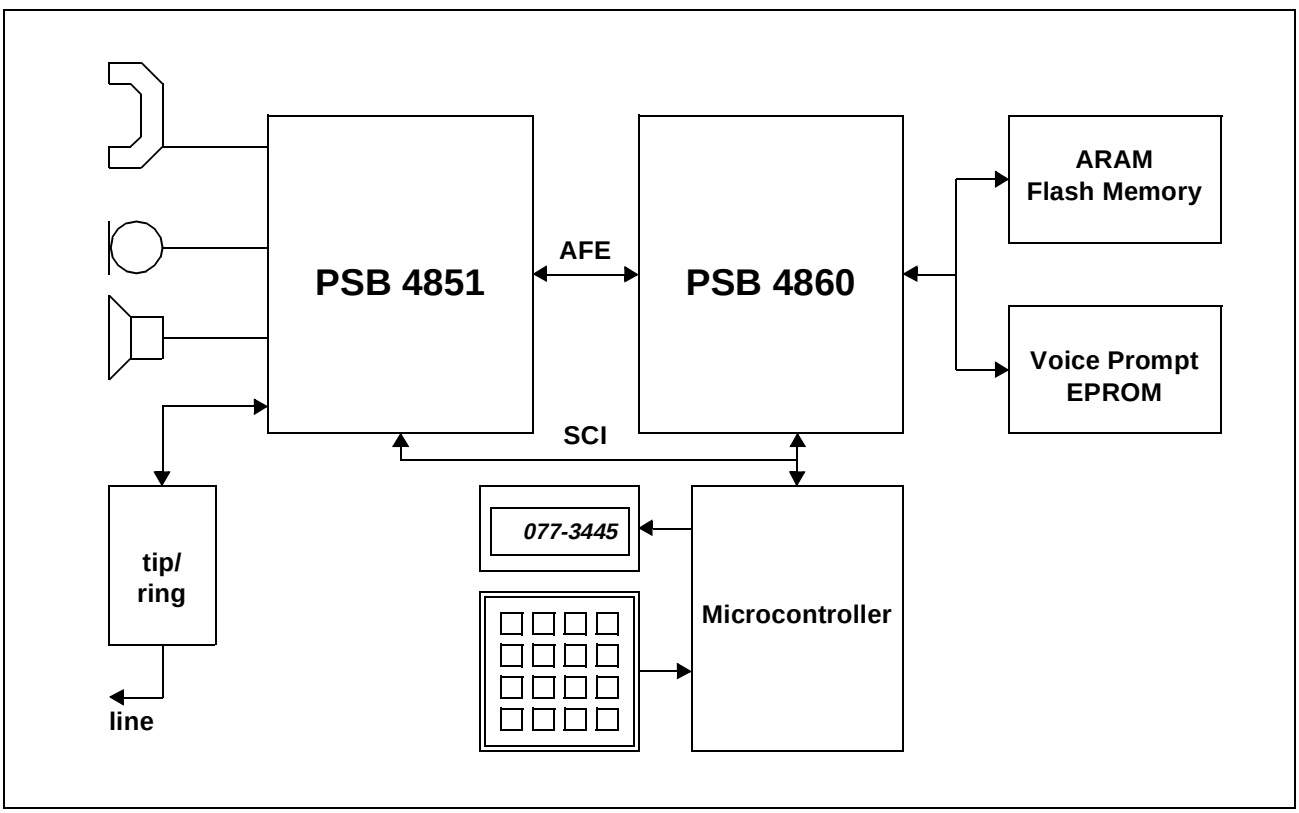


Figure 4
Analog Full Duplex Speakerphone with Digital Answering Machine

1.6.2 DECT Basestation with Full Duplex Featurephone

Figure 5 shows a DECT basestation with acoustic echo cancellation based on the PSB 2170. The full duplex featurephone can be switched to the basestation or a mobile handset dynamically. For programming the serial control interface (SCI) is used while voice data is transferred via the strobed serial data interface (SSDI).

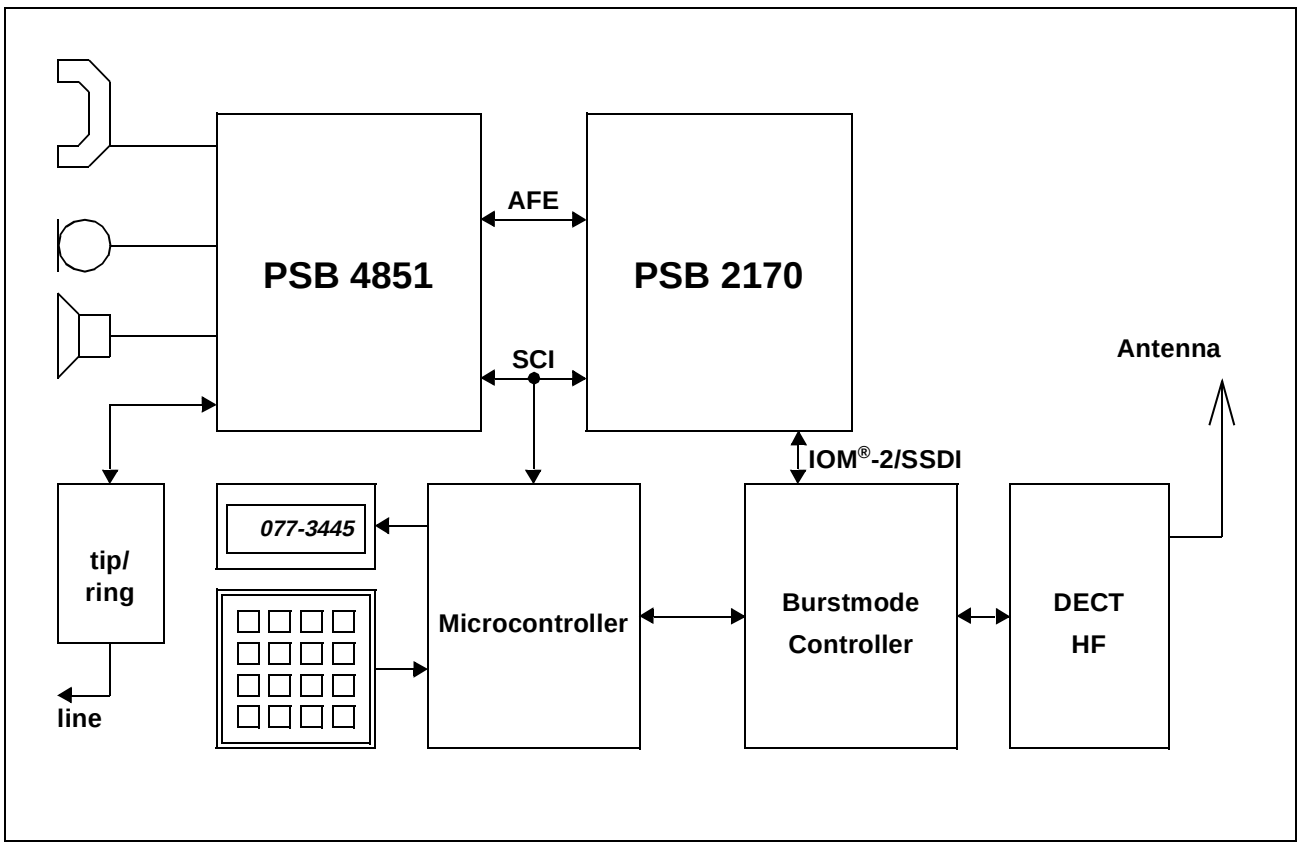


Figure 5
DECT Basestation with Full Duplex Speakerphone

2 Functional Description

The PSB 4851 provides two bidirectional channels from the analog domain to the digital domain, an internal loopback and a sophisticated power management for line-powered operation. The first section describes the signal paths and functional units of the PSB 4851 while the second section discusses the support line powered operation.

2.1 Signal Paths and Functional Units

The PSB 4851 supports three analog inputs, three analog outputs and two digital channels as shown in table 1.

Table 1

Analog Inputs	**Pins**	**Comment**
	AXI	line input from tip/ring interface
	MIP1, MIN1	mic. 1, e.g. speakerphone microphone
	MIP2, MIN2	mic. 2, e.g. handset microphone
Analog Outputs	AXO	line output to tip/ring interface
	HOP, HON	handset earpiece
	LSP, LSN	speakerphone loudspeaker
Digital Channels	AFEDD, AFEDU, AFEFS, AFECLK	Channel 1and 2 of AFE interface (to/ from PSB 2170, PSB 4860)

These signals can be routed in either ***pass-through*** or ***loopback*** mode (Fig. 6). In loopback mode different loops are available for test purposes and line powered operation. In loopback mode the digital part of the PSB 4851 can be completely shut down if it is not needed. The loop on the analog side remains fully functional.

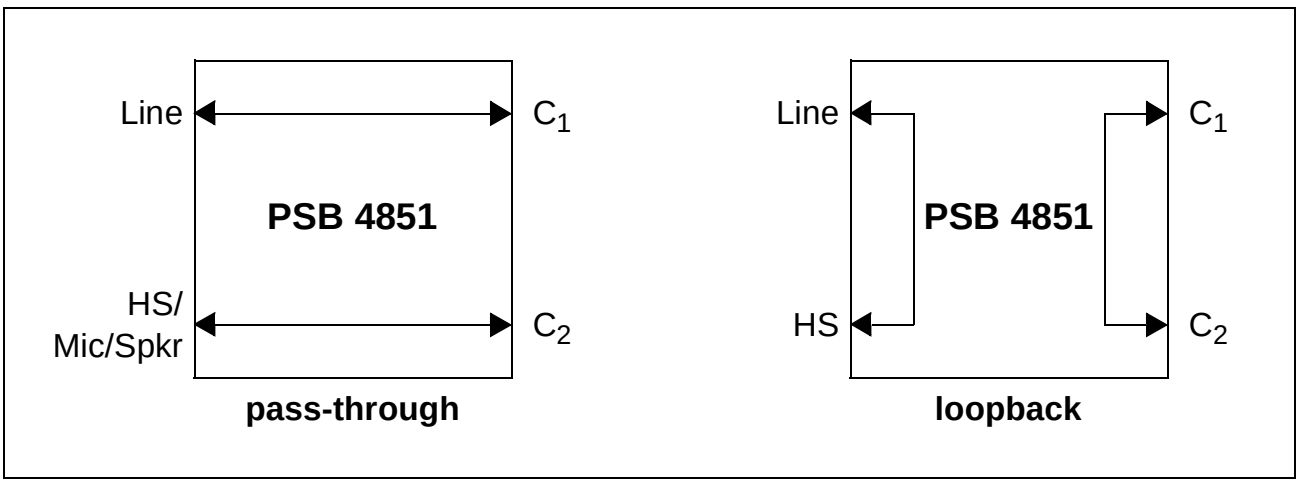


Figure 6
Basic Configurations of PSB 4851

A detailed functional diagram of the PSB 4851 is shown in figure 7.

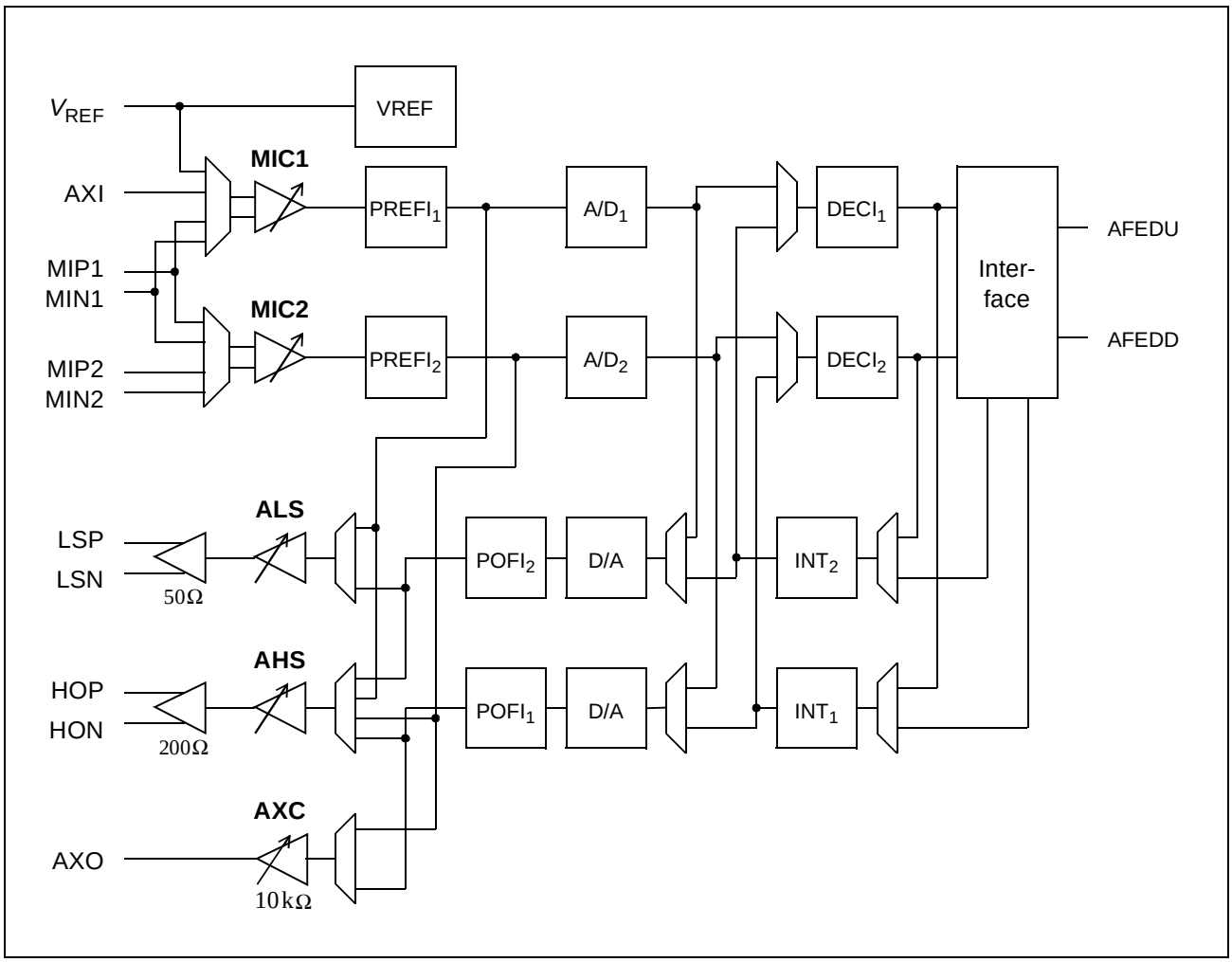


Figure 7
Functional Diagram of PSB 4851

Two differential inputs for microphones and one single ended input for the tip/ring interface are fed to two analog input amplifiers (MIC2, MIC1). These amplifiers can be programmed in steps of 6 dB.

For both the loudspeaker and the handset transducer differential amplifiers (ALS, AHS) are provided. These amplifiers can be programmed within a range of 24 dB in steps of 3 dB or muted.

A third programmable amplifier (AXC) is provided for the tip/ring interface.

2.2 Line Powered Operation

The PSB 4851 supports line powered operation by a flexible power management. The controller can power down all elements that are not needed for the current task. Furthermore, the PSB 4851 can be operated at only 3.3V when the digital parts (A/D, DECI, POFI, D/A and INT) are not needed. In particular, the following three states are useful in line powered operation:

1. **Idle**
   All elements are powered down. The power consumption is minimal. This state is automatically entered by reset.

2. **Ringing**
   MIC1 is in bypass mode, PREFI1 is powered up and ALS is connected to PREFI1. Therefore a signal fed into AXI is amplified by ALS and output at LSP/LSN. In order to maximize the loudness of the ringing signal one of the output drivers of ALS (either LSP or LSN) can be forced to GND thus providing a single ended output. Figure 8 shows the signal routing and the remaining active elements in this mode (single ended mode).

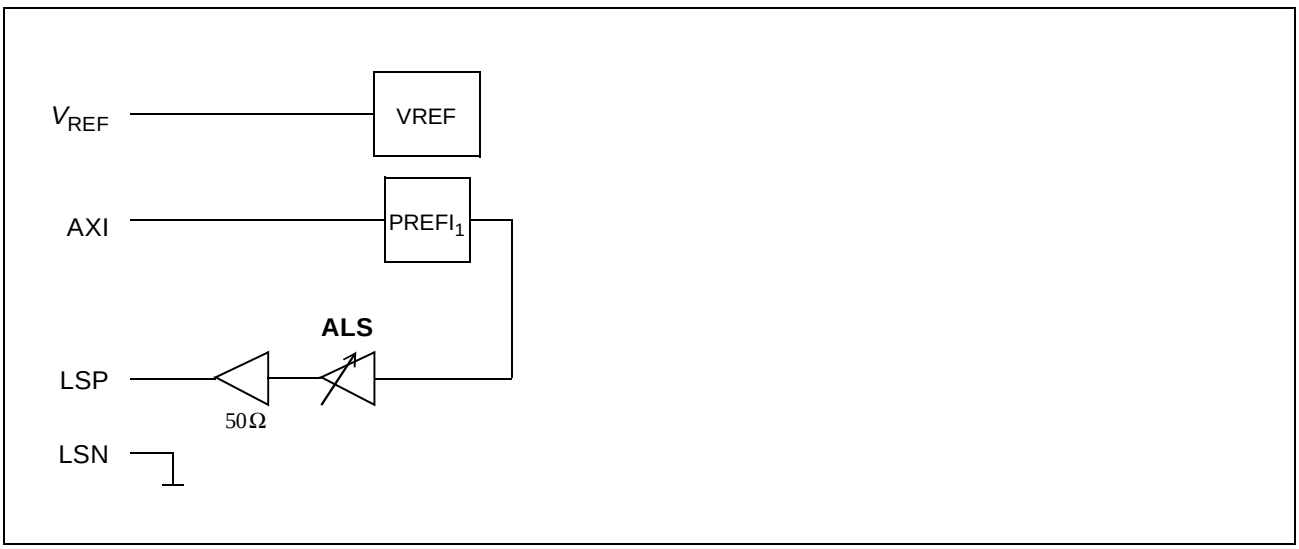


Figure 8
Emergency Ringing Mode

3. **Speech**
   MIC1, PREFI1, MIC2, PREFI2, AHS and AXC are powered up. AHS is connected to PREFI1 and AXC is connected to PREFI2. Therefore the signal fed into MIP2/MIN2 is amplified by MIC2 and AXC and output at AXO. The signal fed into AXI is amplified by MIC1 and AHS and output at HOP/HON. Figure 9 shows the signal routing and the active elements.

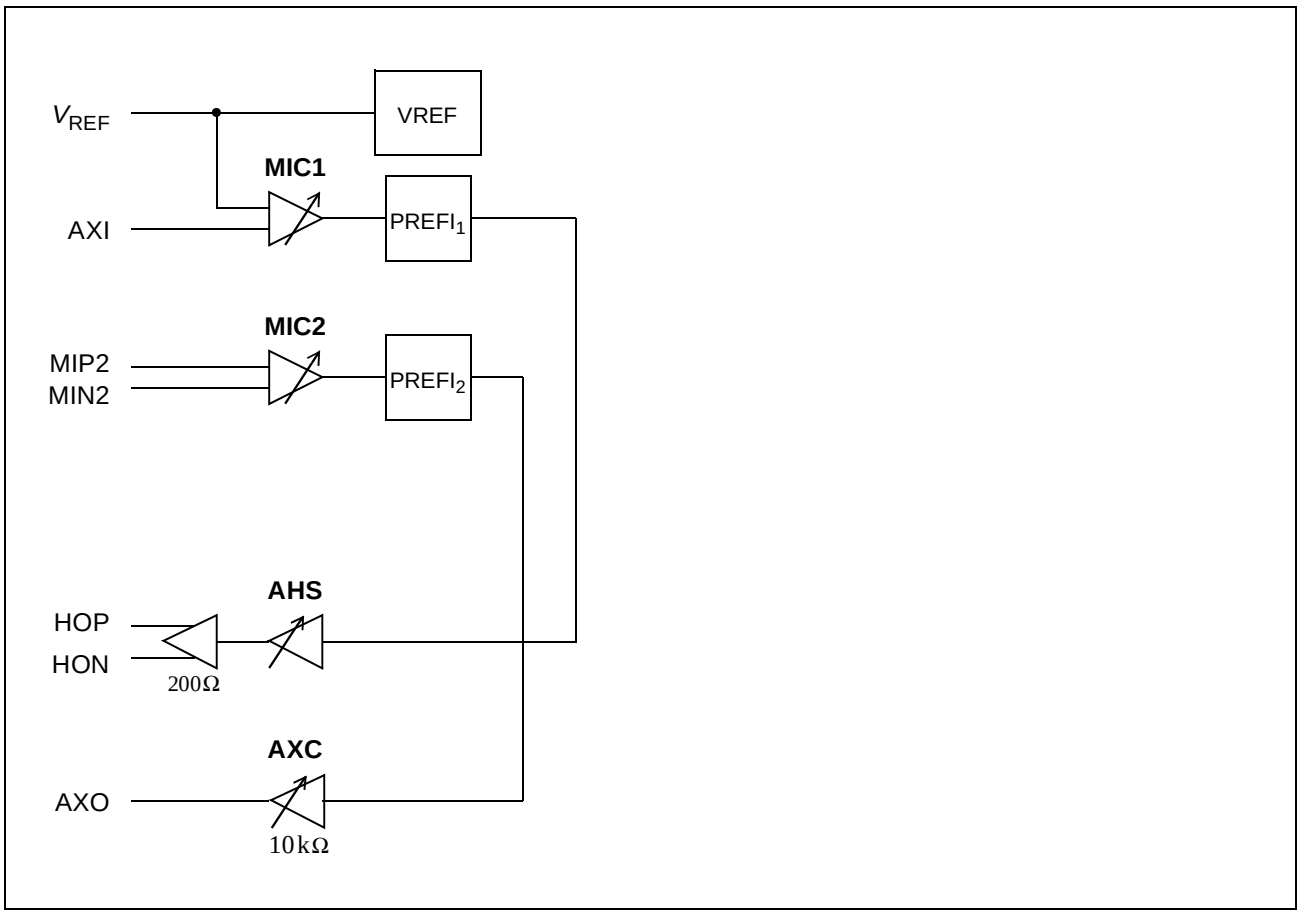


Figure 9
Emergency Speech Mode

Note: An external circuitry should be provided to detect power failure and inform the controller. The controller in turn should reduce the gain of the ALS amplifier if necessary to avoid excessive power consumption.

Note: The serial control interface must remain operational even when some of the connected devices are without power supply. Some devices have clamping diodes at their inputs and might block the bus.

2.3 Analog Front End Interface

The PSB 4851 uses a four wire interface similar to the IOM®-2 interface to exchange information in the digital domain. The main difference is that all timeslots and the channel assignments are fixed as shown in figure 10.

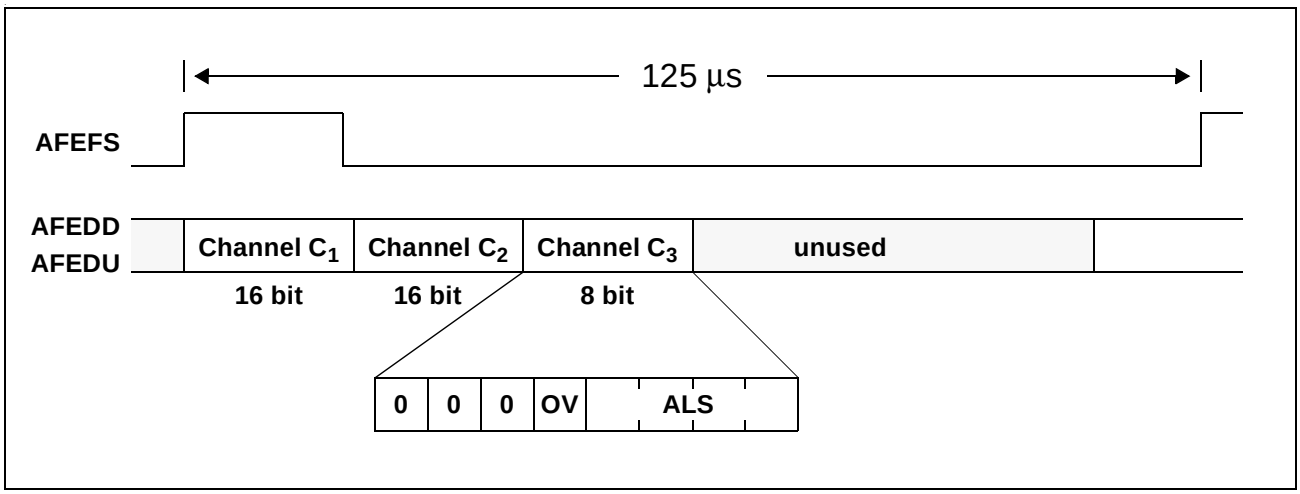


Figure 10
AFE Interface - Frame Structure

Voice data is transferred in 16 bit linear coding in two bidirectional channels C_1 and C_2. For controlled loudhearing an auxiliary channel C_3 is used to transfer the current setting of the loudspeaker amplifier ALS to the PSB 4860. The remaining bits are fixed to zero. In the other direction C_3 transfers an override value for ALS from the PSB 4860 to the PSB 4851. An additional override bit OV determines if the currently transmitted value should override the AOAR:LSC setting. The AOAR:LSC setting is not affected by C_3:ALS override. Table 2 shows the source control of the gain for the ALS amplifier.

Table 2

AOPR:OVRE	C_3:OV	Gain of ALS amplifier
0	-	AOAR:LSC
1	0	AOAR:LSC
1	1	C_3:ALS

Therefore the PSB 4860 can control the gain of the loudspeaker amplifier (ALS) independently from the gain of the handset amplifier (AHS) as shown in figure 11.

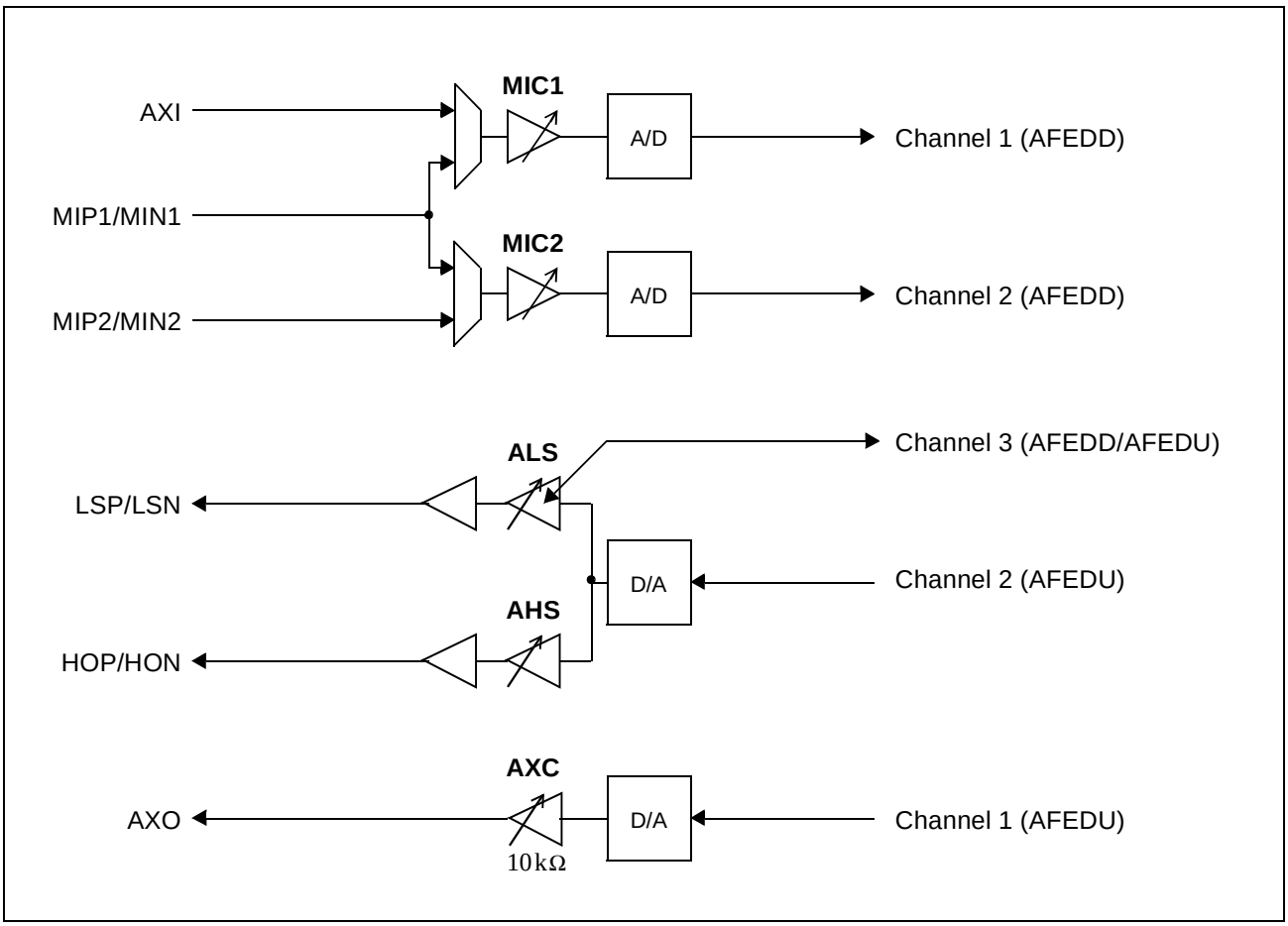


Figure 11
AFE Interface - Signal Routing

Figure 12 shows the synchronization of a frame by AFEFS. The first clock of a new frame (T_1) is indicated by AFEFS switching from low to high before the falling edge of T_1. AFEFS may remain high during subsequent cycles up to T_{32}.

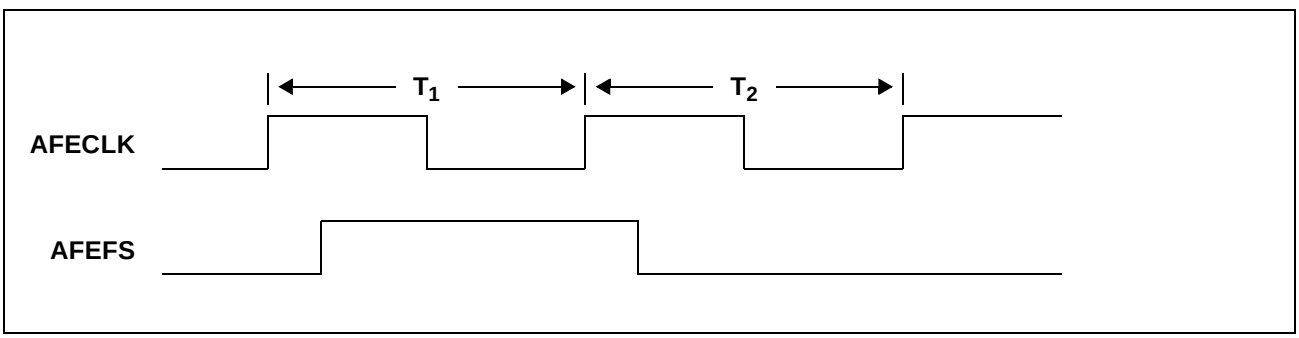


Figure 12
AFE Interface - Frame Start

The data is shifted out with the rising edge of AFECLK and sampled at the falling edge of AFECLK (figure 13).

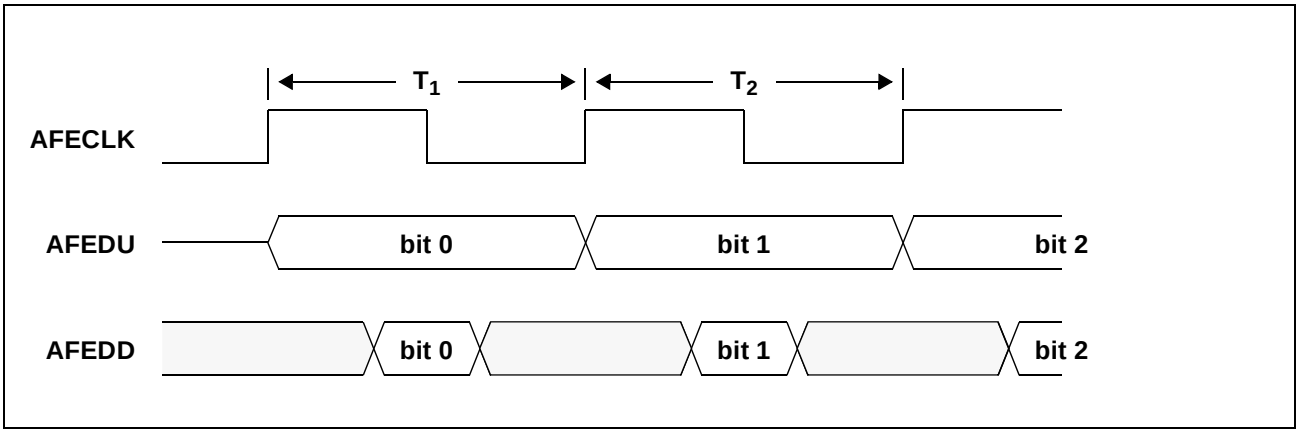


Figure 13
AFE Interface - Data Transfer

If AOPR:OVRE is not set, the channel C_3 is not used by the PSB 4851. All values (C_1, C_2, C_3:ALS) are transferred MSB first. The data clock (AFECLK) rate is fixed at 6.912 MHz. Table 3 shows the clock cycles used for the three channels.

Table 3

Clock Cycles	AFEDD (driven by PSB 4860)	AFEDU (driven by PSB 4851)
T_1-T_{16}	C_1 data	C_1 data
T_{17}-T_{32}	C_2 data	C_2 data
T_{33}-T_{40}	C_3 data	C_3 data
T_{41}-T_{864}	0	tristate

2.4 Serial Control Interface

The serial control interface (SCI) uses four lines. Data is transferred by the lines SDR and SDX at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of an access. Data is sampled by the PSB 4851 at the rising edge of SCLK and shifted out at the falling edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$.

Data is transferred in bytes (8 bits). Data from the controller is latched into a register at the rising edge of $\overline{CS}$. Figure 14 shows a write access to the PSB 4851 and figure 15 shows a read access to the PSB 4851.

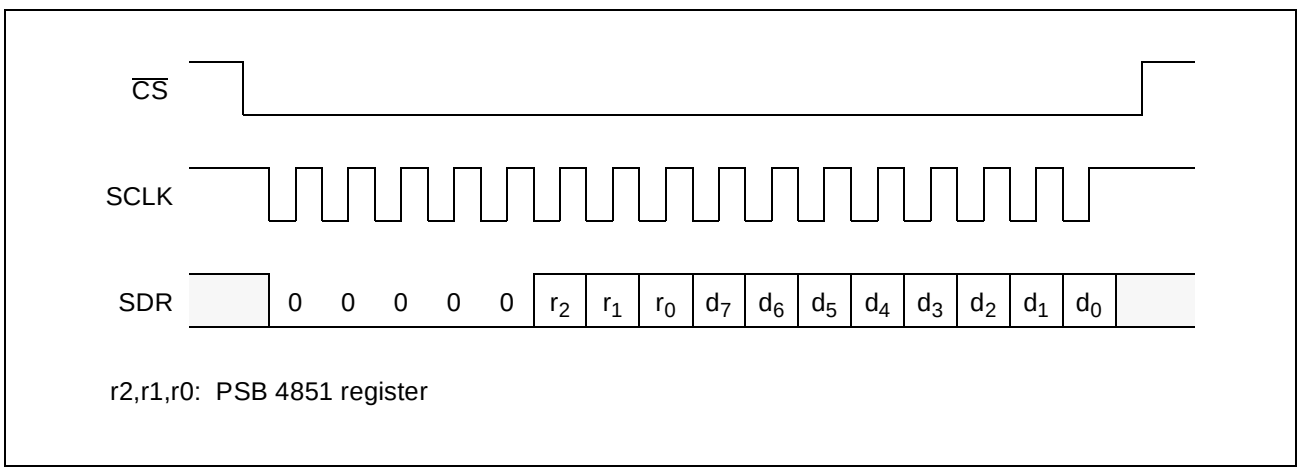


Figure 14
SCI Interface - Write Access

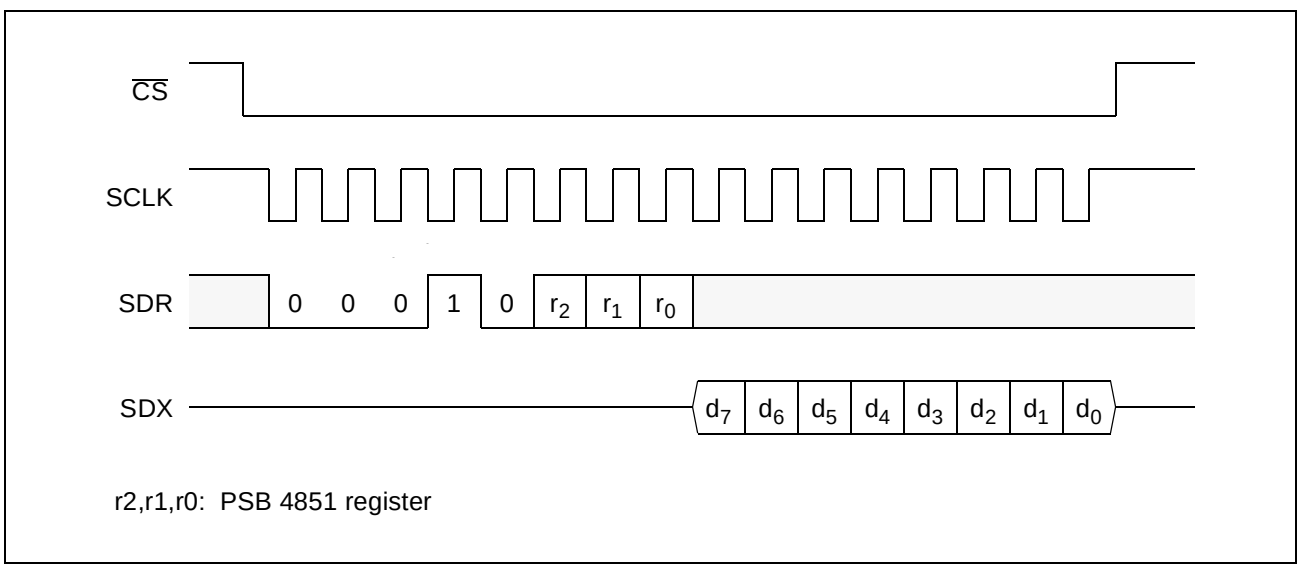


Figure 15
SCI Interface - Read Access

3 Register Description

A summary of the registers of the PSB 4851 is presented in table 4.

Table 4

Name	Reg	7							0
AIAR	**1**	MIC2				MIC1			
AIPR	**2**	0	ADC2	ADC1	EVREF	0	0	ISS	
AOAR	**3**	HOC				LSC			
AOCR	**4**	SEM	AXC			DHOP	DHON	DLSP	DLSN
AOPR	**5**	OSS			DAC2	DAC1	PSS	0	OVRE
TFCR	**6**	DHPR	DHPX	ALTF			DLTF		RT
TMR	**7**	TM			0	0	0	0	0

All registers are set to 0 after reset.

REG 1: AIAR - AFE Input Amplification Register

7							0
MIC2				MIC1			

MIC1 MIC1 amplifier control

3	2	1	0	Description
0	0	0	0	MIC1and PREFI1 are in power down mode
0	0	0	1	0 dB amplification
0	0	1	0	6 dB amplification
0	0	1	1	12 dB amplification
0	1	0	0	18 dB amplification
0	1	0	1	24 dB amplification
0	1	1	0	30 dB amplification
0	1	1	1	36 dB amplification
1	0	0	0	42 dB amplification
1	1	1	1	MIC1 is in bypass mode, PREFI1 is powered up

MIC2 MIC2 amplifier control

7	6	5	4	Description
0	0	0	0	MIC2 and PREFI2 are in power-down mode
0	0	0	1	0 dB amplification
0	0	1	0	6 dB amplification
0	0	1	1	12 dB amplification
0	1	0	0	18 dB amplification
0	1	0	1	24 dB amplification
0	1	1	0	30 dB amplification
0	1	1	1	36 dB amplification
1	0	0	0	42 dB amplification
1	1	1	1	MIC2 is in bypass mode, PREFI2 is powered up

REG 2: AIPR - AFE Input Path Register

7						0
0	ADC2	ADC1	EVREF	0	0	ISS

ISS Input Source Selection

1	0	Description
0	0	reserved
0	1	AXI connected to A/D1, MIP1/MIN1 connected to A/D2
1	0	MIP1/MIN1 connected to A/D1, MIP2/MIN2 connected to A/D2
1	1	AXI connected to A/D1, MIP2/MIN2 connected to A/D2

EVREF Enable VREF

0: VREF module is enabled when any other module needs the reference voltage

1: VREF module always enabled

ADC1 A/D Control 1

0: A/D_1 is in power down mode

1: A/D_1 active

ADC2 A/D Control 2

0: A/D_2 is in power down mode

1: A/D_2 active

Note: If ADC1 and ADC2 are set to 0 then DEC_1, DEC_2, INT_1, INT_2 and the timing generation are also forced into power down mode.

REG 3: AOAR - AFE Output Amplification Register

7							0
HOC				LSC			

LSC Loudspeaker Amplifier Control

3	2	1	0	Description
0	0	0	0	ALS is in power-down mode
0	0	0	1	11.5 dB amplification
0	0	1	0	8.5 dB amplification
0	0	1	1	5.5 dB amplification
0	1	0	0	2.5 dB amplification
0	1	0	1	-0.5 dB amplification
0	1	1	0	-3.5 dB amplification
0	1	1	1	-6.5 dB amplification
1	0	0	0	-9.5 dB amplification
1	0	0	1	-12.5 dB amplification
1	0	1	0	-15.5 dB amplification
1	0	1	1	-18.5 dB amplification
1	1	0	0	-21.5 dB amplification
1	1	1	1	ALS is in bypass mode

HOC Handset Amplifier Control

7	6	5	4	Description
0	0	0	0	AHS is in power-down mode
0	0	0	1	2.5 dB amplification
0	0	1	0	-0.5 dB amplification
0	0	1	1	-3.5 dB amplification
0	1	0	0	-6.5 dB amplification
0	1	0	1	-9.5 dB amplification
0	1	1	0	-12.5 dB amplification
0	1	1	1	-15.5 dB amplification
1	0	0	0	-18.5 dB amplification
1	0	0	1	-21.5 dB amplification
1	1	1	1	AHS is in bypass mode

REG 4: AOCR - AFE Output Configuration Register

7					0
SEM	AXC	DHOP	DHON	DLSP	DLSN

DLSN Disable Loudspeaker Amplifier Output N

0: LSN output of ALS amplifier controlled by LSC setting

1: LSN controlled by SEM setting

DLSP Disable Loudspeaker Amplifier Output P

0: LSP output of ALS amplifier controlled by LSC setting

1: LSP controlled by SEM setting

DHON Disable Handset Amplifier Output N

0: HON output of AHS amplifier controlled by HOC setting

1: HON output of AHS amplifier disabled (power down)

DHOP Disable Handset Amplifier Output P

0: HOP output of AHS amplifier controlled by HOC setting

1: HOP output of AHS amplifier disabled (power down)

AXC Auxiliary Output Control

6	5	4	Description
0	0	0	AXO is in power-down mode
0	0	1	-6 dB amplification
0	1	0	-9 dB amplification
0	1	1	-12 dB amplification
1	0	0	-15 dB amplification
1	0	1	-18 dB amplification
1	1	0	-21 dB amplification
1	1	1	-24 dB amplification

SEM Single Ended Mode

0: LSN (LSP) fixed to GND

1: LSN (LSP) tristated

REG 5: AOPR - AFE Output Path Register

7					0
OSS	DAC2	DAC1	PSS	0	OVRE

OVRE Override Enable

0: Gain for ALS is always defined by LSC

1: Gain for ALS can be overridden by interchip communication

DAC1 D/A Control 1

0: $POFI_1$ and $D/A_1$are in power down mode

1: $POFI_1$ and D/A_1 are active

PSS Power Supply Selection

0: 3.3V power supply (all digital parts must be powered down)

1: 5V power supply

DAC2 D/A Control 2

0: $POFI_2$ and D/A_2 are in power down mode

1: $POFI_2$ and D/A_2 are active

OSS Output Source Selection

7	6	5	Description
0	0	0	ALS and AHS are connected to $PREFI_1$, AXC is connected to $PREFI_2$ $POFI_1$ and $POFI_2$ must be set to power down
0	0	1	ALS is connected to $PREFI_1$, AHS and AXC are connected to $PREFI_2$ $POFI_1$ and $POFI_2$ must be set to power down
0	1	-	reserved
1	0	-	reserved
1	1	0	ALS and AHS are connected to $POFI_2$, AXC is connected to $POFI_1$
1	1	1	ALS is connected to $POFI_2$, AHS and AXCare connected to $POFI_1$

REG 6: TFCR - Test Function Configuration Register

7				0
DHPR	DHPX	ALTF	DLTF	RT

DHPR Disable High-Pass (Receive Direction)

0: High Pass activated (Receive)

1: High Pass disabled (Receive)

DHPX Disable High-Pass (Transmit Direction)

0: High Pass activated (Transmit)

1: High Pass disabled (Transmit)

ALTF Analog Loop Test Function

5	4	3	Description
0	0	0	Normal Mode
0	0	1	Analog Loop via Front End
0	1	0	Analog Loop via Converter
0	1	1	Analog Loop via 64kHz
1	0	0	Analog Loop via Interface

DLTF Digital Loop Test Function

2	1	Description
0	0	Normal Mode
0	1	Digital Loop via PCM register
1	0	Digital Loop via 64kHz
1	1	Digital Loop via Noiseshaper

RT Ram Test

0: normal mode

1: RAM initialization test (internal test only)

REG 7: TMR - Test Mode Register

7					0
TM	0	0	0	0	0

TM Test Mode

7	6	5	Description
0	0	0	Normal Mode
1	-	-	Reserved
-	1	-	Reserved
-	-	1	Reserved

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A [1)]	– 25 to 80	°C
Storage temperature	T_{STG}	– 65 to125	°C
Voltage on any pin with respect to ground	V_S	– 0.3 to V_{DD} + 0.3	V
Maximum voltage on any pin	V_{max}	7	V

1) Reduced performance e.g. noise and gain tracking

ESD-integrity (according MIL-Std 883D, method 3015.7): 1000 V
exception: The pins #16, #18, #19 and #20 are not protected against voltage stress > 630 V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.2 DC Characteristics (5 V)

$V_{DDD}/V_{DDA}/V_{DDP}$ = 5 V ± 5%; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input leakage current	I_{IL}	– 1.0		1.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
H-input level	V_{IH}	2.0		V_{DD} + 0.3	V	
L-input level	V_{IL}	– 0.3		0.8	V	
H-output level (AFEDU only)	V_{OH}	V_{DD} – 0.45			V	I_O = 2 mA
L-output level	V_{OL}			0.45	V	I_O = – 2 mA
Input capacitance	C_I			10	pF	
Output capacitance	C_O			15	pF	
V_{DD} standby supply current	I_{DDS1}			50	µA	power down (after reset, no clock on AFECLK)
	I_{DDS2}		1.3	1.8	mA	V_{VREF} = ON
V_{DD} supply current operating [1)]	I_{DDO1}		3.0	3.8	mA	emergency ringing via ALS (single ended mode)
	I_{DDO2}		4.1	5.1	mA	emergency handset mode (differential mode)
	I_{DDO3}		15.5	20.0	mA	full operation (loudhearing)

1) Operating power dissipation is measured with all analog outputs open. All analog inputs are set to V_{REF}. For the emergency ringing mode, the tone generator of the controller is used (square wave). In this mode the loudspeaker amplifier gain is set by the controller.

4.3 DC Characteristics (3.3 V)

$V_{DDD}/V_{DDA}/V_{DDP}$ = 3.3 V - 3.6 V; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input leakage current	I_{IL}	– 1.0		1.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
H-input level	V_{IH}	1.3		V_{DD} + 0.3	V	
L-input level	V_{IL}	– 0.3		0.5	V	
H-output level	V_{OH}	V_{DD} – 0.45			V	I_O = 2 mA
L-output level	V_{OL}			0.45	V	I_O = – 2 mA
Input capacitance	C_I			10	pF	
Output capacitance	C_O			15	pF	
V_{DD} standby supply current	I_{DDS1}			50	µA	power down (after reset, no clock on AFECLK)
	I_{DDS2}		1.3	1.8	mA	V_{VREF} = ON
V_{DD} supply current	I_{DDO1}		3.0	3.8	mA	emergency ringing via ALS, single ended mode
operating [1]	I_{DDO2}		4.1	5.1	mA	emergency handset mode, differential mode

1) Operating power dissipation is measured with all analog outputs open. All analog inputs are set to V_{REF}.

4.4 AC Characteristics

Digital inputs are driven to 2.4 V for a logical “1” and to 0.45 V for a logical “0”. Timing reference points are 2V and 0.8 V. The AC-testing waveforms are shown below.

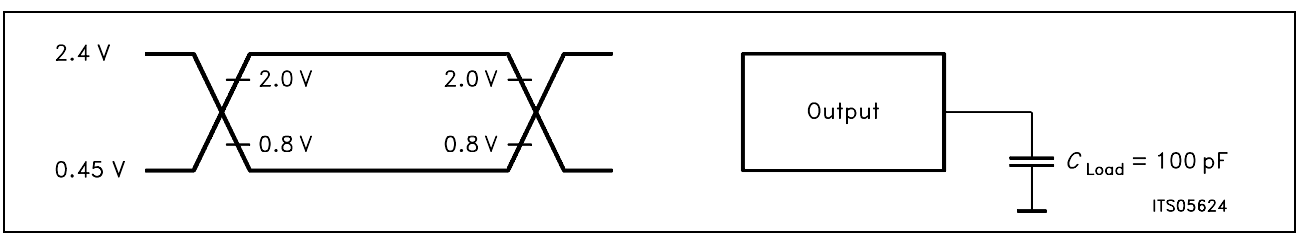


Figure 38
Input/Output Waveforms for AC-Tests

Analog Front End Input Characteristics [1)]

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
AXI-input impedance	Z_{AXI}	12.5	20.5		kΩ	300 – 3400 Hz
AXI-input voltage swing	V_{AXI}			19.3	mVpk	42 dB, V_{dd}=5 V
AXI-input voltage swing	V_{AXI}			1.67	Vpk	0 dB, V_{dd}=5 V
AXI-input voltage swing	V_{AXI}			12	mVpk	42 dB, V_{dd}=3.3 V
AXI-input voltage swing	V_{AXI}			0.75	Vpk	0 dB, V_{dd}=3.3 V
AXI-gain	G_{AXI}			42	dB	9.55 mV @ 1 kHz
AXI-input impedance in bypass-mode	Z_{AXI}	160	270		kΩ	300 – 3400 Hz
AXI-gain in bypass-mode	G_{AXI}			0	dB	1V @ 1 kHz
MIP/MIN1,2-input voltage swing	$V_{MIP/MIN}$			19.3	mVpk	42 dB, V_{dd}=5 V
MIP/MIN1,2-input voltage swing	$V_{MIP/MIN}$			12	mVpk	42 dB, V_{dd}=3.3 V
MIP/MIN1,2-gain	$G_{MIP/MIN}$			42	dB	9.55 mV @ 1 kHz
RST input	t_{RSTI}	1			µs	

Analog Front End Output Characteristics

AHO-output impedance	Z_{AHO}			2	Ω	300 – 3400 Hz
AHO-output voltage swing [1)]	V_{AHO}			3.2	Vpk	V_{dd} = 5V, load measured from HOP to HON
AHO-output voltage swing [1)]	V_{AHO}			2.0	Vpk	V_{dd} = 3.3V, load measured from HOP to HON
ALS-output impedance	Z_{ALS}			2	Ω	300 – 3400 Hz
ALS-output voltage swing [1)]	V_{ALS}			3.2	Vpk	V_{dd} = 5V, load measured from LSP to LSN

[1] The maximum voltage swing at the internal paths corresponds to the maximum PCM-code (± 127).

Electrical Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
ALS-output voltage swing [1]	V_{ALS}			2.0	Vpk	V_{dd}= 3.3V, load measured from LSP to LSN
AXO-output impedance	Z_{AXO}		15	21	Ω	300 – 3400 Hz
AXO-output voltage swing [1]	V_{AXO}			1.2	Vpk	V_{dd} = 5V, load measured from AXO to GND
AXO-output high voltage [1]	V_{AXOH}			3.6	Vpk	V_{dd} = 5V, input load – 0.12 mA reference: GND
AXO-output low voltage [1]	V_{AXOL}			1.2	Vpk	V_{dd} = 5V, input load + 0.12 mA reference: GND
AXO-output voltage swing [1]	V_{AXO}			0.7	Vpk	V_{dd} = 3.3V, load measured from AXO to GND
V_{REF} output impedance	Z_{VREF}		3	5	Ω	Load measured from V_{REF} to V_{SSA}
V_{REF} output voltage	V_{VREF}	2.3	2.4	2.5	V	input load – 2 mA
V_{REFBG} output voltage	V_{VREFBG}		1.2		V	with ext. capacitor

Transmission Characteristics

$V_{DDD}/V_{DDA}/V_{DDP}$ = 5 V ± 5%; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 °C

Parameter	Limit Values		Unit	Test Condition
	min.	max.		
Attenuation Distortion @ 0 dBmO	0 – 0.25 – 0.25 – 0.25 – 0.25 0	 0.25 0.45 0.9 	dB dB dB dB dB dB	< 200 Hz 200 – 300 Hz 300 – 2400 Hz 2400 – 3000 Hz 3000 – 3400 Hz > 3400 Hz
Out-of-band signals		 – 35 – 45 – 35 – 40	 dB dB dB dB	receive signal filtering: 4.6 kHz >8.0 kHz transmit: 4.6 kHz >8.0 kHz
Group delay distortion @ 0 dBmO		750 380 130 750	µs µs µs µs	500 – 600 Hz 600 – 1000 Hz 1000 – 2600 Hz 2600 – 2800 Hz
Signal-to-total distortion (sine signal)	50 39 29 24		dB dB dB	0 to – 20dBm0[1)] – 30 dBm0 – 40 dBm0 – 45 dBm0
Gain tracking (sine signal) @ – 10 dBmO	– 0.3 – 0.6 – 1.6	0.3 0.6 1.6	dB dB dB	3 to – 40 dB – 40 to – 50 dB – 50 to – 55 dB
Idle-channel noise (Psophometric)		– 75 – 66	dBmO dBmO	receive transmit
Channel crosstalk		– 75	dB	Reference: 0 dBmO
Programmable gain	– 0.5 – 1.0	0.5 1.0	dB dB	step accuracy overall accuracy

1) For single ended inputs only within gain settings 0 dB to 18db.

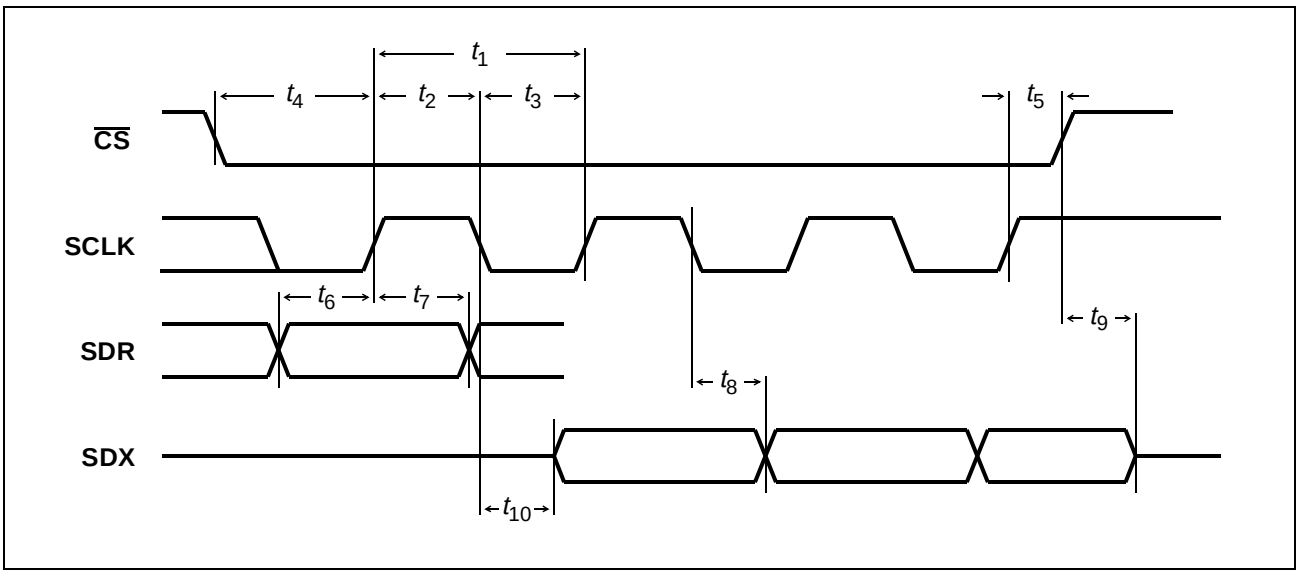


Figure 16
SCI Interface

Parameter SCI Interface	Symbol	Limit values		Unit
		Min	Max	
SCLK cycle time	t_1	500		ns
SCLK high time	t_2	100		ns
SCLK low time	t_3	100		ns
$\overline{CS}$ setup time	t_4	0		ns
$\overline{CS}$ hold time	t_5	10		ns
SDR setup time	t_6	40		ns
SDR hold time	t_7	40		ns
SDX data out delay	t_8		80	ns
$\overline{CS}$ high to SDX tristate	t_9		40	ns
SCLK to SDX active	t_{10}		80	ns

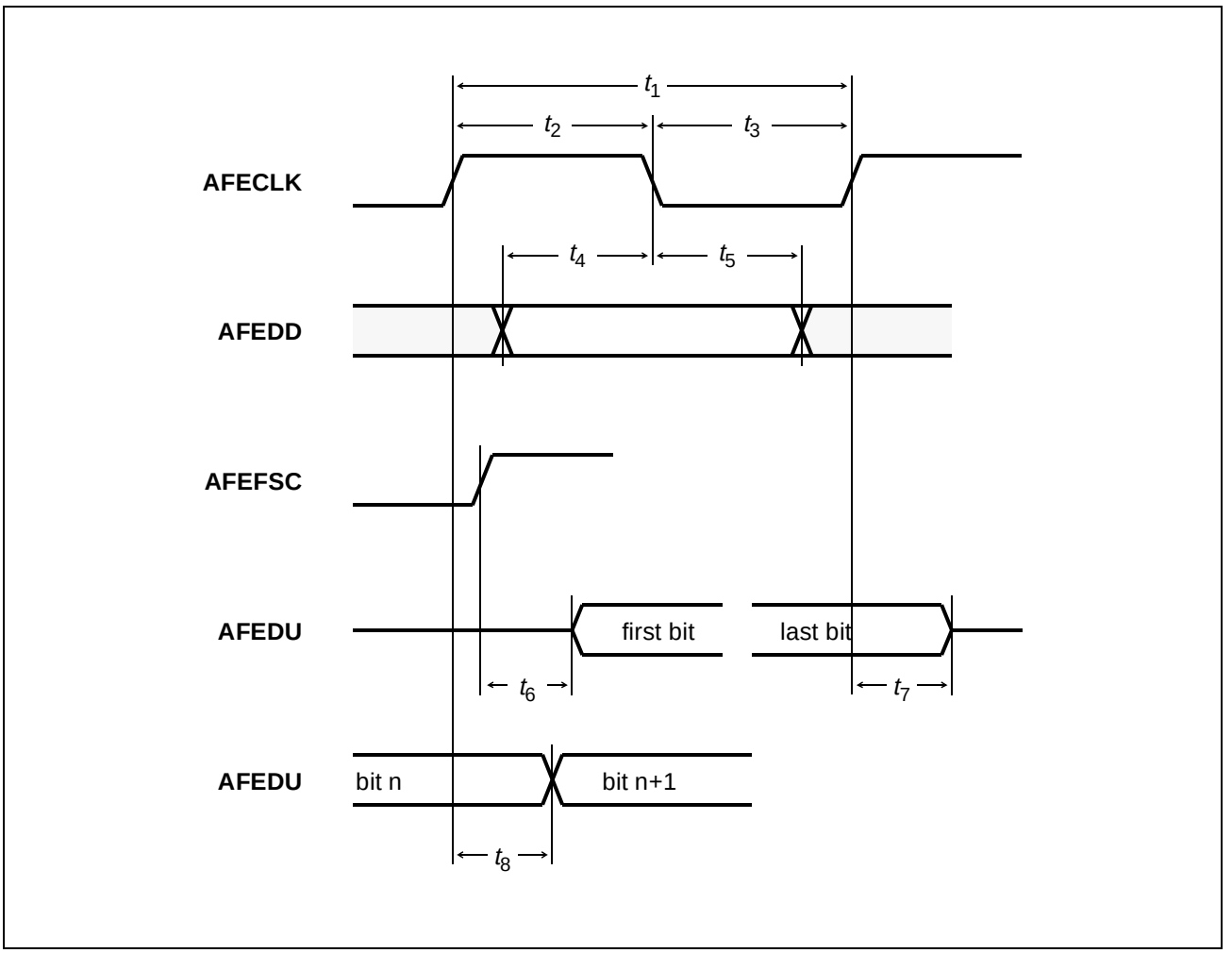


Figure 17
AFE Interface - Bit Synchronization Timing

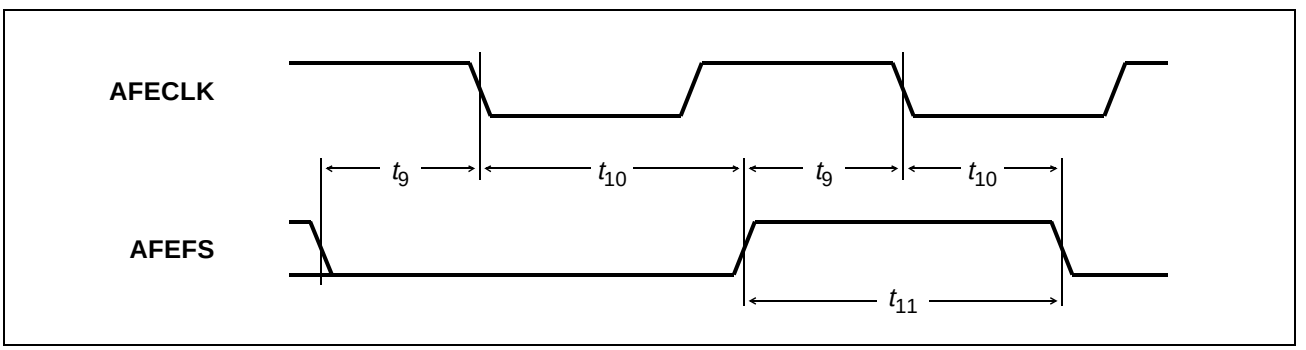


Figure 18
AFE Interface - Frame Synchronization Timing

Electrical Characteristics

Parameter AFE Interface	Symbol	Limit values		Unit
		Min	Max	
AFECLK period	t_1	125	165	ns
AFECLK high	t_2	50		ns
AFECLK low	t_3	50		ns
AFEDD setup	t_4	20		ns
AFEDD hold	t_5	20		ns
AFEDU high impedance to active	t_6		20	ns
AFEDU from active to high impedance	t_7		20	ns
AFEDU output delay	t_8		20	ns
AFEFS setup	t_9	20		ns
AFEFS hold	t_{10}	20		ns
AFEFS high	t_{11}	1		t_1

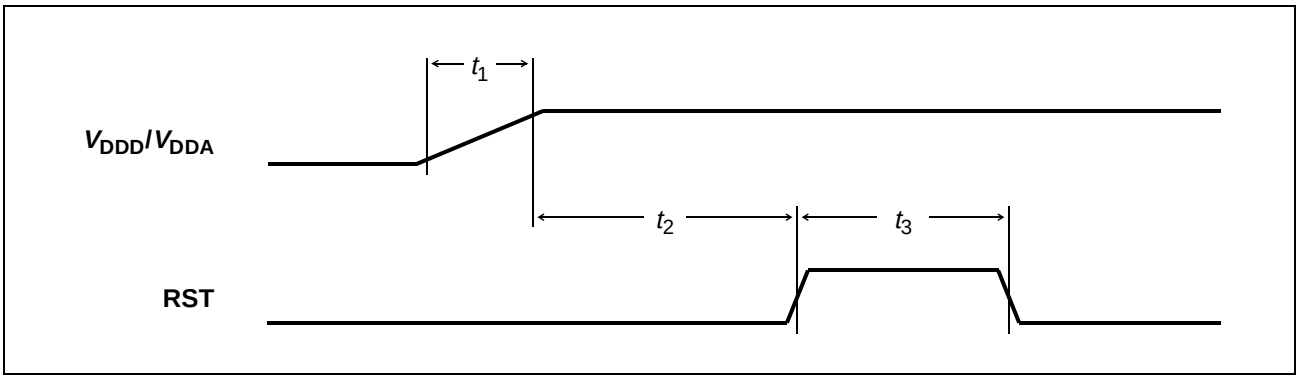
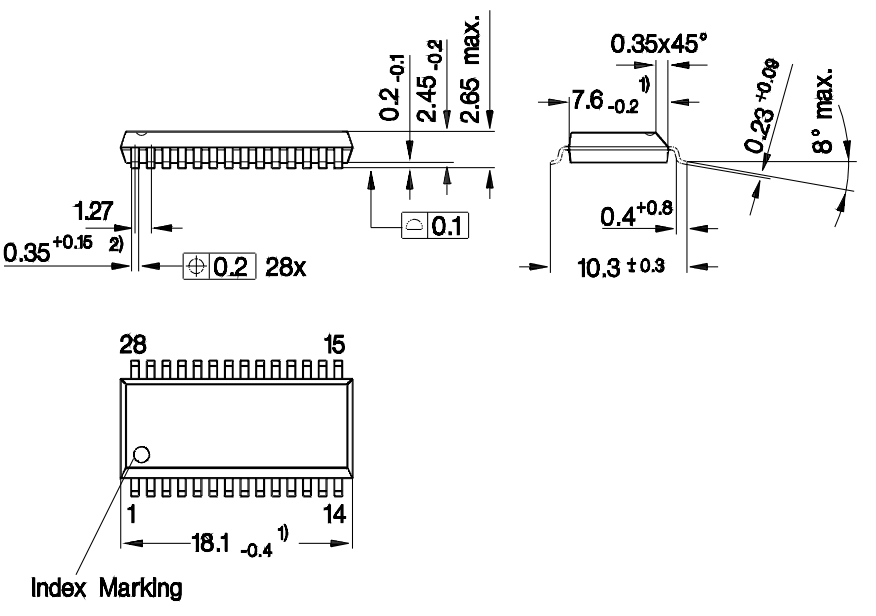


Figure 19
Power and Reset Timing

Parameter Power and Reset Timing	Symbol	Limit values		Unit
		Min	Max	
V_{DDD}/V_{DDA} rise time 5%-95%	t_1		20	ms
Supply voltages stable to RST high	t_2		100	ns
RST high	t_3	100		ns

5 Package Outlines

Plastic Package, P-DSO-28-1 (SMD)
(Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm