SIEMENS

ICs for Communications

Analog Line Interface Solution
ALIS

PSB 4595 Version 2.0
PSB 4596 Version 2.1

Product Overview 08.97

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Previous Version:		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)

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1 Overview

The Analog Line Interface Solution (ALIS), PSB 4595 and PSB 4596, provides in two chips the analog modem front-end with an innovative solution which allows a single hardware design to be used throughout the world.

The PSB 4595 (ALIS-A) provides the fixed functions of the Data Access Arrangement (DAA): hybrid, powering from the telephone line, and analog-to-digital and digital-to-analog conversion. Adaptation to different countries' requirements (DC characteristics, transhybrid balancing, and termination impedance) is provided by downloading coefficient sets, provided by Siemens, to the PSB 4596 (ALIS-D). The ALIS-D additionally provides equalization and adaptation of the receive/transmit level, as well as integrating ring detection, pulse dialing, tone (DTMF) generation, and Caller-ID functions.

- Isolation from the analog line is provided by a capacitive interface. Because there is no transformer, the ALIS has excellent linearity, flat frequency response, and low distortion over the entire voiceband, even at low frequencies.
- Caller-ID (Bell 202 and ITU-T V.23) can function even when the host PC is in sleep mode: the ALIS will save all the information provided by the Central Office (CLIP).
- The ALIS will support a data pump in all modem applications, including V.34+ and all 56 kbps modem techniques.
- High level of integration allows ALIS applications to have a small form factor, making it ideal for PCMCIA applications.

The ALIS front-end is an effective partner for a data pump or a host-based software modem. Its adaptability makes it a perfect match for mobile computer modems.

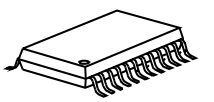
Analog Line Interface Solution
ALIS

PSB 4595
PSB 4596

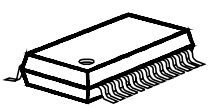
CMOS

2 Features

- Fully programmable Data Access Arrangement (DAA) to meet all countries' requirements with one design: DC characteristics, transhybrid balancing, termination impedance matching, receive/transmit level adaptation, and equalization.
- Innovative interface replaces the conventional transformer by a capacitive link, providing better transmission at low frequencies and higher data transfer rate.
- Integration of ring detection, pulse dialing, and DTMF generation.
- Programmable Caller-ID receiver, including storage of CID when the PC is in sleep mode.
- 16-bit linear codec meets requirements for V.34bis and all 56 kbps modem techniques.
- Analog side line-fed (by tip/ring) to minimize power consumption.



P-TSSOP24

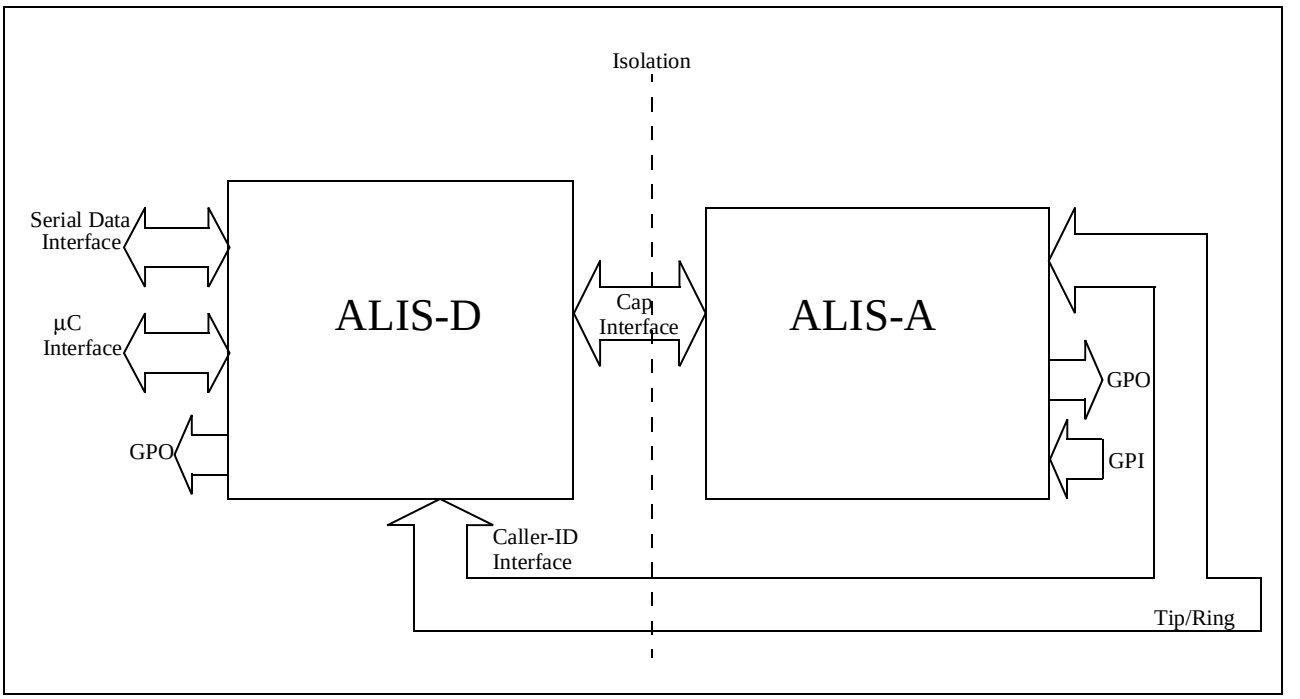


P-SSOP28

- Wake-Up function to support PC power management.
- Flexible digital interface for adaptation to different data pumps.
- High-pass filter in receiver to suppress disturbance from the power supply (50/60 Hz). This can be switched on or off.
- Two-chip solution: the P-TSSOP24 and P-SSOP28 package is PCMCIA conformant.
- General purpose I/O pins.

Type	Ordering Code	Package
PSB 4595 V2.0	Q67106-H6754	P-TSSOP24
PSB 4596 V2.1	Q67106-H6755	P-SSOP28

3 Logic Symbol



GPI: General Purpose Input
GPO: General Purpose Output

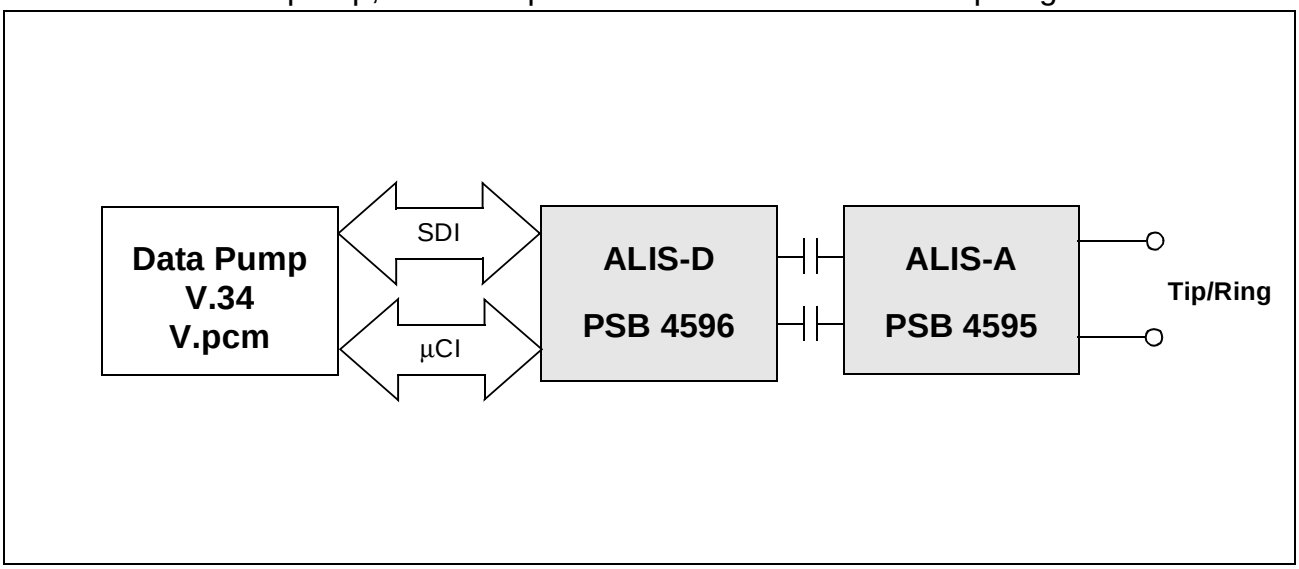
Figure 1 Logic Symbol of the ALIS Chipset

4 Typical Applications

The ALIS can be used both in collaboration with a DSP chip and with host-based software modems, providing the DAA with a minimum of external components.

4.1 ALIS with DSP-based Modem

For a modem data pump, the ALIS provides the front-end to the tip/ring.



Note: SDI: Serial Data Interface
µCI: µ-Controller Interface

Figure 2 DSP-based Modem Application

Isolation is provided by a capacitive interface, without transformer. This allows very flat frequency response over the entire voice band, even at low frequencies.

In PCM Modem applications, the 50/60 Hz high-pass filter can be turned off.

4.2 ALIS with Software Modem

The ALIS can also be used in a host-based software modem application, in which V.34 or the PCM Modem techniques are run on the host. In this application, the Serial Data Interface (SDI) is connected to the USB or PCI interface via a FIFO structure.

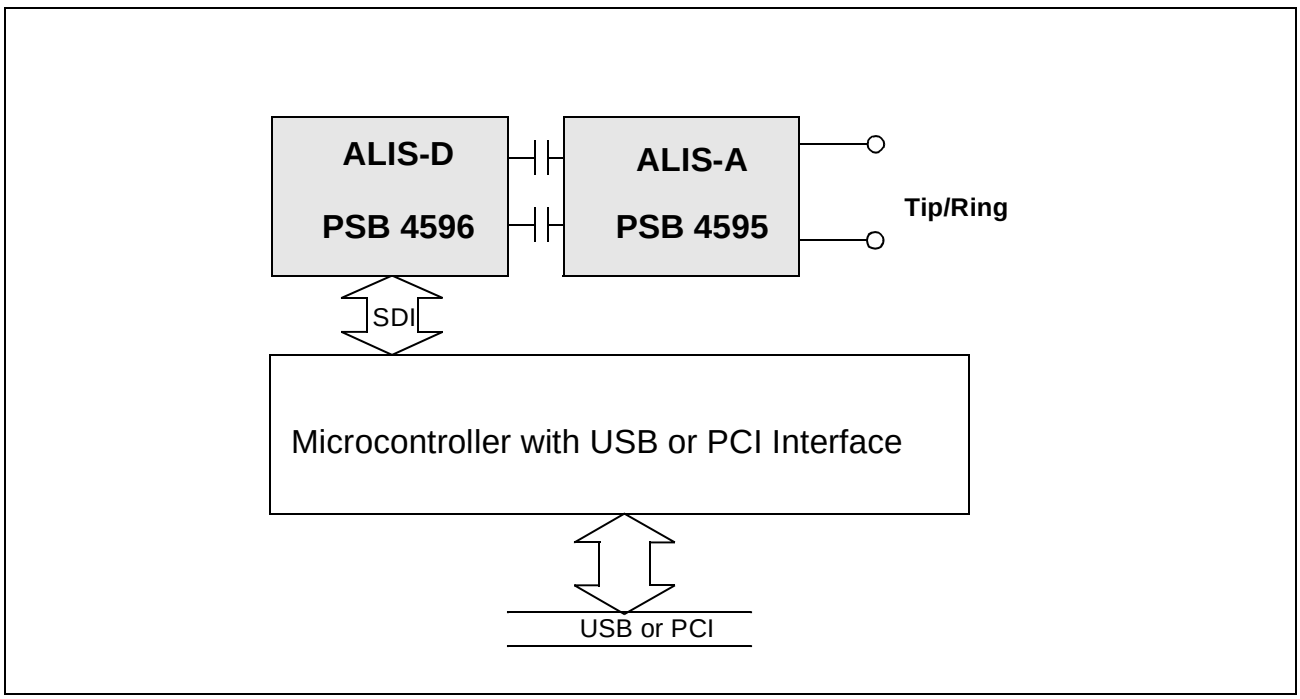


Figure 3 Software Modem Application

4.3 Hybrid Modem (ISDN plus Analog)

The ALIS can be combined with a SIEMENS ISDN chipset to support hybrid modems, with both tip/ring and ISDN (S- or U-interface) connection.

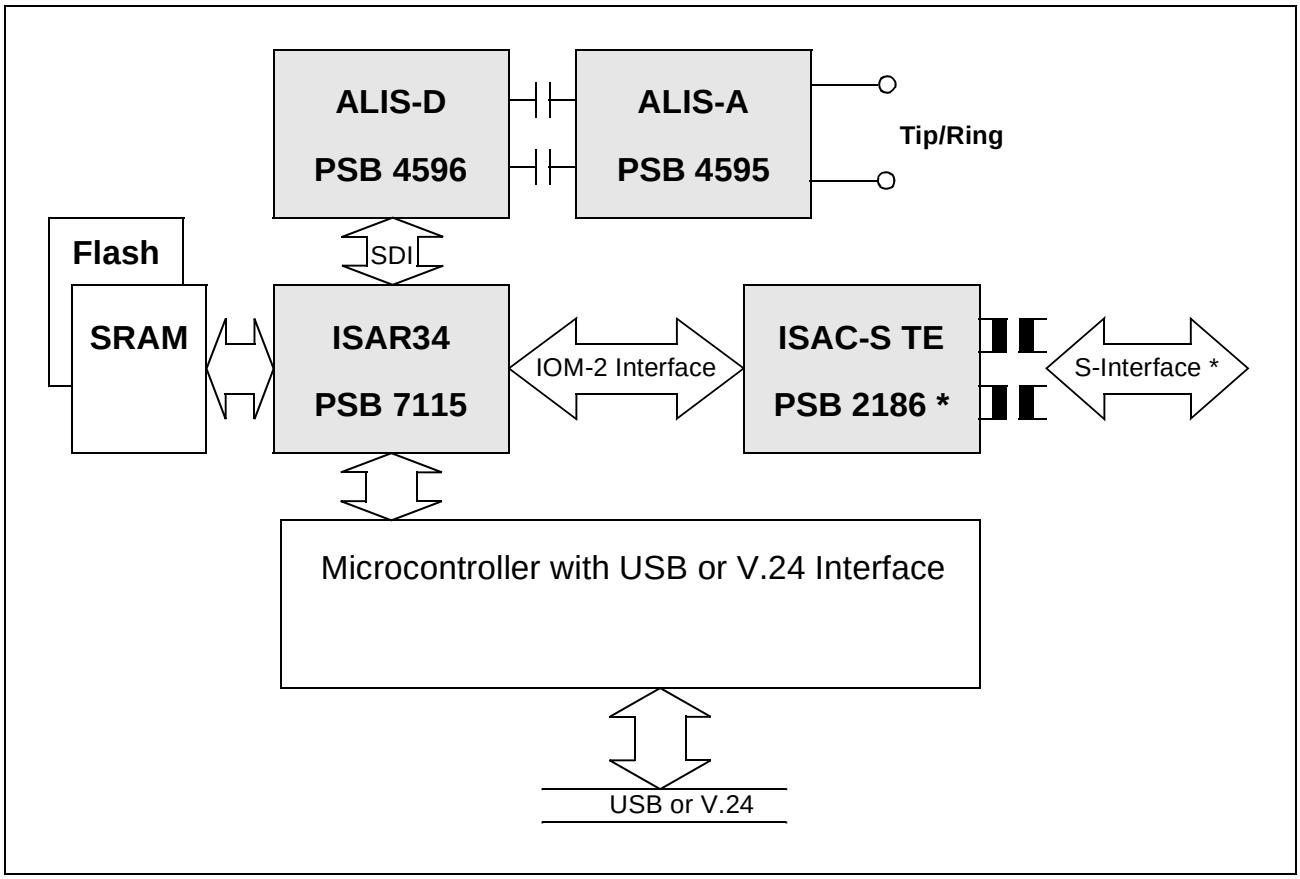


Figure 4 Hybrid Modem Application, with S-interface: ISAR34 Enhanced Data Access Controller (PSB 7115) and ISDN Access Controller for S-bus ISAC-S TE (PSB 2186)

* Figure 4 shows a hybrid modem with the ISDN S-interface. To meet the ISDN U-interface, the ISAC-S TE PSB 2186 is replaced by the IEC-Q TE PSB 21911.

4.4 Modem plus Speakerphone

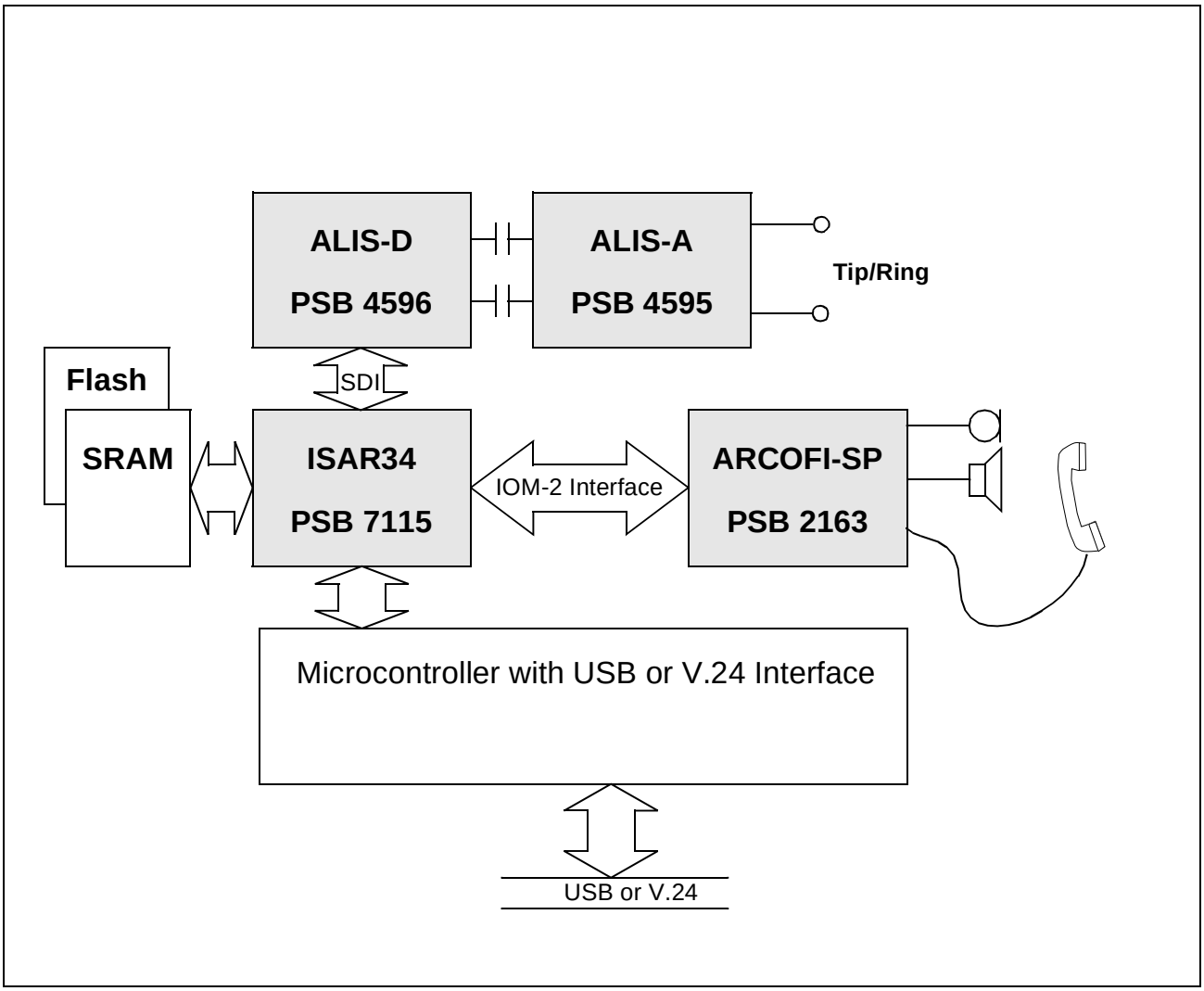


Figure 5 Application with Speakerphone: ARCOFI-SP Audio Ringing Codec (PSB 2163) and ISAR34 Enhanced Data Access Controller (PSB 7115)

5 Functional Description

The ALIS chip set provides all the major parts of the front-end for modem solutions. The circuit consists of two components: a codec filter and an electronic DAA. Ring Detection, Pulse Dialing and Caller-ID functions are integrated on-chip. Different operating states (Sleep, Conversation, Ringing, etc.) have been implemented to allow the ALIS to consume minimal power.

5.1 Block Diagram

The tip/ring telephone line interface is connected mainly with the ALIS-A. It is also connected with the ALIS-D for Caller-ID functions.

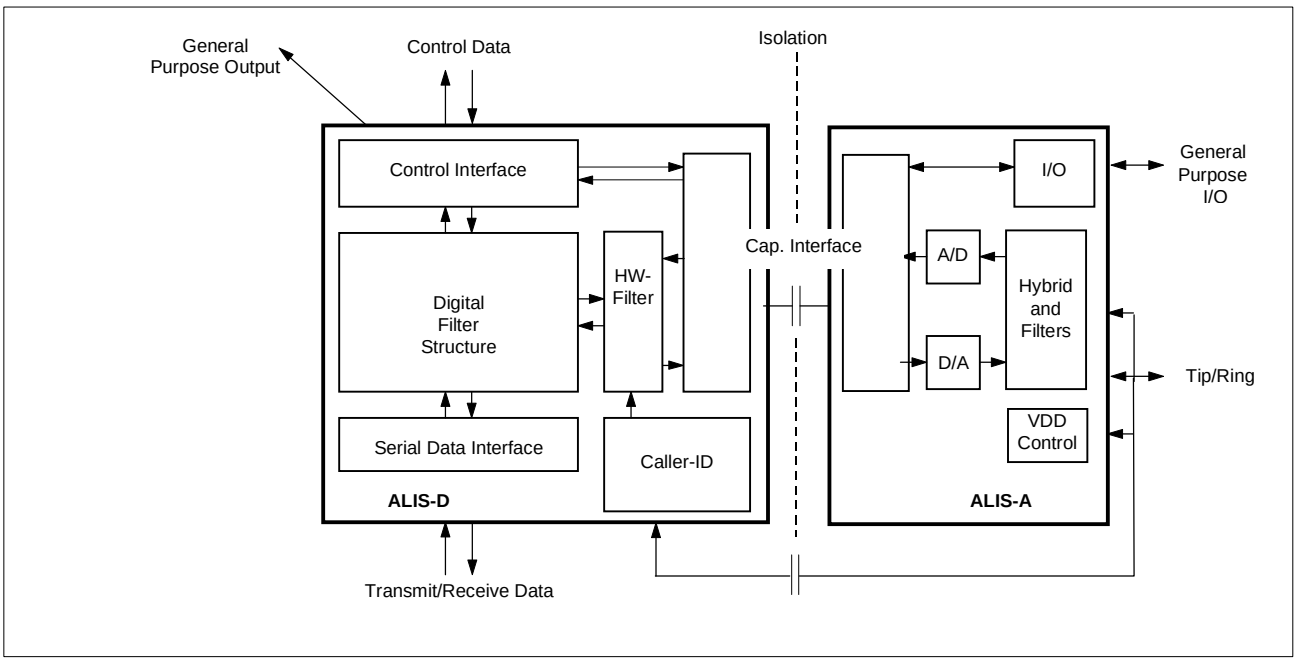


Figure 6 ALIS Block Diagram

ALIS-A

At the ALIS-A, the tip/ring interfaces with:

- VDD Control: this sets the level of the supply voltage for the ALIS-A. The level is selected by program.

- Hybrid and Filters: the hybrid provides two-wire to four-wire conversion, and the analog anti-aliasing pre-filters and smoothing post-filters provide signal conditioning.

The modem data path proceeds from the Filters to the Capacitive Interface through the Analog-to-Digital (ADC) or the Digital-to-Analog (DAC) converters. These are over-sampling converters, to assure required conversion accuracy.

The Capacitive Interface provides isolation to the ALIS-D from the ALIS-A.

There are two pairs of general purpose I/Os. They operate when the ALIS-A is in the Ringing or Conversation states.

ALIS-D

At the ALIS-D, the tip/ring interfaces through two capacitors to the Caller-ID input pins.

The hardware filters perform interpolation and decimation for both Caller-ID and for data, before they proceed to the digital filter structure, which performs equalization, gain adjustment, impedance matching, and other DAA functions in accordance with the downloaded coefficient set.

Transmit and Receive data are transferred between the ALIS-D and the data pump through the Serial Data Interface.

The Control Interface allows external control of the ALIS features and provides transparent access to ALIS commands and signalling pins, so that pre-calculated coefficient sets can be downloaded from the system to the on-chip Coefficient RAM (CRAM) to program the filters.

There is one General Purpose Output pin that can be used, for example, to control the hook switch.

5.2 Data Path

The ALIS architecture is based on digital filters. In the next few diagrams, the data path through these filters is shown. Each filter corresponds to a particular system element. Some of the filters can be programmed by the user.

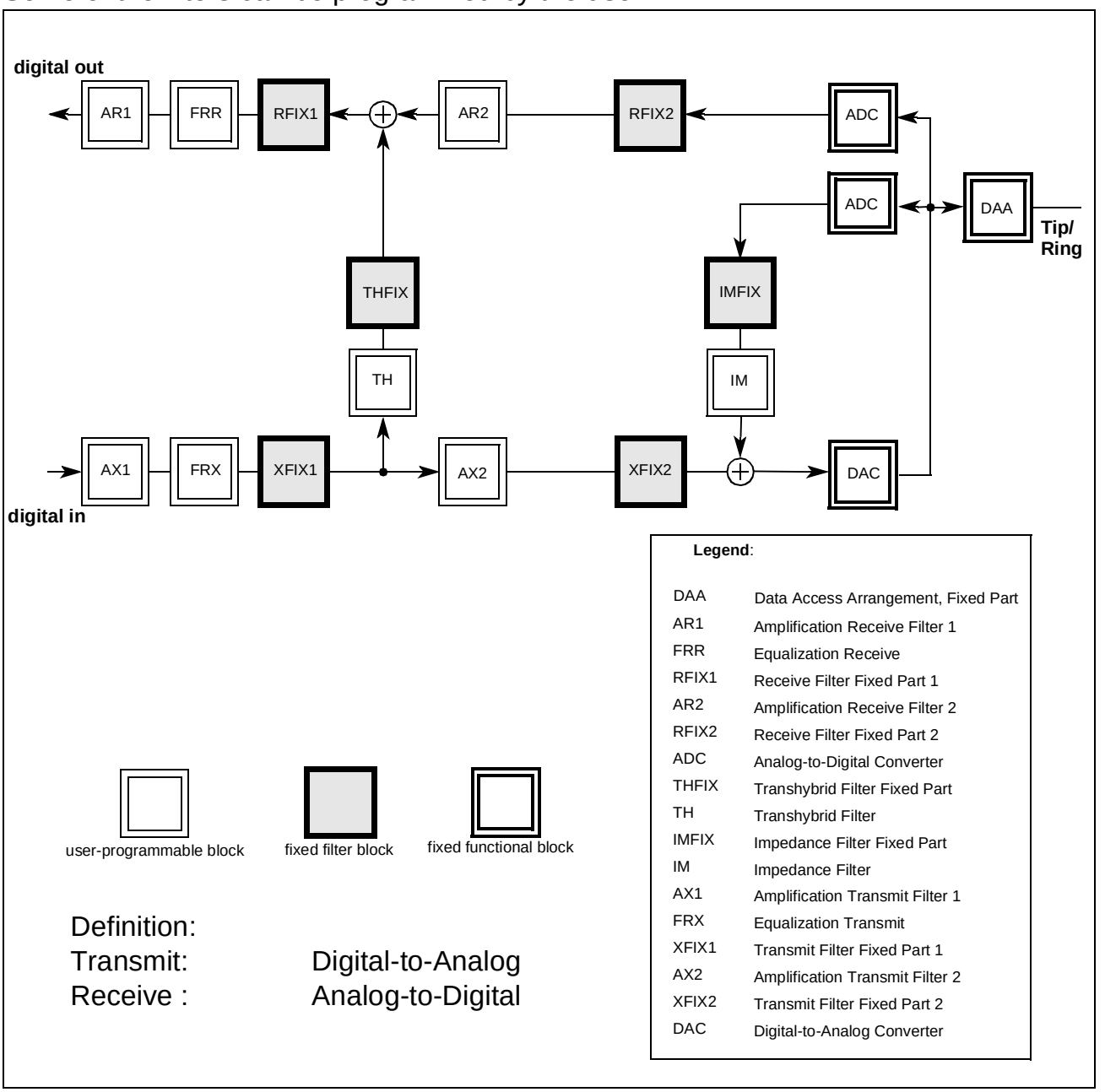


Figure 7 Modem Data Path

5.2.1 Receive Path

The analog signal proceeds from the tip/ring to the ALIS-A. It continues to an anti-aliasing pre-filter with an analog gain stage; the gain can be programmed to -3.5, 0.0, 2.5, or 6.0 dB. The Analog-to-Digital Converter (ADC) is a sigma-delta converter, which converts the signal to a 1-bit digital data stream. The signal is then passed to the ALIS-

D, where the first stage of down-sampling is performed in hardware, for better performance, in the digital filter RFIX2.

Subsequent stages of processing are done by microcode in the digital filter structure, to allow adaptability. Gain adjustment is provided in two stages, in AR1 and AR2. The total gain adjustment can be set by program in two ranges: from 14 to 24 dB, with step size 0.5 dB; and from -3 to 14 dB, with a step size between 0.02 and 0.05 dB.

Between them is a stage of decimation to reduce the sampling rate to the 8 kHz PCM rate, and a low-pass filter to band-limit the signal in accordance with ITU-T G.714 and ETSI (NET33) recommendations (in RFIX1); and a stage of equalization (in FRR).

Finally the signal is passed out to the Serial Data Interface (SDI).

The ALIS meets or exceeds all ITU and ETSI (NET33) recommendations on attenuation distortion and group delay.

5.2.2 Transmit Path

The digital input signal is received from the SDI. Most processing steps are done in microcode in the digital filter structure, allowing programmable flexibility.

There are two stages of gain adjustment, in AX1 and AX2. The total gain adjustment can be set by program in two ranges: from -14 to -24 dB, with step size 0.5 dB; and from 3 to -14 dB, with step size between 0.02 and 0.05 dB.

Between them is a stage of equalization (in FRX), a high-pass filter and a low-pass filter to band-limit the signal (in XFIX1); and a first stage of interpolation.

Further up-sampling is done in hardware (in XFIX2), and the 1-bit data stream is converted to analog in the DAC and smoothed by a post-filter. This is followed by an analog gain stage, which can be set to 3.5, 0.0, -2.5, or -6.0 dB, before the signal is converted to a two-wire signal.

There are also two independent tone generators which can insert tones into the Transmit path. They have adjustable frequencies, with default 2 kHz, and a programmable bandpass-filter to adapt the output for DTMF. When either tone generator is on, the data signal transmission is suppressed.

5.2.3 Loops

The ALIS implementation includes two loops. One is used to generate the AC-termination impedance (IM, IMFIX) and the other is used to perform proper hybrid balancing (TH, THFIX).

5.2.4 Test Features

There are three loopbacks on the ALIS-D to test interfaces:

- Host interface: loopback from the PCM interface (just inside the ALIS-D)
- Caller-ID interface: loopback from Caller-ID input to capacitive interface

- Capacitive interface: loopback through different parts of the capacitive interface

There are two loopbacks on the ALIS-A:

- Tip/ring interface: loopback from the tip/ring, before the ADC
- Codec: loopback from the tip/ring, after the codec

5.3 Ring and Caller-ID Signal Path

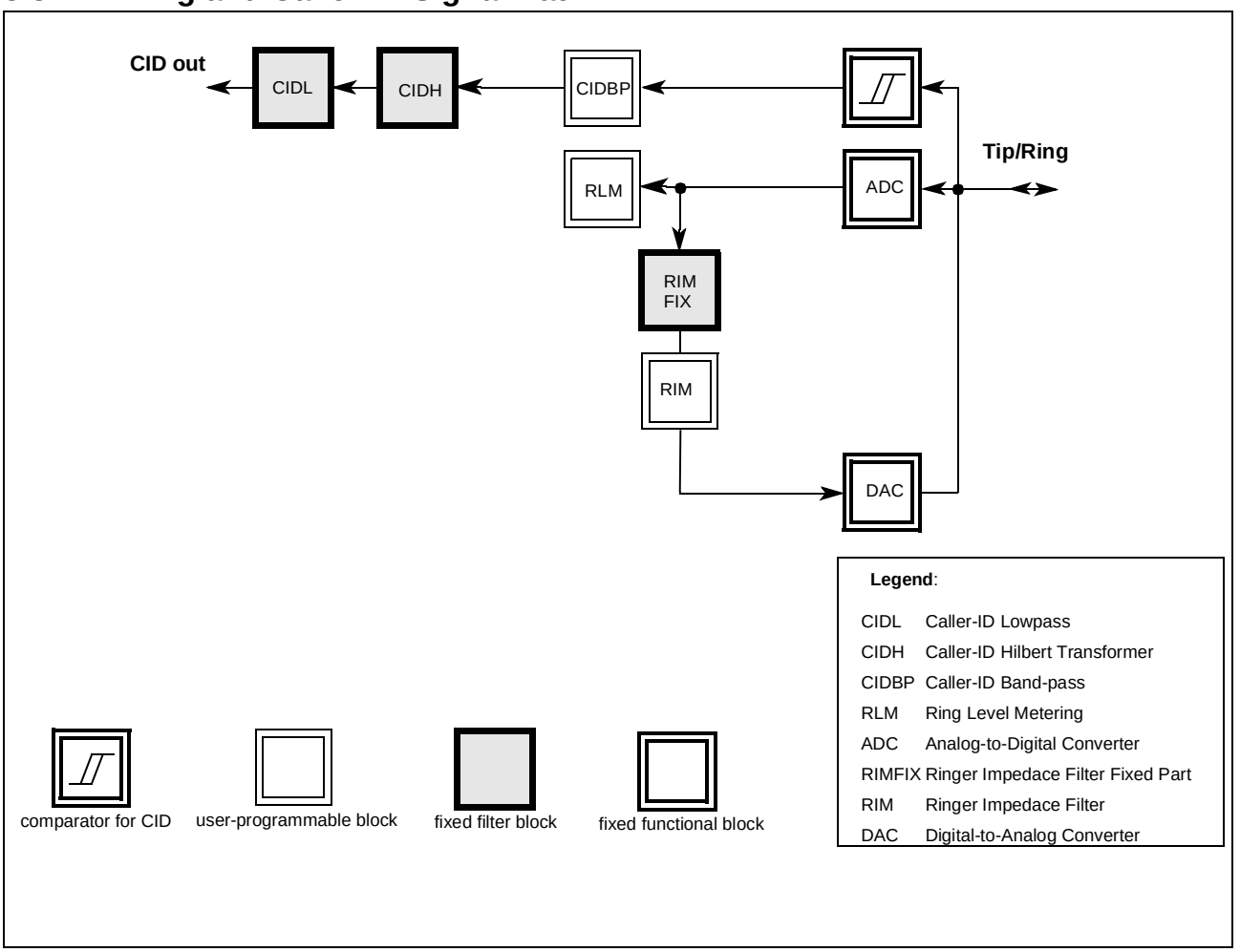


Figure 8 Ring Signal Path

These data paths operate only when the ALIS is in Ringing state.

5.3.1 Caller-ID (CID) Path

The Caller-ID receiver meets Bellcore specifications TR-NWT-000030 and SR-TSV-002476 for Caller-ID. In this service, the calling party's information (Calling Line Identification Presentation (CLIP)) is transmitted in the silent interval between the first and second ring. The ALIS receives and stores up to 4096 bits of the 1200 baud FSK signal. The de-coding scheme meets the Bell 202 and ITU-T V.23 specifications.

The FSK signal from the tip/ring bearing the caller information is converted to a 1-bit data stream by a comparator to minimize power consumption. Down-sampling is done in digital hardware filters. The signal undergoes band-pass filtering in CIDBP, Hilbert transforms in CIDH, and low-pass filtering in CIDL. The output CID-out is sampled at 1200 baud, and stored in the CID-RAM.

5.3.2 Ring-Level Metering (RLM) Path

The analog signal is converted to a 1-bit data stream in the ADC. After decimation in hardware filters, the remaining processing is done in the digital filter structure (in RLM): band-pass filtering to select the ringing frequency, and integration to determine if the amount of energy in-band has exceeded the threshold for a valid ring signal. The band-pass parameters and threshold are programmable.

5.3.3 Loops

There is one loop to generate the Ring-termination Impedance (RIM).

6 Interfaces Overview

6.1 Host Interface

The host interface consists of a serial µ-controller interface and a 16-bit Serial Data Interface. In the parallel operating mode, they connect separately to a µ-controller and to a data pump and require 8 pins. In time-multiplex (MUX) mode, a single port can be used to connect to a DSP with embedded µ-controller, requiring 5 pins.

6.2 Connection to the telephone line

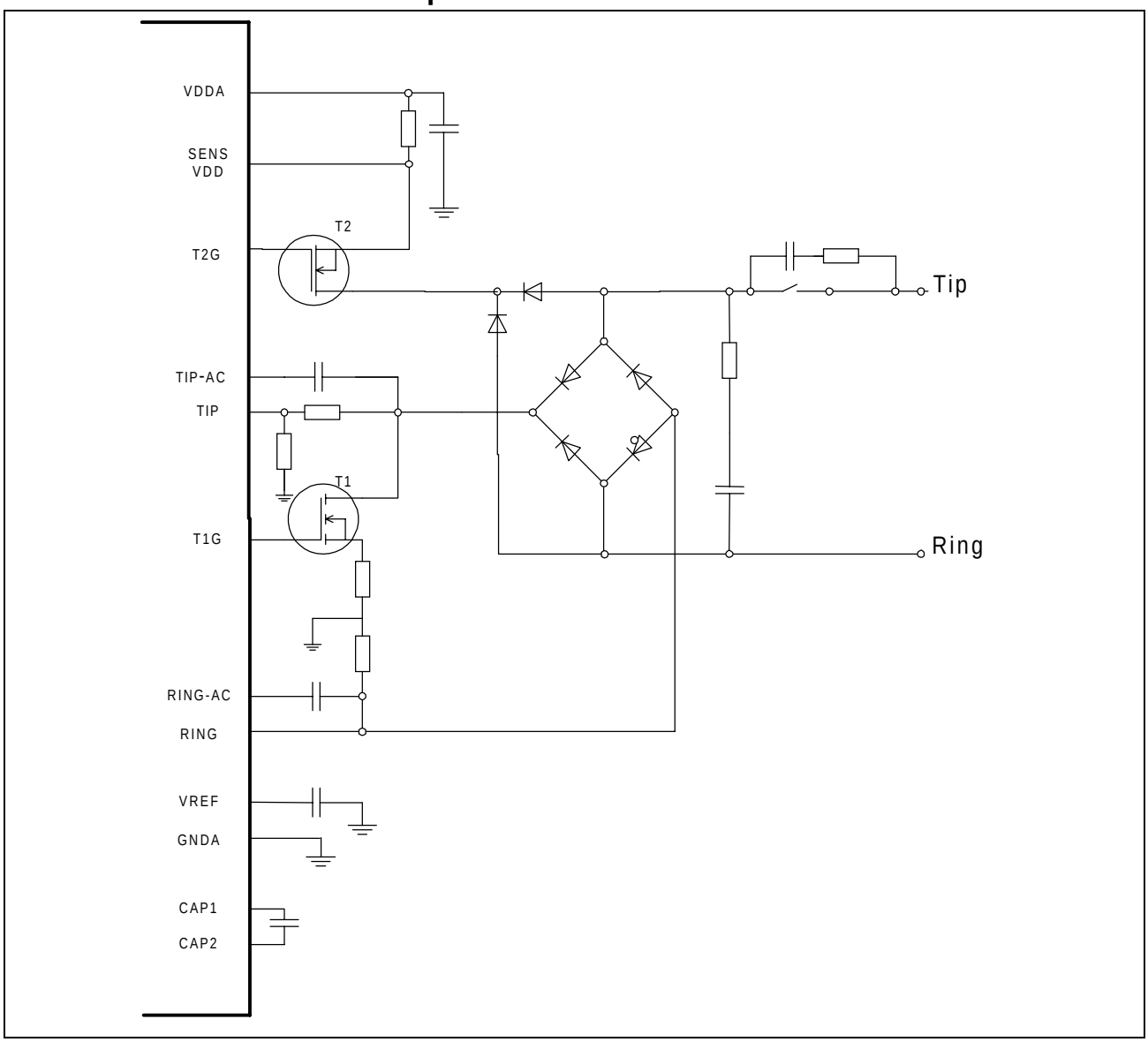


Figure 9 Connection of the ALIS-A to the Telephone Line

As shown in the figure, the ALIS-A requires a minimum of components to complete the DAA:

- Protection circuit: not shown.

- Bridge: these diodes must be Schottky diodes. Recommended: Dual Schottky diode SIEMENS BAT 240A.

- Resistors for current sensing.

- Capacitors for AC coupling and VDD buffering.

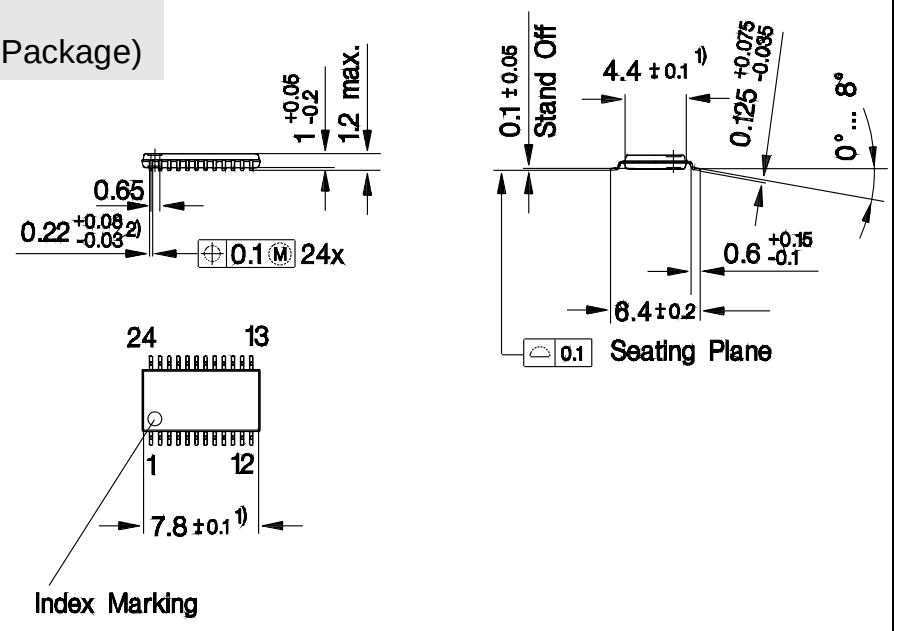
- Two transistors (T1, T2) to handle the line current. T2 must be of depletion type, in order to deal with start-up. Recommended transistors: T1: SIEMENS BSP 88; T2: SIEMENS BSP 129.

- Components for EMC protection: not shown, as they depend on the board layout.

The ALIS-D can optionally be connected to the tip/ring to provide Caller-ID functions. The CID circuit requires two capacitors and four resistors.

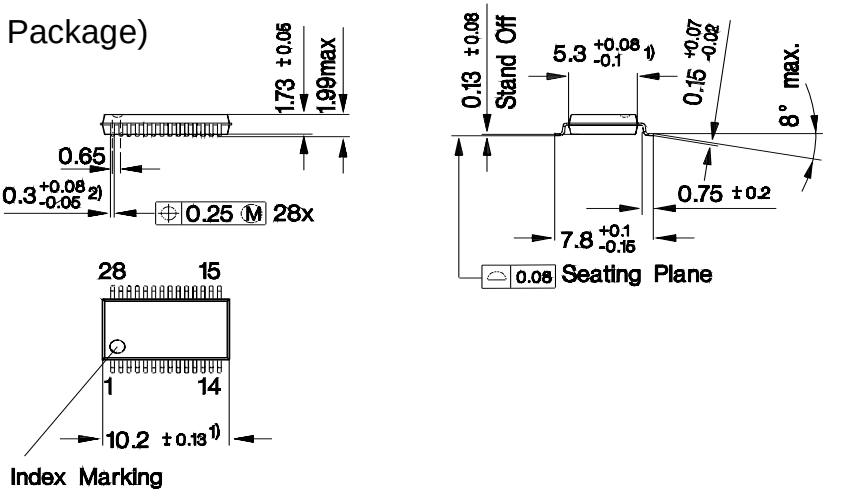
7 Package Outlines

P-TSSOP24 PSB 4595
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

P-SSOP28 PSB 4596
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm