SIEMENS

ICs for Communications

Analog Line Interface Solution ALIS
PSB 4595 Version 2.0
PSB 4596 Version 2.1

User's Manual 04.97 Preliminary Data

T4595-XV20-P1-7600

ALIS **Revision History:** **Current Version: 04.97**		
Previous Version:		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)

Edition 04.97

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
HL CT

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1 Overview

The two chip solution PSB 4595 and PSB 4596 forms the complete frontend of a modem or fax machine. This Analog Line Interface Solution (ALIS) consists of DAA, codec and hybrid and bridges the gap between phone line and data pump. The analog PSB 4595 is fabricated in low-power 0.8 µm BiCMOS technology, the digital PSB 4596 in 0.8 µm CMOS technology. The ALIS concept is a fully programmable modem frontend which allows one single design for the worldwide market:

- Adaptation to specific countries and applications is achieved by downloading appropriate coefficient sets.
- Isolation is achieved by a digital capacitive interface, without a transformer; this makes the ALIS especially suitable for PCMCIA modem design.
- Using an advanced digital filter concept in combination with the programmable electronic DAA the ALIS provides both: excellent transmission performance and high adaptability. This second-generation digital filter concept also allows a maximum of independence between the different filter blocks. This performance makes ALIS suitable for V.34+ and V.PCM modem applications.

A minimum number of external components is required to complete the functionality of the ALIS. The internal precision is based on a very accurate bandgap reference. The frequency behaviour is determined mostly by digital filters which exhibit no fluctuations. As a result of the ADC and DAC concepts linearity is limited only by second-order parasitic effects.

The ALIS chipset can be easily adapted and connected to various modem data pumps or to host based modem solutions. The flexible digital interface of ALIS allows easy programming via the modem data pump or a controller.

Siemens offers a range of reference and evaluation tools for the ALIS chipset. For appropriate tools please contact your next Siemens representative.

SIEMENS

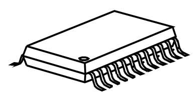
Analog Line Interface Solution
ALIS

PSB 4595
PSB 4596

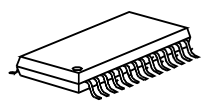
CMOS

1.1 Features

- ALIS substitutes Data Access Arrangement (DAA), Codec and hybrid
- Ring Detection: Level, Frequency and Cadence
- Caller ID: Detection, Decoding and Storage
- Programmable to the different Country Requirements
- Programmable DC characteristics
- ALIS supports V.34+ and V.PCM
- ALIS meets ETS 300 001 and FCC requirements
- Isolation by digital capacitive interface
- Analog part supplied from the Tip/Ring line by integrated voltage regulator
- High performance Analog to Digital and Digital to Analog Conversion
- DSP based solution to adapt the transmission behaviour especially for
  - AC impedance matching
  - transhybrid balancing
  - frequency response
  - gain
- Advanced test capabilities:
  - digital loops
  - analog loops
- High pass in receive to suppress disturbances from the mains (50/60 Hz)
- Isolated control pins for general purpose use



P-TSSOP24



P-SSOP28

- Advanced low power 0.8µm analog BICMOS technology for ALIS analog and 0.8µm CMOS technology for ALIS digital
- Two Chip solution: P-TSSOP24 and P-SSOP28 package are PCMCIA conform

Type	Ordering Code	Package
PSB 4595 V2.0	Q67106-H6754	P-TSSOP24
PSB 4596 V2.1	Q67106-H6755	P-SSOP28

1.2 Logic Symbol

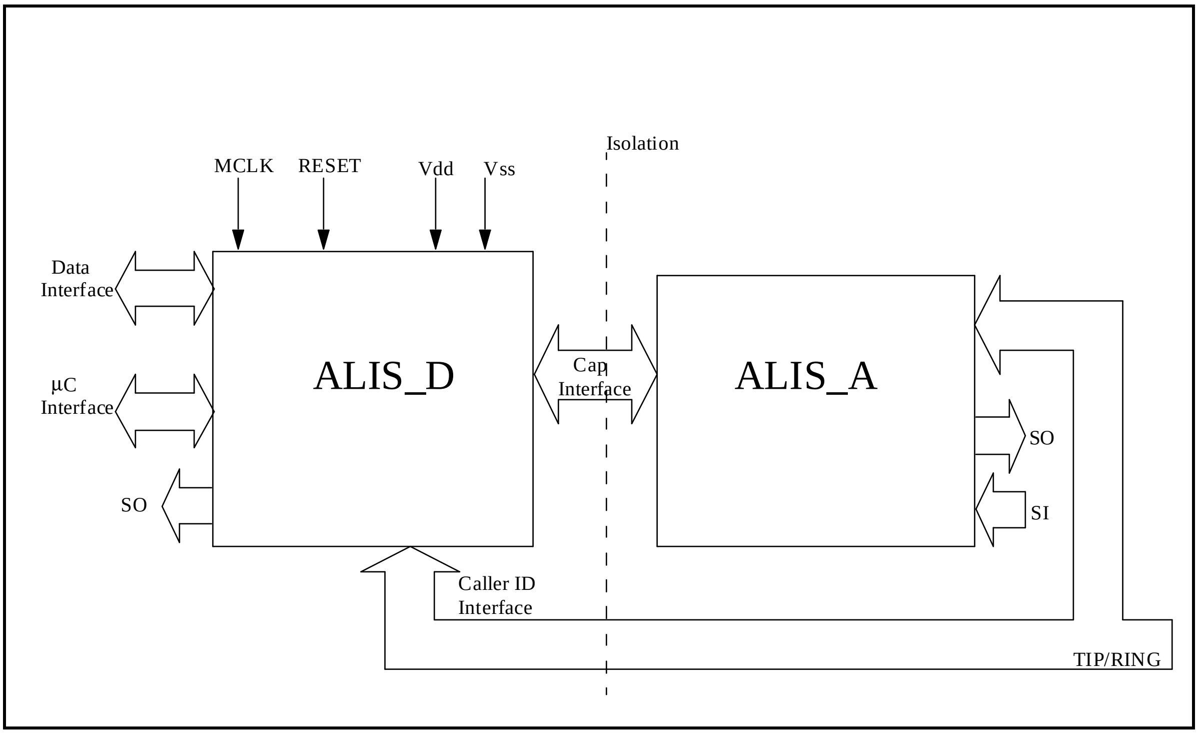


Figure 1: Logic Symbol of the ALIS Chipset

1.3 Pin Configuration

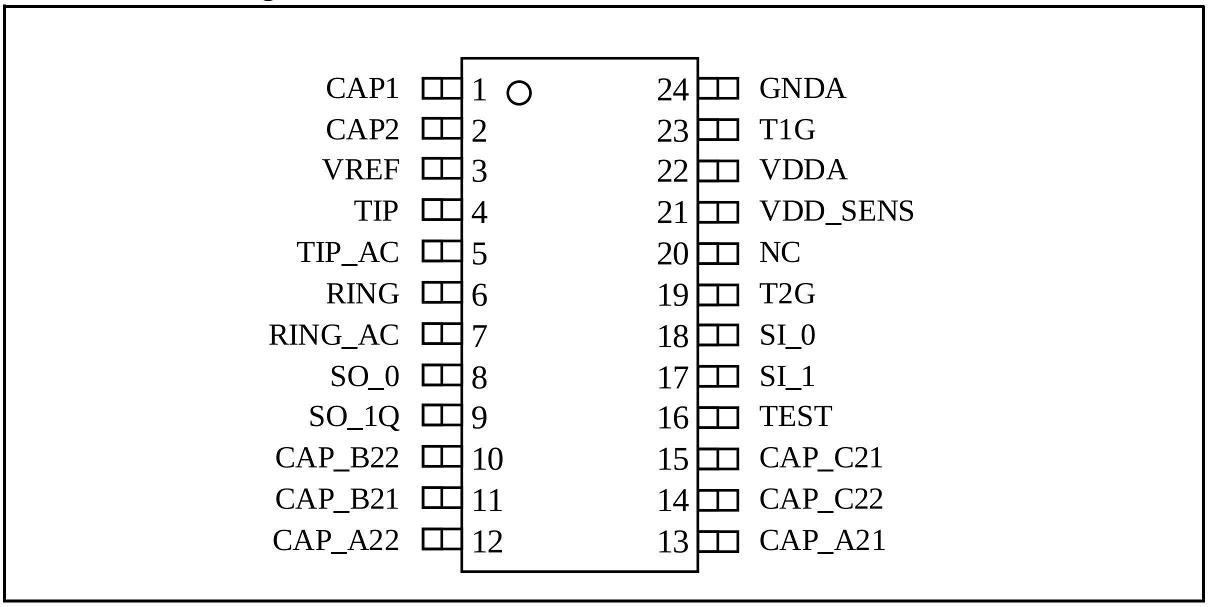


Figure 2: Pin Configuration of ALIS _A (top view)

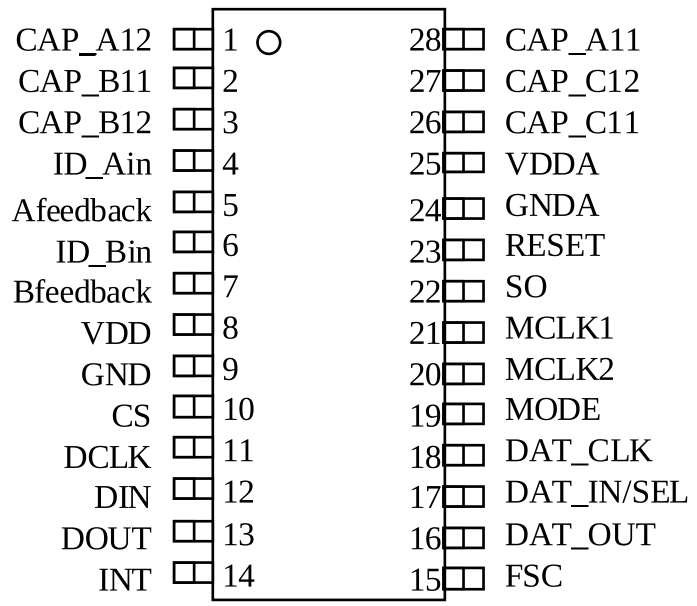


Figure 3: Pin Configuration of ALIS _D (top view)

2 Pin Definition and Functions

2.1 ALIS_A PSB 4595

Pin No.	Symbol	Function	Descriptions
22	VDDA	Power	Programmable supply for the circuitry
24	GNDA	Power	Analog ground: All signals are referred to this pin
4	TIP	I	TIP ac+dc sense input
5	TIP_AC	I	TIP ac sense input
6	RING	I	RING ac+dc sense input
7	RING_AC	I	RING ac sense input
23	T1G	O	Gate for external transistor T1 (ac/dc control)
19	T2G	O	Gate for external transistor T2 (VDDA control)
21	VDD_SENS	I	VDDA sense input
3	VREF	I/O	Reference voltage: Must be connected to an external Capacitance with more than 10 nF (typ. 15 nF) to GNDA
1	CAP1	I/O	Pin for external capacitor with more than 1 µF for DC filtering to pin Cap2
2	CAP2	I/O	See Cap1
18	SI_0	I	Auxiliary input pin 0
17	SI_1	I	Auxiliary input pin 1
8	SO_0	O	Auxiliary output pin 0
9	SO_1Q	O	Auxiliary output pin 1
16	TEST	I	Must be connected permanently to GNDA
13	CAP_A21	I	Must be connected by a capacitance with more than 5pF to CAP_A11.
12	CAP_A22	I	Must be connected by a capacitance with more than 5pF to CAP_A12.
11	CAP_B21	O	Must be connected by a capacitance with more than 5pF to CAP_B11.
10	CAP_B22	O	Must be connected by a capacitance with more than 5pF to CAP_B12.

Pin No.	Symbol	Function	Descriptions
15	CAP_C21	I	Must be connected by a capacitance with more than 5pF to CAP_C11.
14	CAP_C22	I	Must be connected by a capacitance with more than 5pF to CAP_C12.

Table 1: ALIS_A pin definition

2.2 ALIS_D PSB 4596

Pin No.	Symbol	Function	Description
8	VDD	Power	+5 Volt supply for the digital circuitry
9	GND	Power	Ground digital: All signals are referred to this pin
25	VDDA	Power	+5 Volt supply for the analog circuitry
24	GNDA	Power	Ground analog: All analog signals are referred to this pin
21	MCLK1	I	Master clock1: One pin of a crystal or ceramic resonator is connected. This pin can also be driven from an external clocking source of 16.384 MHz, synchronous to FSC
20	MCLK2	O	Master clock2: Other pin of a crystal or ceramic resonator is connected. When MCLK1 is driven by an external clock this pin should be left open
23	RESET	I	Reset input: Forces the device to the default mode (low active)
15	FSC	BI	As input: Frame synchronisation clock, 8 kHz, identifies the beginning of the frame, FSC must be synchronous to DATCLK As Output: Indicates the beginning of a new frame
17	DAT_IN / SEL	I	Data-interface: Receive Data from the DSP, the data is received in 16 bit bursts every 125 µs. Interface selection pin in mux mode.
16	DAT_OUT	O	Data-interface: Transmit Data to the DSP, the data is transmitted in 16 bit bursts every 125 µs
18	DAT_CLK	I	Data clock 128 to 1024 kHz: Determines the rate at which Data is shifted into or out of the Data Interface
10	CS	I	µ–controller interface: Chip select enable to read or write data, active low
11	DCLK	I	µ–controller interface: Clock, maximum clock rate 1024 kHz

Pin No.	Symbol	Function	Description
12	DIN	I	µ–controller interface: Input data
13	DOUT	TRI	µ–controller interface: DOUT is high 'Z' if no data is transmitted
14	INT	O	µ–controller interface: Interrupt output pin
19	MODE	I	Interface Mode pin (parallel or mux mode)
4	ID_Ain	I	Input for Caller ID comparator (connection to TIP)
6	ID_Bin	I	Input for Caller ID comparator (connection to RING)
5	Afeedback	O	Feedback for Caller ID comparator
7	Bfeedback	O	Feedback for Caller ID comparator
28	CAP_A11	O	Must be connected by a capacitance with more than 5pF to CAP_A21.[1)]
1	CAP_A12	O	Must be connected by a capacitance with more than 5pF to CAP_A22.
2	CAP_B11	I	Must be connected by a capacitance with more than 5pF to CAP_B21.
3	CAP_B12	I	Must be connected by a capacitance with more than 5pF to CAP_B22.
26	CAP_C11	O	Must be connected by a capacitance with more than 5pF to CAP_C21.
27	CAP_C12	O	Must be connected by a capacitance with more than 5pF to CAP_C22.
22	SO	O	Auxiliary output pin [2)]

1) For a detailed description of the cap interface see “ALIS Cap interface” on page 83

2) can be used to control the hook switch

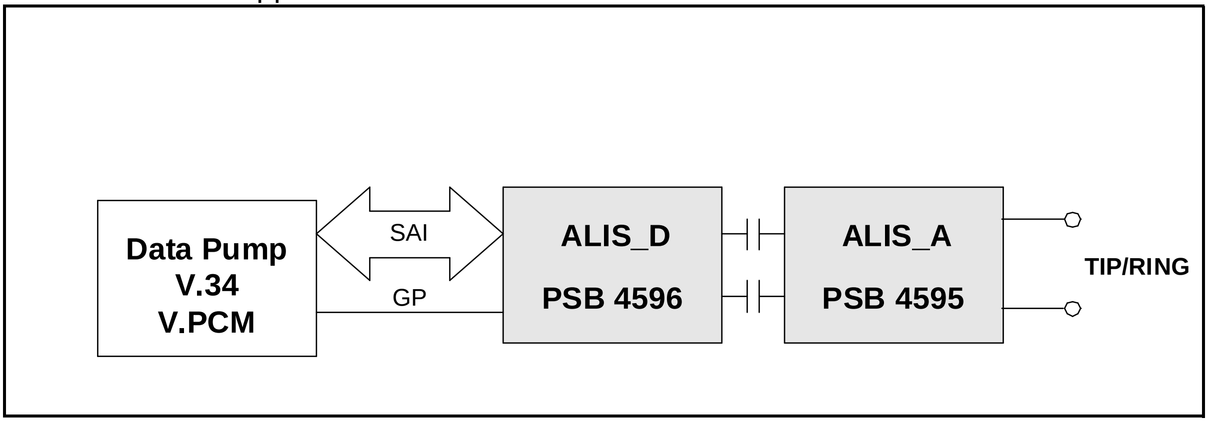
Table 2: ALIS_D pin definition

3 System Integration

ALIS can be used in different modem applications to connect the data pump to the TIP/RING wire.

3.1 ALIS with V.34 Chipset

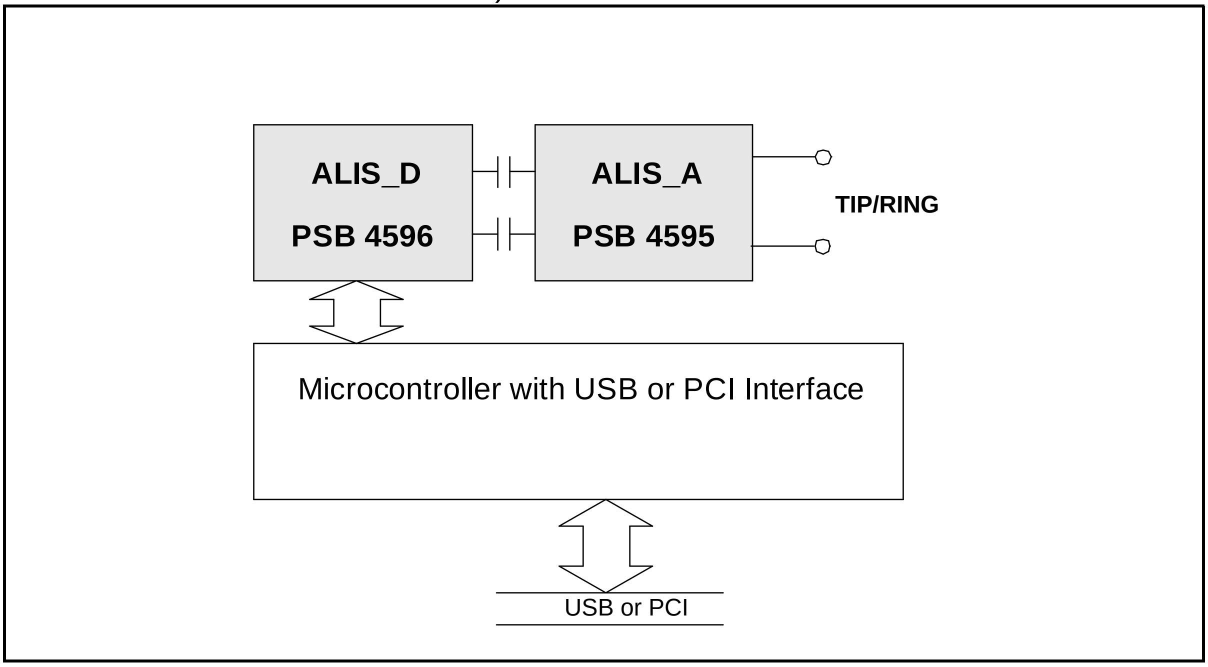
In combination with a V.34 chipset ALIS is an optimal solution for standard V.34 and V.PCM modems applications.



Note: SAI Serial Audio Interface
GP General Purpose I/O pin's

3.2 ALIS with Software Modem

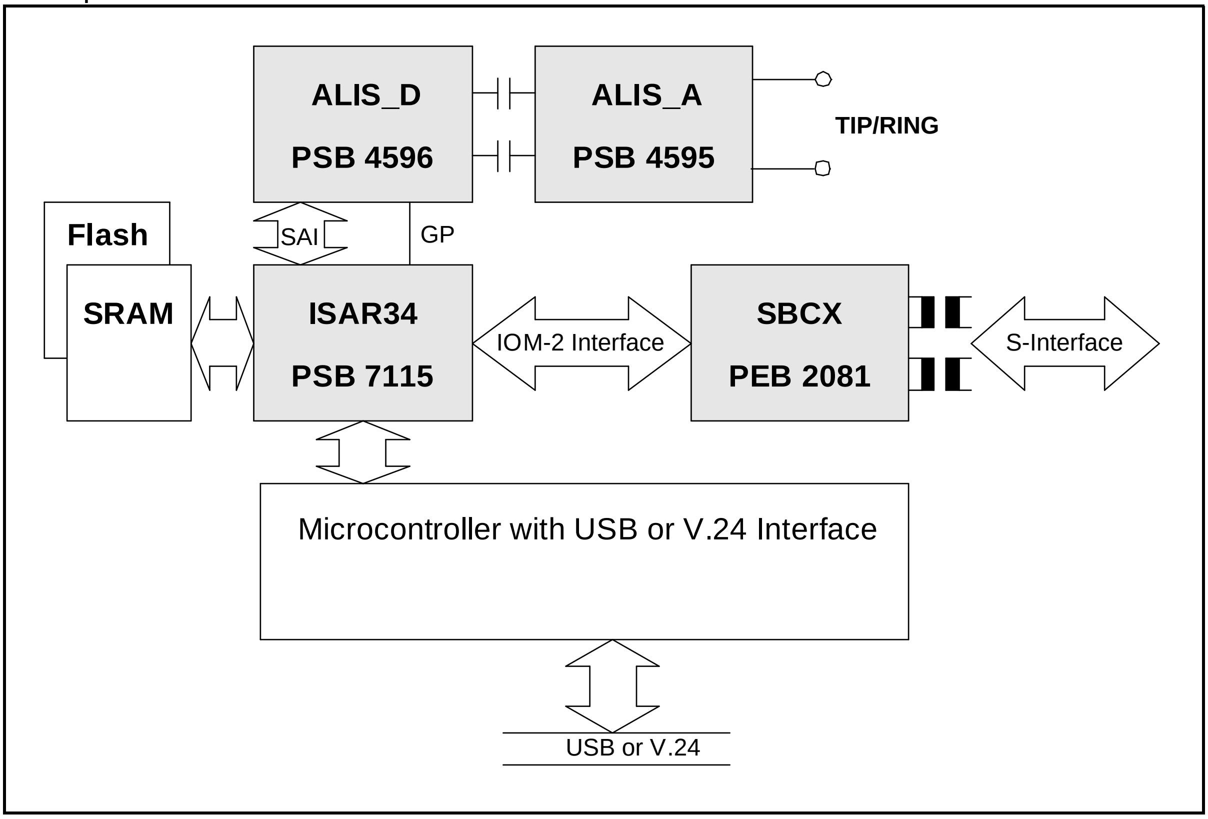
ALIS also supports software modems where V.34 runs on the host computer (e.g. in combination with an USB Controller)



3.3 Dual Mode Modem

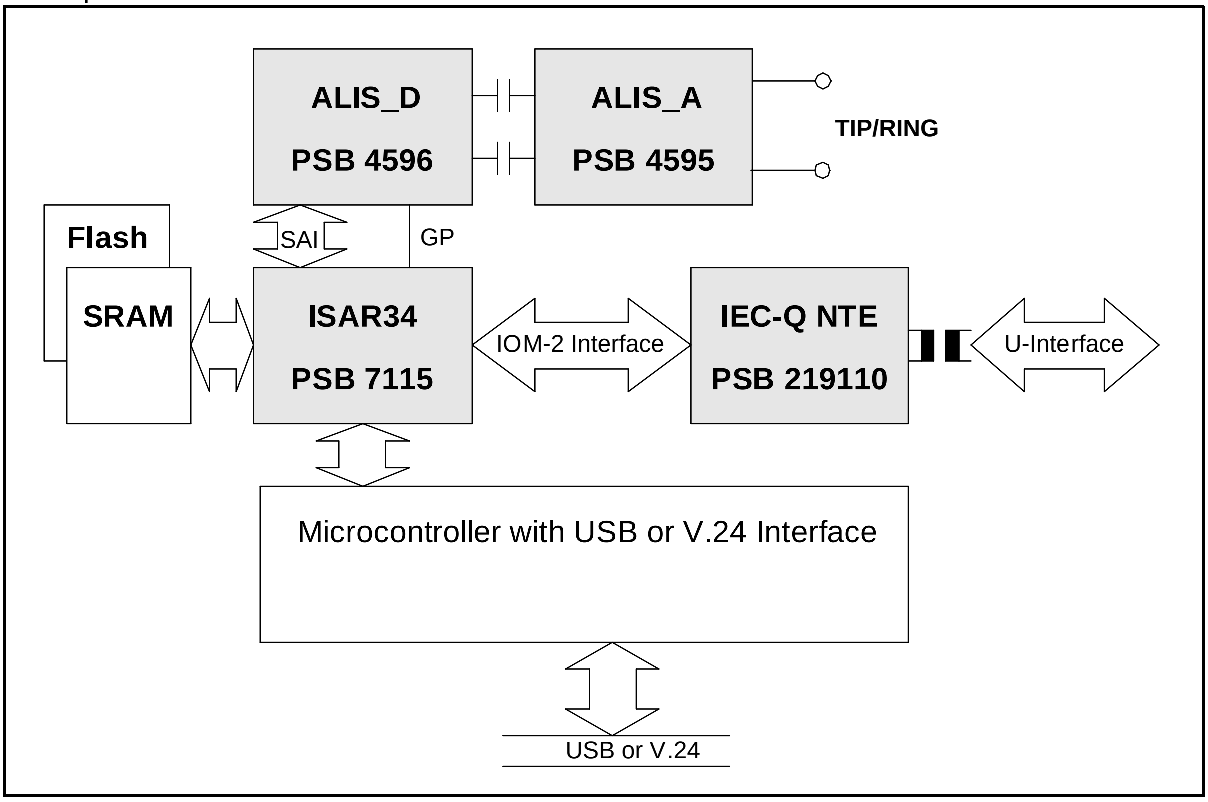
In combination with the SIEMENS ISDN chipset ALIS supports dual mode modems to connect either to the TIP/RING line or to a S or a U-interface for ISDN applications.

Example for a dual mode modem with an S-interface



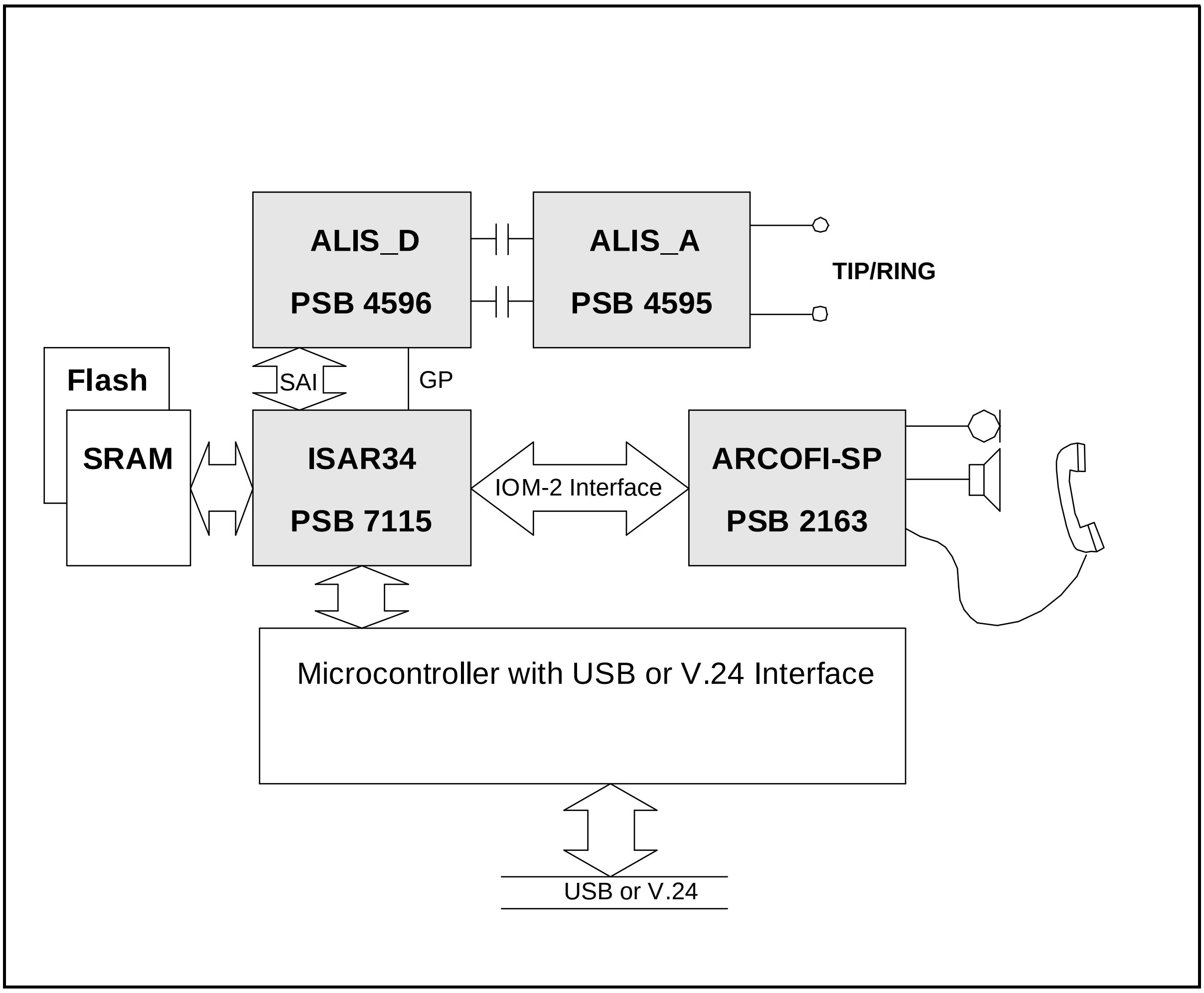
ISAR34 Enhanced data access controller (PSB 7115)
SBCX S/T Bus Interface Circuit Extended (PEB 2081)

Example for a dual mode modem with an U-interface



ISAR34 Enhanced data access controller (PSB 7115)
IEC-Q NTE ISDN Echo Cancellation Circuit for Network Termination and Terminals

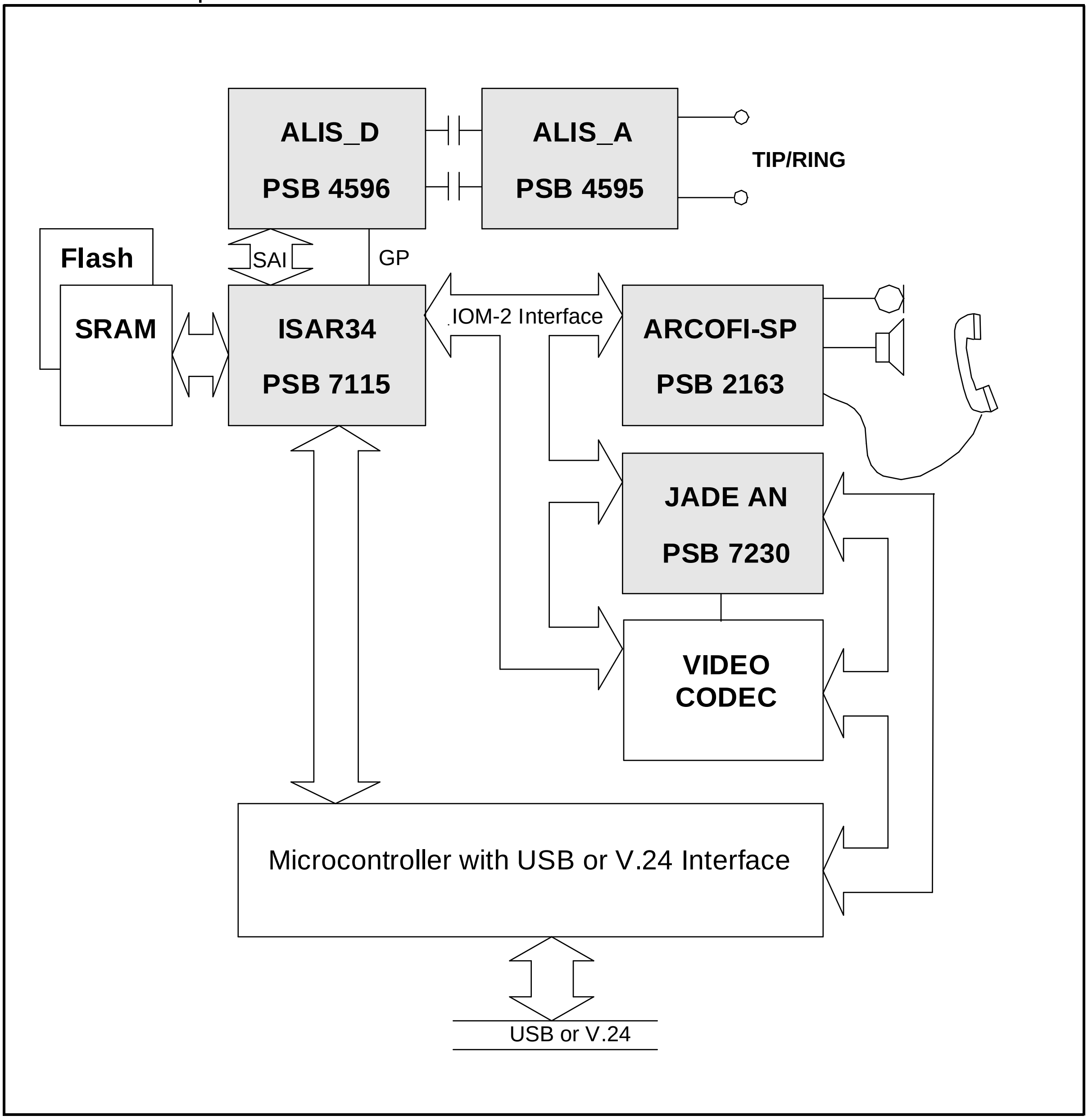
3.4 Modem with Speakerphone



ARCOFI-(SP) Audio Ringing Codec (PSB 2160, PSB 2163, PSB 2165, PSB 2168)
ISAR34 Enhanced data access controller (PSB 7115)

3.5 Analog Videophone

The picture below shows a system solution for an analog videophone application using a SIEMENS chipset.



ARCOFI-(SP) Audio Ringing Codec (PSB 2160, PSB 2163, PSB 2165, PSB 2168)

ISAR34 Enhanced data access controller (PSB 7115)

JADE Joint Audio Decoder Encoder (PSB 7230, PSB 7238)

4 ALIS Realization

The ALIS chip set replaces all the major parts of traditional frontend for modem solutions.The circuit consists of two major parts, a DSP based Codec and an electronic DAA. Advanced features like ring detection, pulse dialing and caller-ID are integrated on-chip. To minimize power consumption additional operating modes like Sleep Mode or Ringing Mode are implemented.

4.1 ALIS Block Diagram

The analog front end (ALIS_A) is connected to the line via TIP/RING. The programmable supply voltage for ALIS_A is generated from the line by the Vdd-Control. Two/four wire transformation is realized in the Hybrid. Analog antialiasing Prefilters (PREFI) and smoothing Postfilters (POFI) are included for signal conditioning. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) assure the required conversion accuracy. The ADC and DAC are connected to the Digital Signal Processor (DSP) on the digital part (ALIS_D) via a dedicated capacitive interface which also provides the required isolation to the line. Special Hardware Filters perform filtering functions like interpolation and decimation. The DSP handles all the necessary algorithms, e.g., bandpass filtering, sample rate conversion, ring detection, caller ID decoding etc. Also, all programmable filters and functions are controlled and processed by the DSP. The control interface allows external control of the ALIS features and provides transparent access to ALIS commands and signalling pins. Thus precalculated sets of coefficients can be downloaded from the system to the on-chip Coefficient RAM (CRAM) to program the filters. Transmit and receive data is transferred from and to the data pump via the data interface.

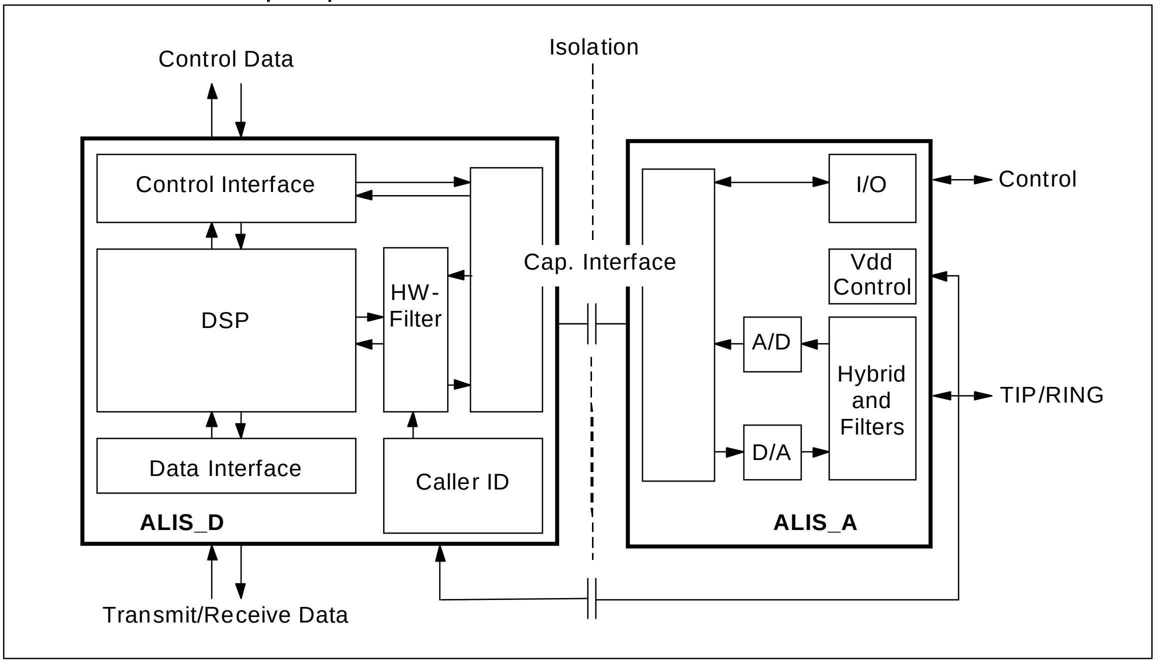


Figure 4: ALIS Block Diagram

4.2 ALIS AC Signal Flow Graph

This second-generation digital filter concept also allows a maximum of independence between the different filter blocks. Each filter block has a one-to-one correspondence with a particular network element.

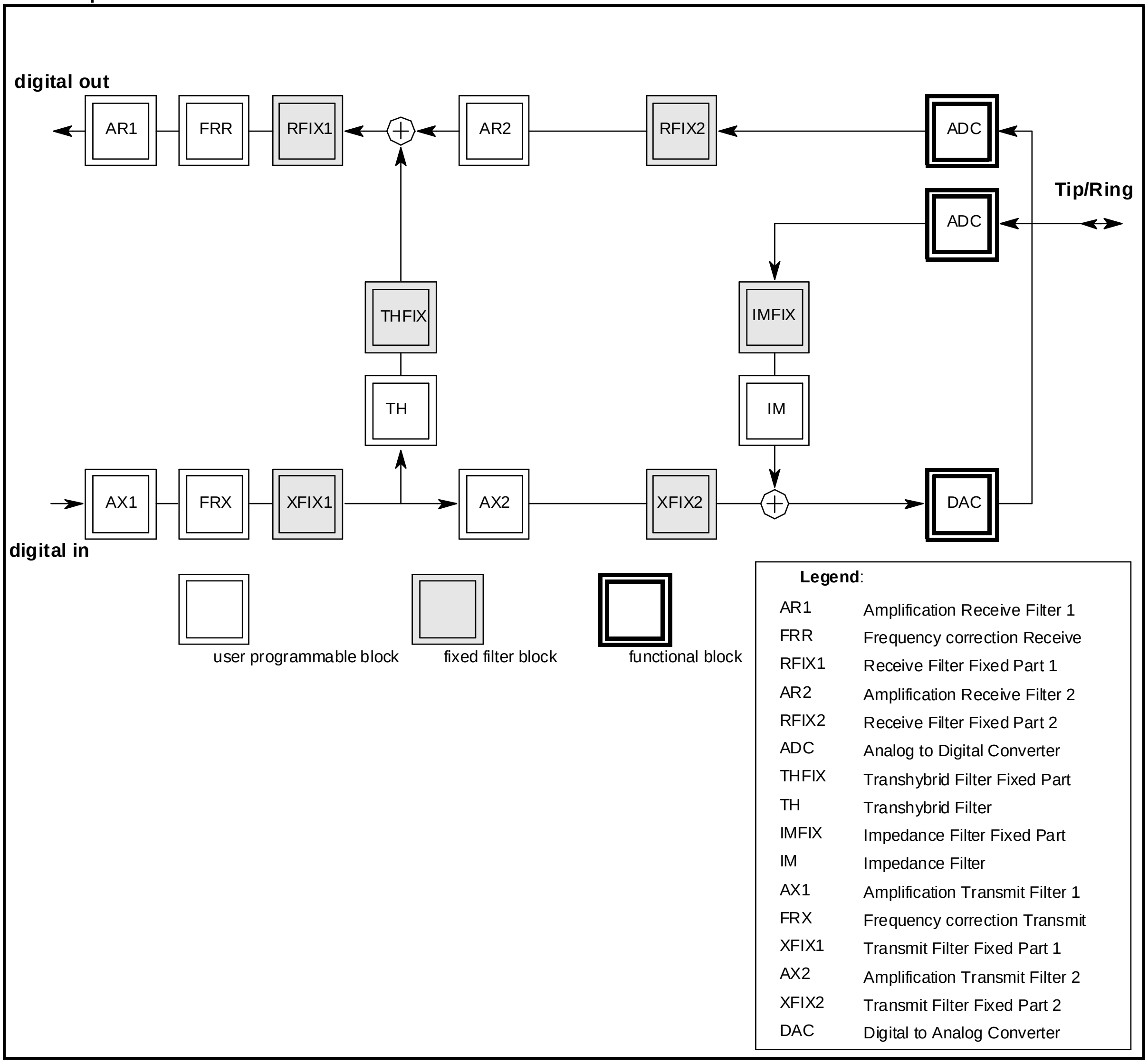


Figure 5: AC Signal flow graph

Definition:

Transmit - path: D/A path

Receive - path: A/D path

4.2.1 Receive Path

After passing the DAA and a simple antialiasing Prefilter with an analog gain stage the voice signal is converted to a 1-bit digital data stream in the Sigma-Delta-converter. The first downsampling steps are performed in fast running digital hardware filters. The following steps are implemented in micro-code which is executed by the central DSP. This allows an easy and flexible programming of many parameters. At the end the fully processed signal is transferred to the data interface.

4.2.2 Transmit Path

The digital input signal is received via the data interface. Low-pass filtering, gain correction and frequency response correction are implemented in micro-code and executed by the DSP. The upsampling interpolation is then performed by fast hardware structures to reduce the DSP load. The upsampled 1-bit data stream is converted to an analog equivalent which is smoothed by a Postfilter (POFI) and converted to a 2 wire signal in the DAA.

4.2.3 Loops

The ALIS implementation includes two loops. One is used to generate the AC-termination impedance (IM) and the other is used to perform proper hybrid balancing (TH). A simple additional path IM (from the receive to the transmit path) supports the impedance matching function.

4.2.4 Test Features

There are several analog and digital test loops implemented in ALIS. For test purposes it is possible to short-cut the receive and the transmit path at two different points.

4.3 ALIS Ring and CID Signal Flow Graph

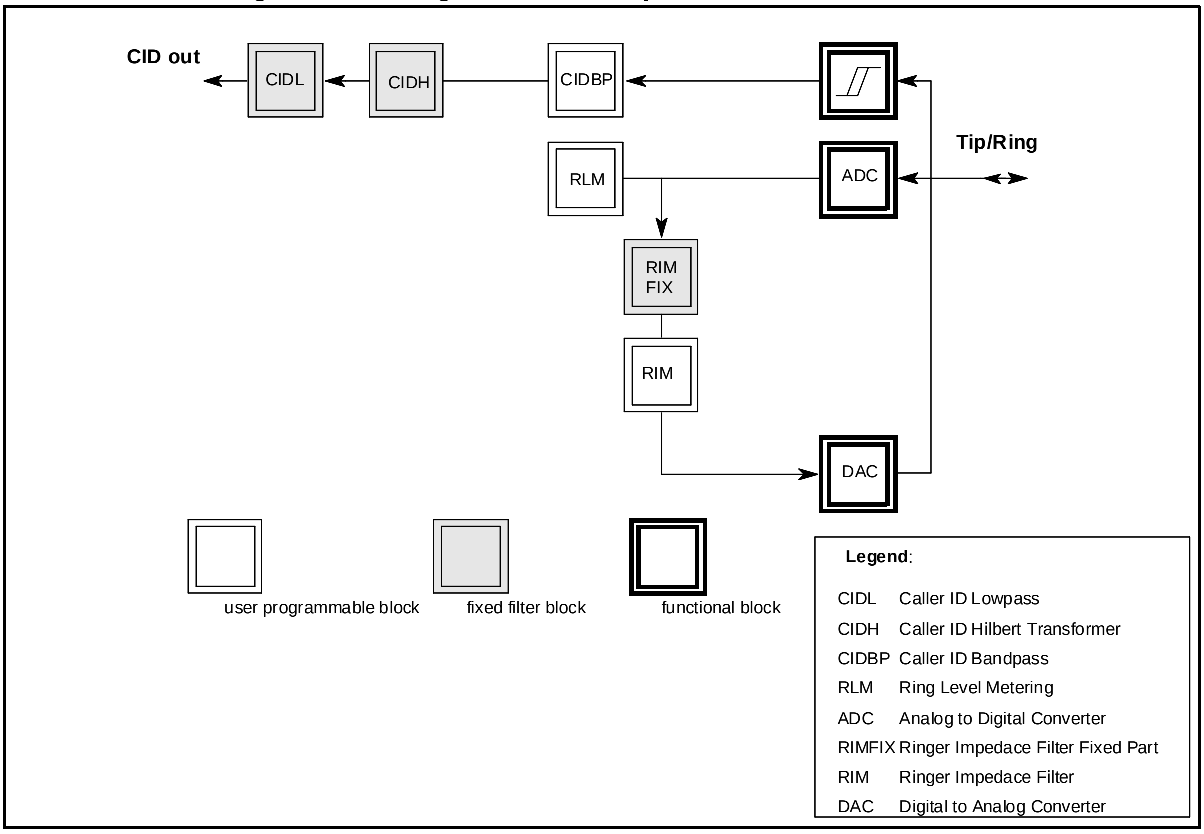


Figure 6: Ring Signal flow graph

4.3.1 Caller ID (CID) Path

The FSK-Signal which contains the caller information is converted to a 1-bit data stream by a comparator to minimize power consumption. Downsampling steps are performed in fast running digital hardware filters. To decode the caller ID band-pass filtering, hilbert-transforming and other functions are executed by the DSP.

4.3.2 Ring Level-Metering (RLM) Path

Ring detection is realized in this path. The digital input is band-pass filtered, integrated and compared to a threshold to determine if a ring signal occurred. Threshold and band-pass filter are programmable. The result of this operation can be monitored by reading the RMR bit. See “CR1 Configuration Register 1 (dialing)” on page 38

4.3.3 Loops

There is one loop to generate the Ring-termination Impedance (RIM).

5 Configurations Overview

5.1 Connection to the telephone line

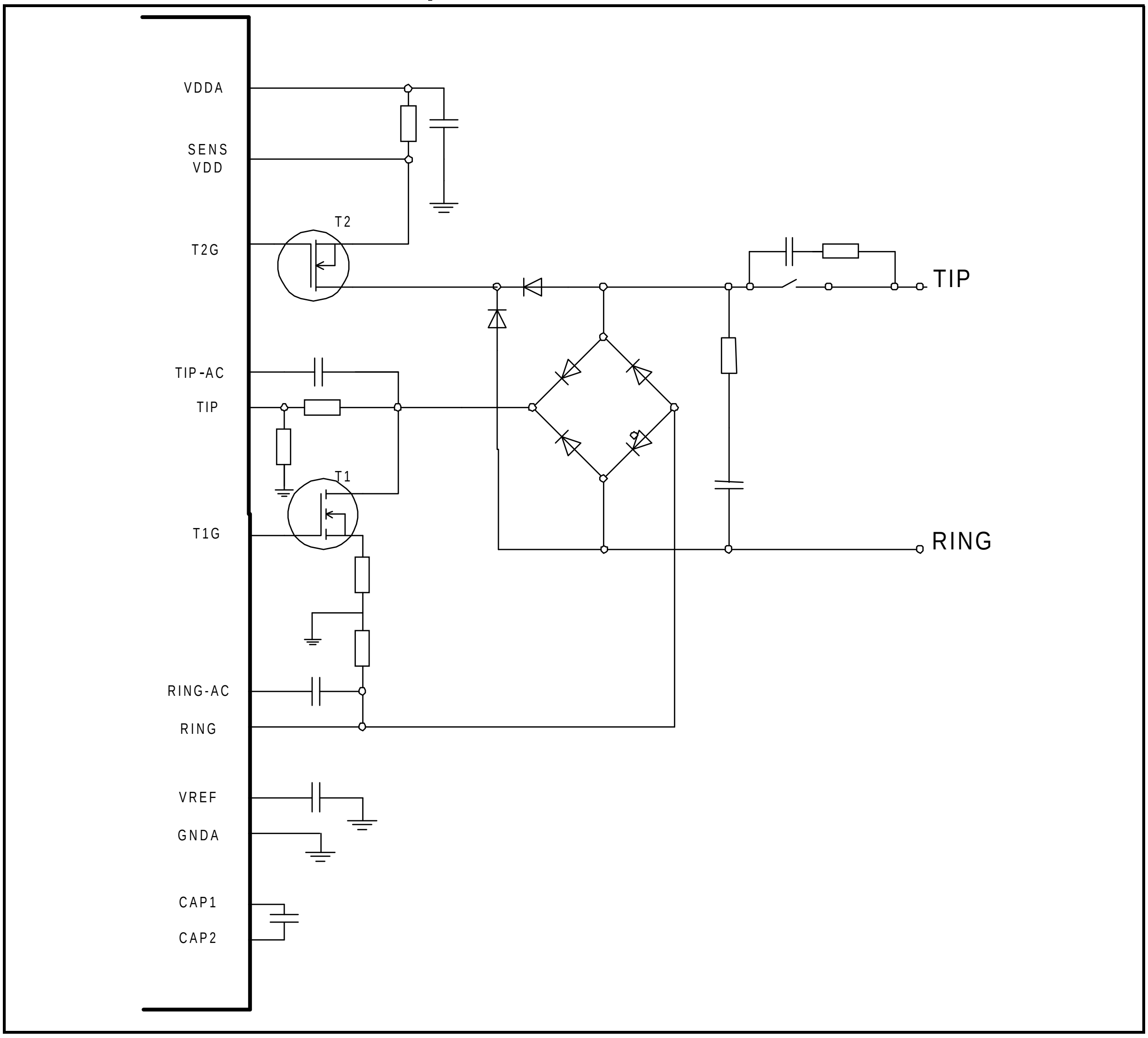


Figure 7: Connection to the telephone line

Recommended Transistors:

T1: BSP 88

T2: BSP 129

In addition to the protection circuit and the bridge, two transistors (T1, T2) to handle the line currents, a few resistors for current measurement and some capacitors for AC coupling and VDD buffering are necessary. For start-up reasons the transistor T2 has to be of depletion type. External components for EMC protection are not shown, as they strongly depend on the board layout.

5.2 Host Interface

The host interface consists of a serial µ-controller interface and a 16-bit linear data interface. They are used to connect the ALIS either to a µ*-controller* and or to a data pump. The two serial interfaces can be accessed on two parallel ports or in time-multiplex (MUX) mode on one single port.

5.2.1 The µ-Controller Interface

The internal configuration registers, the auxiliary ports, and the Coefficient RAM (CRAM) of the ALIS are programmable via the serial µ-controller interface. The µ-controller interface consists of 4 pins:

CS:	Chip select, for enabling interface (active low)
DCLK:	Clock, 1 kHz to 1024 kHz
DIN:	Data input
DOUT:	Data output

CS is used to start a serial access to the ALIS registers and the Coefficient RAM. Following a falling edge of CS the first eight bits received on DIN specify the command. Subsequent data bytes (number depends on command) are stored in the selected configuration registers or the selected part of the coefficient RAM.
Serial interface specification: 8 bit, no parity, no start/stop bit. Every command must begin with a falling edge of CS.

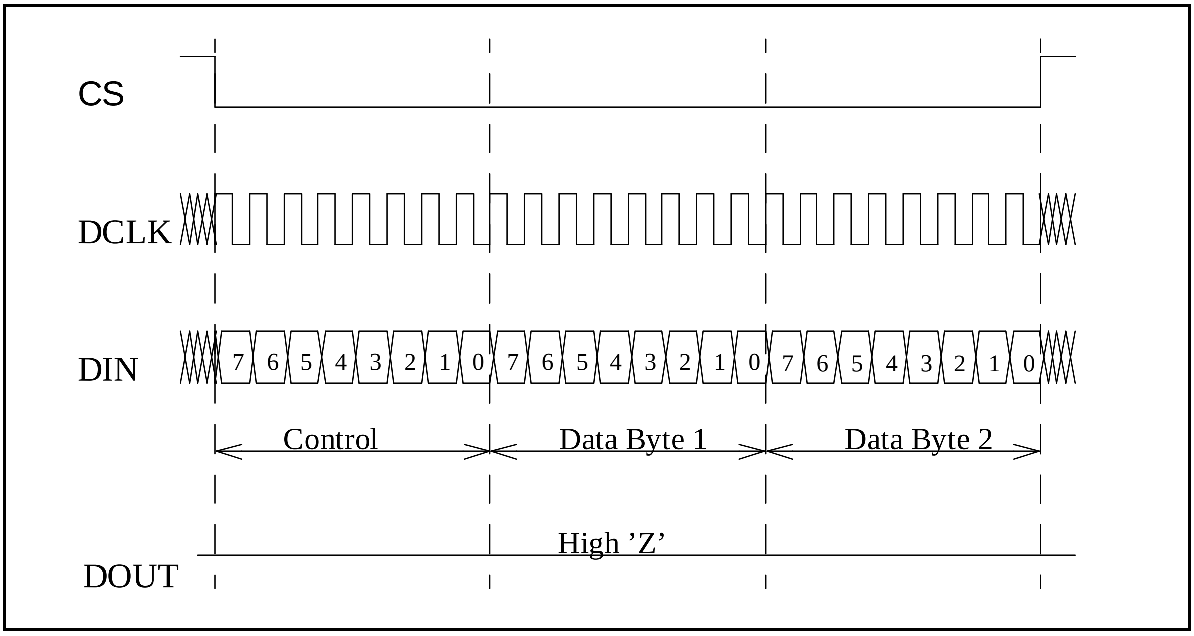


Figure 8: Example for a write access, with two data bytes transferred

If the first eight bits received via DIN specify a read-command, the ALIS will start to response via DOUT with its specific identification byte. The number of specified data bytes within the command (contents of configuration registers, or contents of the CRAM) will follow on DOUT.

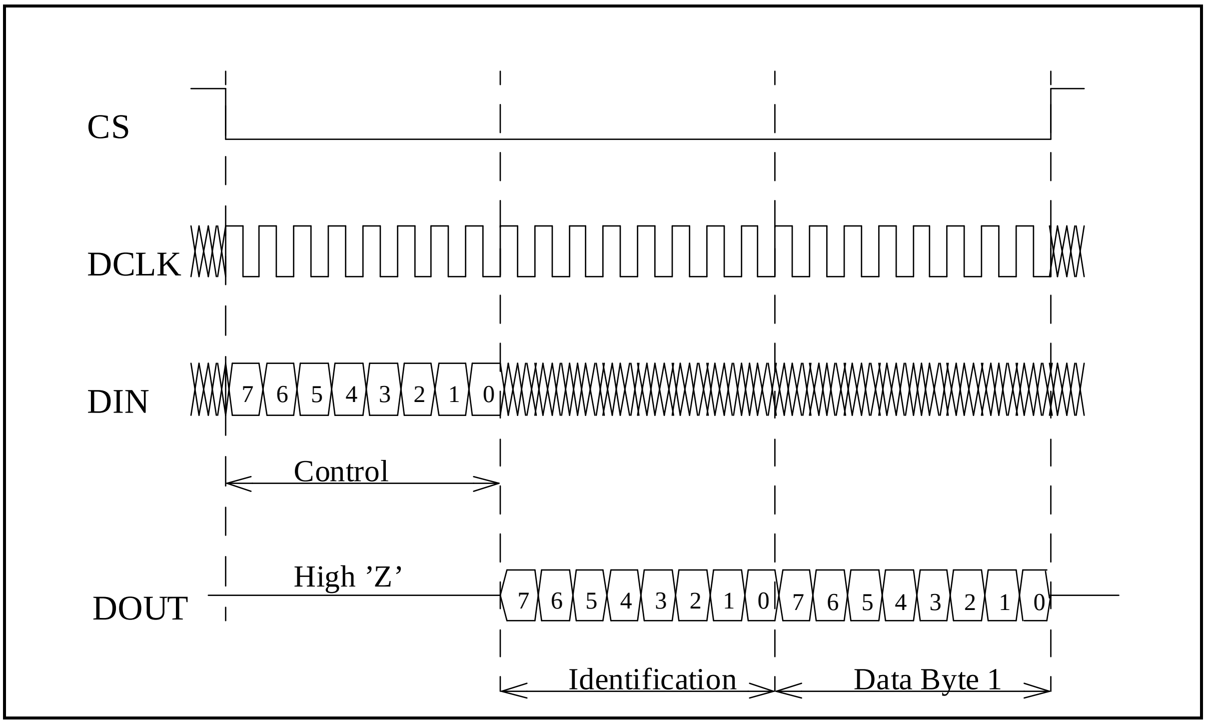


Figure 9: Example for a read access, with one data byte transferred via DOUT

The data transfer is synchronized by DCLK. DIN is latched at the falling edge of DCLK, while DOUT changes with the rising edge of DCLK. During execution of a command which is followed by output data (read command), the device will not accept any new command via DIN. The data transfer sequence can be interrupted by setting CS to high.

To reduce the number of connections to the µ-Processor DIN and DOUT may be strapped together to a bidirectional datapin.

5.2.2 The Data Interface

A serial data-interface is used for the transfer of voice data. The data-interface consists of 5 pins:

DAT_CLK:	Clock, 128 kHz to 1024 kHz
FSC:	Frame Synchronisation Clock, 8 kHz
DAT_IN:	Transmit Data input
DAT_OUT:	Receive Data output

The Frame Sync (FSC) pulse identifies the beginning of a receive and a transmit frame. DAT_CLK synchronizes the data transfer on DAT_IN and DAT_OUT. The data bytes are serialized to 16 bit width and MSB first. The rising edge indicates the start of the bit, while the falling edge is used to latch the contents of the received data.

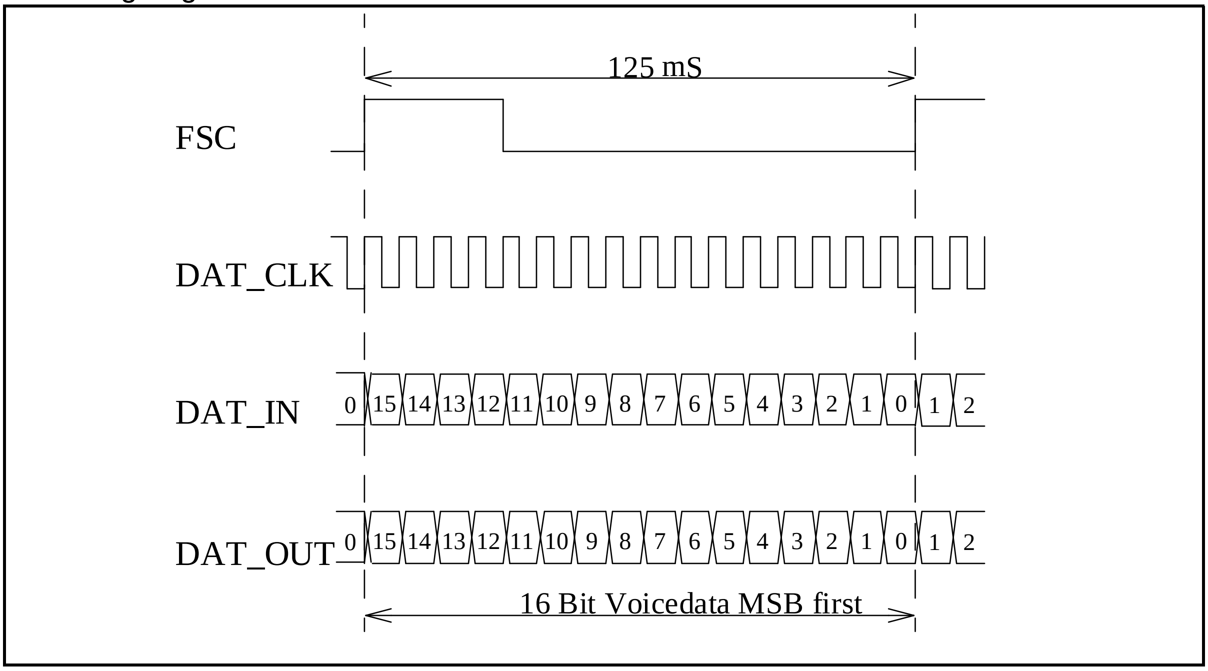


Figure 10: Example for a clock rate of 128 kb/s

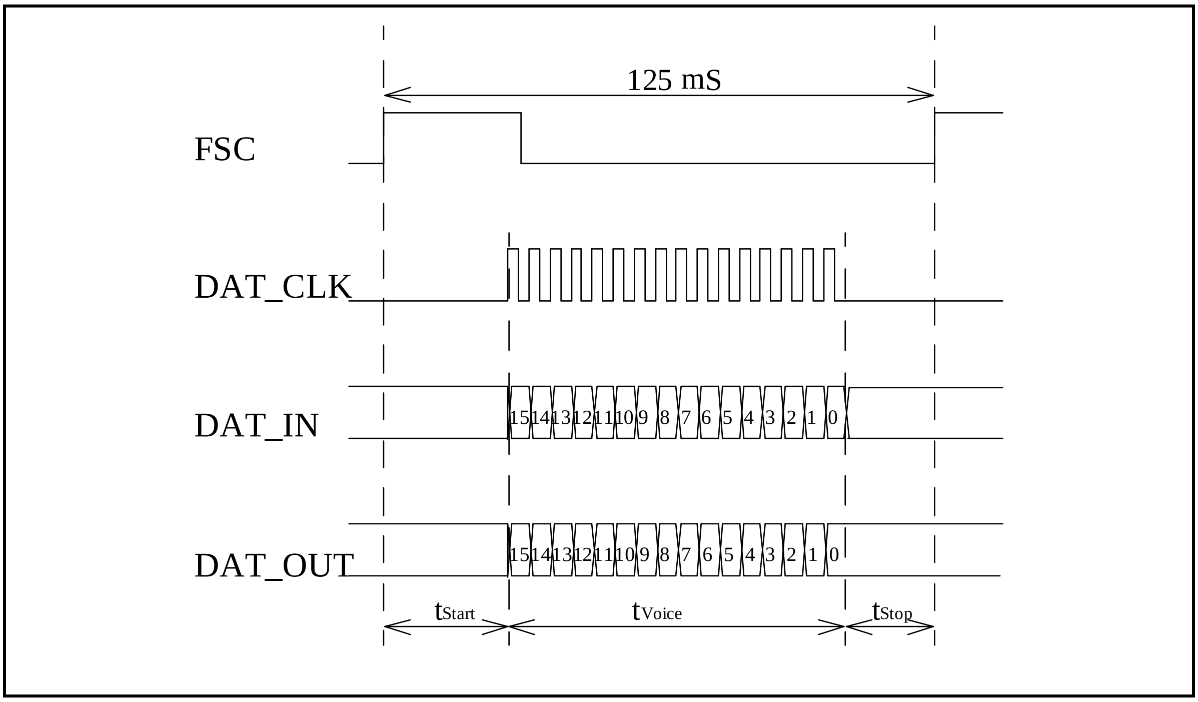


Figure 11: Example for clock rate higher than 128 kb/s
The data package must stay within the frame, t_{Start} > 0 and t_{Stop} > 0.

The FSC signal can be generated externally by the host, or by ALIS.

5.2.3 Interface Modes

5.2.3.1 Parallel Mode

By connecting the MODE pin to GND the µC and the data interface are accessed via two parallel ports.

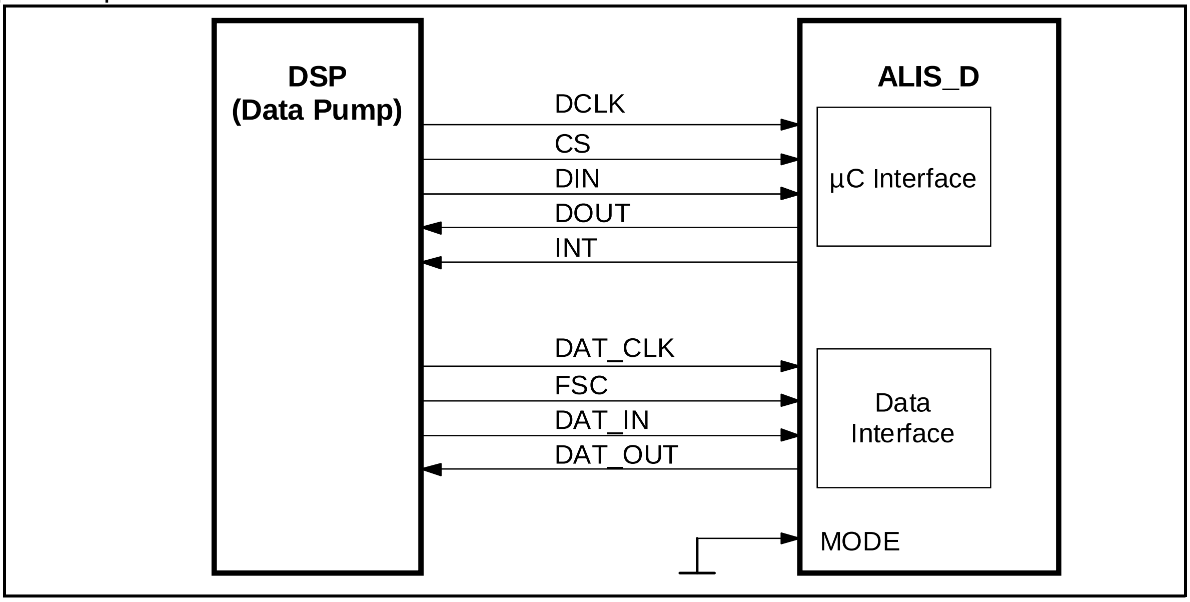


Figure 12: Host interface in parallel mode, FSC as input

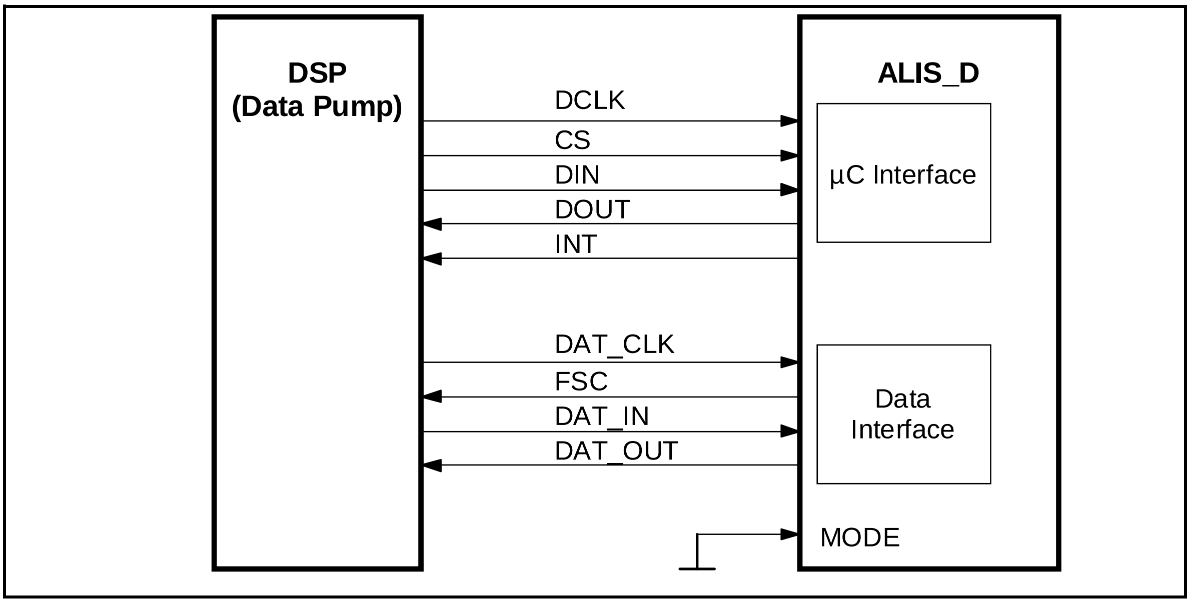


Figure 13: Host interface in parallel mode, FSC as output

5.2.3.2 Multiplex Mode

By connecting the MODE pin to VDD the two interfaces are time multiplexed on one single port. The selection between the interfaces is done by the DAT_IN/SEL pin.

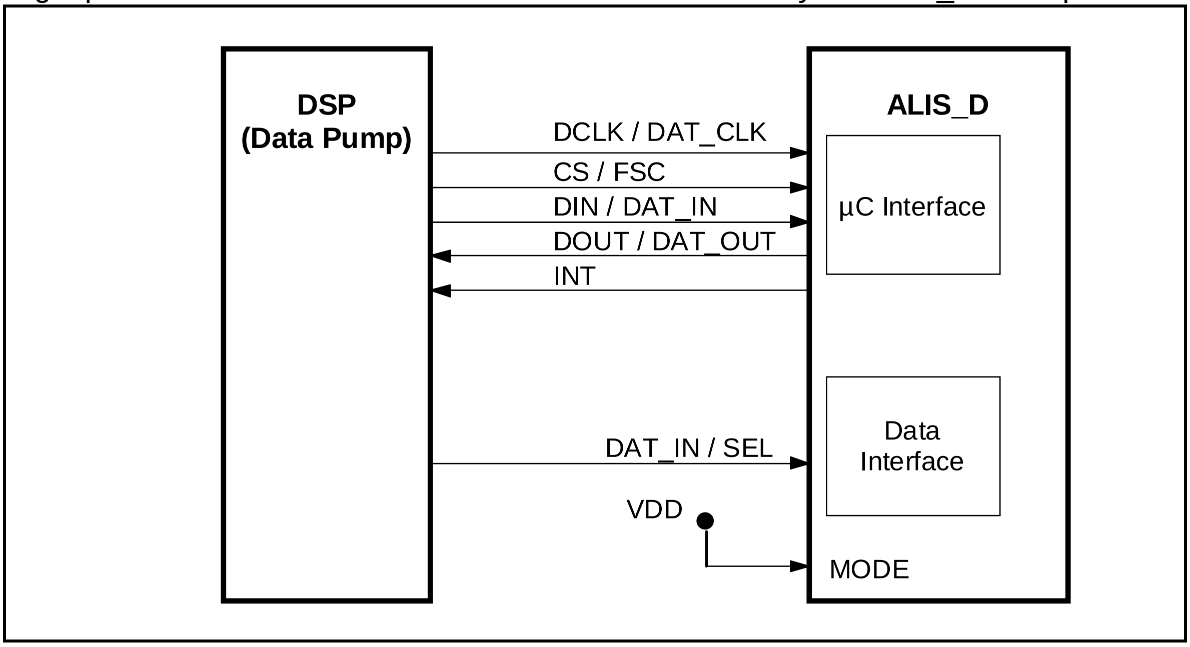


Figure 14: Host interface in MUX mode, FSC as input

DAT_IN / SEL = 0	
PIN No	**Function**
11	DCLK
10	CS
12	DIN
13	DOUT

DAT_IN / SEL = 1	
PIN No	**Function**
11	DAT_CLK
10	FSC
12	DAT_IN
13	DAT_OUT

Table 3: Pin definition in MUX mode, FSC as input

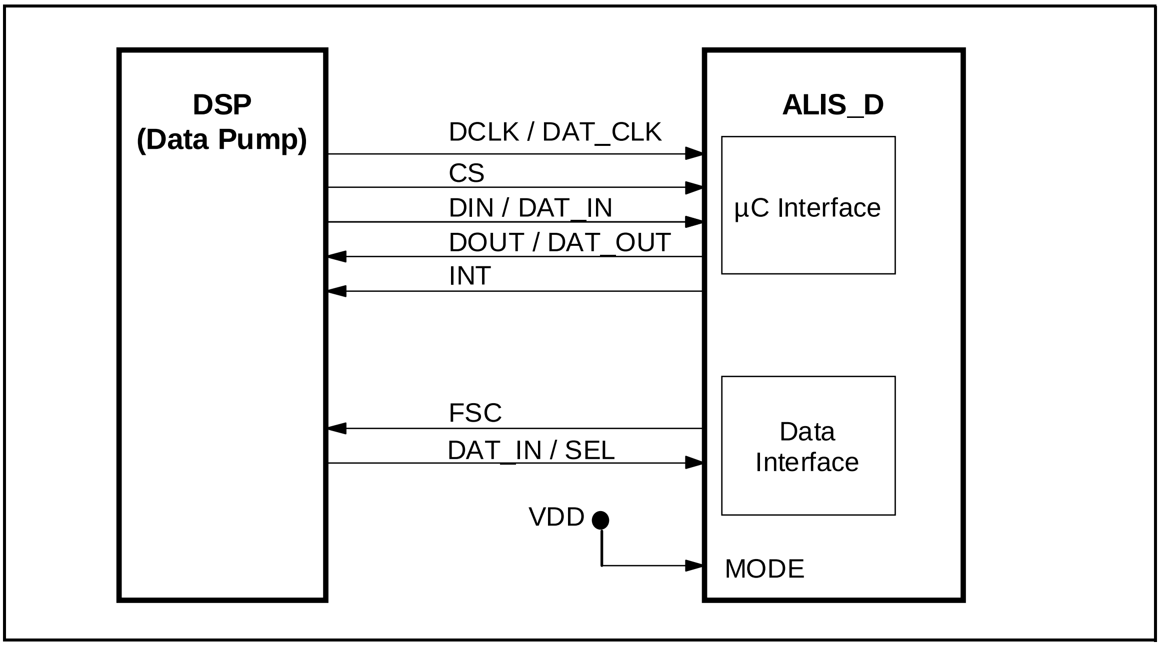


Figure 15: Host interface in MUX mode, FSC as output

DAT_IN / SEL = 0	
PIN No	**Function**
11	DCLK
10	CS
12	DIN
13	DOUT
15	FSC (output)

DAT_IN / SEL = 1	
PIN No	**Function**
11	DAT_CLK
10	VDD / GND 1)
12	DAT_IN
13	DAT_OUT
15	FSC (output)

1) must be connected to a fixed potential

Table 4: Pin definition in MUX mode, FSC as output

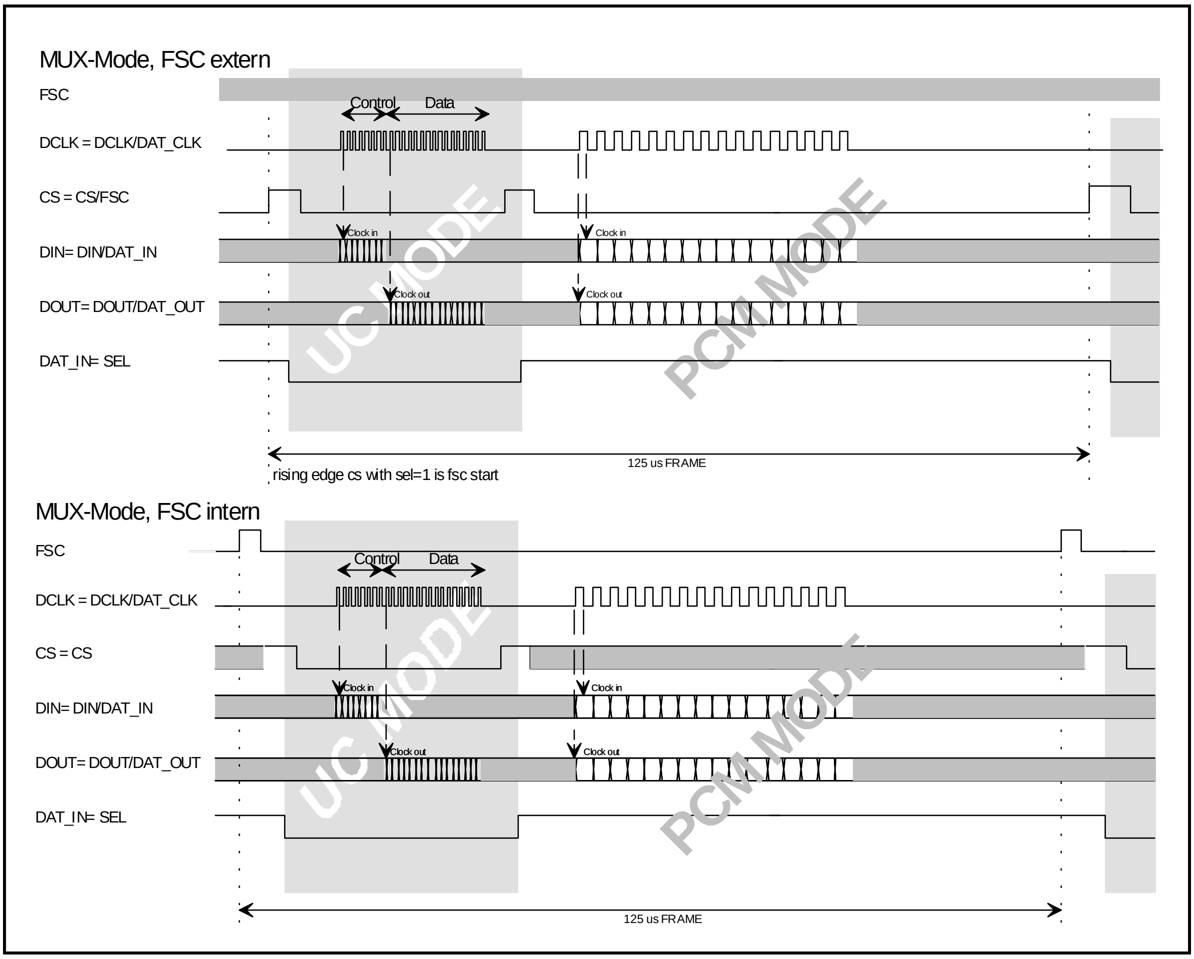


Figure 16: Protocol for transmission of µC- and PCM data in MUX mode

5.3 Clocking

ALIS works with a master clock frequency of typically 16.384 MHz. This clock can either be supplied from an external source or generated with a crystal by ALIS_D.

It is essential that the ratio of the master clock frequency to the FSC frequency is exactly 2048. This is of course guaranteed if the FSC signal is generated internally.

5.3.1 External clock

An external clock signal must be connected to pin MCLK1. The MCLK2 pin must remain unconnected and the CLK_EXT bit in CR0 must be programmed to a logic '1'. See "CR0 Configuration Register 0 (filters)" on page 37

5.3.2 Crystal clock

Because the ALIS includes an on- chip oscillator circuit, an external crystal may be used. The crystal should be connected across the MCLK1 and MCLK2 pins with two capacitors connected as shown in figure 17. The CLK_EXT bit in CR0 must be programmed to a logic ’0’ (=default value after reset). Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor- grade crystal should be used.

To ensure that the ratio between master clock and FSC signal is correct, ALIS must be programmed to internal FSC generation (set Fsc_en bit in CR4 to a logic’1’). See “Host interface in parallel mode, FSC as output” on page 29 and “Host interface in MUX mode, FSC as output” on page 31.

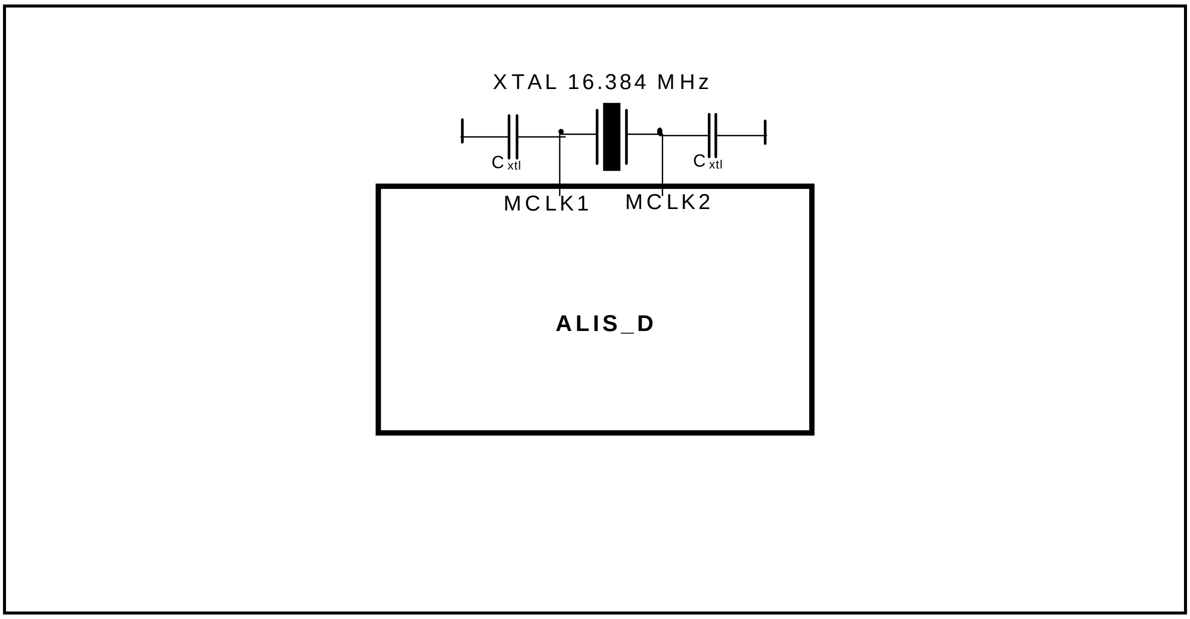


Figure 17: External crystal connections

5.4 Capacitive Interface

To decouple ALIS_A from ALIS_D, a capacitive interface is used. It is a bidirectional serial interface and used for exchanging control and data information between ALIS_A and ALIS_D. To avoid distortion and for performance reasons the transmission format is digital. For size and tolerance of the capacitors see page “ALIS Cap interface” on page 83.

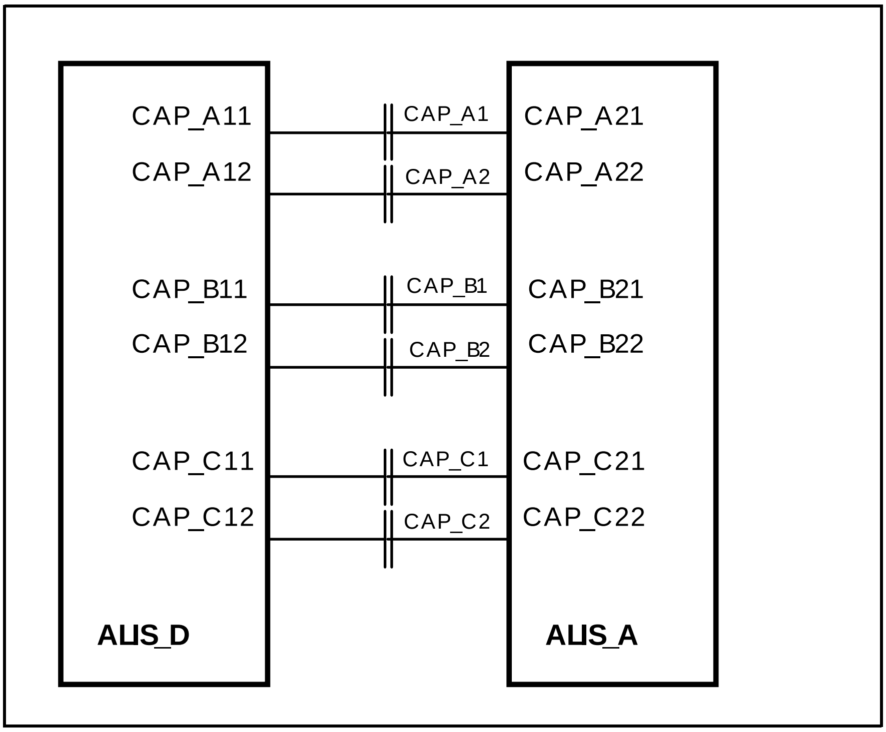


Figure 18: Connection of capacitive interface between ALIS_A and ALIS _D

5.5 Caller ID Interface

To receive the Caller ID ALIS_D has to be connected to the line via a RC network. See “ALIS Caller ID Interface” on page 82

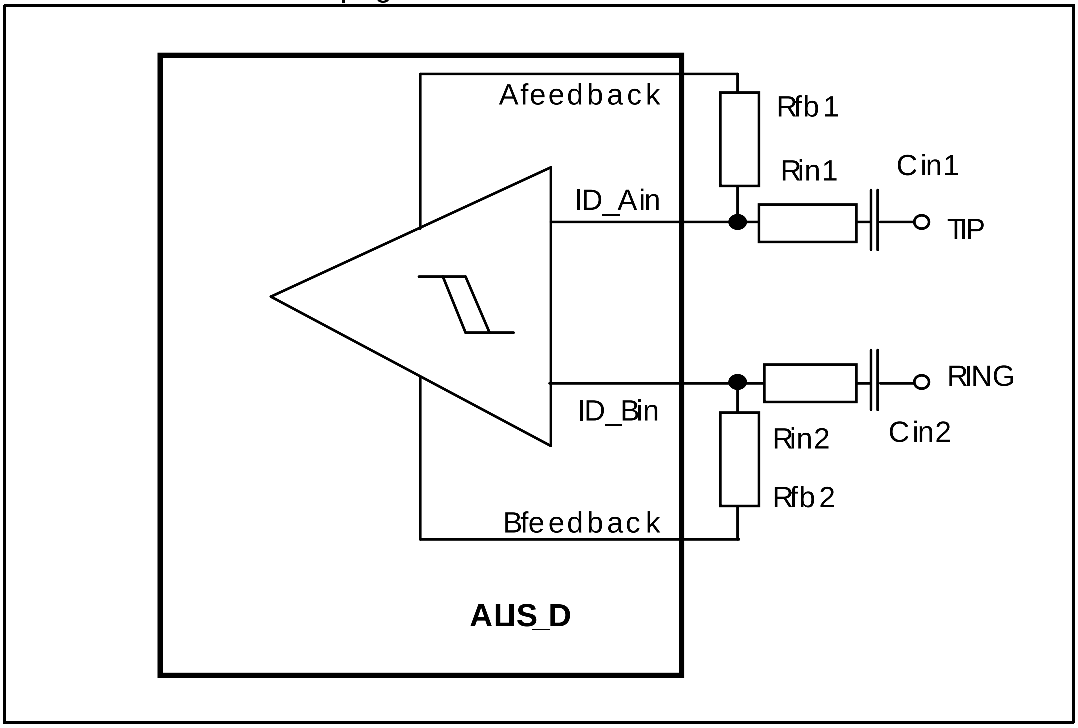


Figure 19: Caller ID interface connection of ALIS_D to TIP/RING

6 Programming ALIS

With the appropriate commands ALIS can be programmed and verified very flexibly via the serial µ-controller interface.
Four different commands are used to access the various control registers and RAMs (SOP, XOP COP and CAO command). The first byte received via DIN, selects the command type. Each command can be used as a write or read command. Due to the extended ALIS control facilities, SOP, XOP and COP commands contain additional information for programming (writing) and verifying (reading) the ALIS status (e.g., number of subsequent bytes, software reset, operating mode).
With a SOP, XOP or COP command up to 8 bytes of data can be read or written. With the CAO command all 512 bytes of the caller-ID RAM can be read or written. Any read command causes the ALIS to respond with its specific identification byte before sending the requested information.

6.1 Types of Commands and Data Bytes

The ALIS commands are selected by bit 3, 4 and 6 of the command byte as shown below.

SOP command

Bit	7	6	5	4	3	2	1	0
	PU 1	PU 0	RW	1	0	LSEL2	LSEL1	LSEL0

XOP command

Bit	7	6	5	4	3	2	1	0
	RST	0	RW	1	1	LSEL2	LSEL1	LSEL0

COP command

Bit	7	6	5	4	3	2	1	0
	0	0	RW	0	CODE 3	CODE 2	CODE 1	CODE 0

CAO command

Bit	7	6	5	4	3	2	1	0
	0	1	RW	1	1	0	0	0

6.1.1 Storage of programming information:

- 6 Configuration registers: CR0, CR1,... CR5 accessed by SOP commands
- 8 Extended registers: XR0, XR1,... XR7 accessed by XOP commands
- 1 Coefficient RAM: CRAM accessed by COP commands
- 1 Caller ID RAM: RAM accessed by CAO commands

6.2 SOP Command

With the SOP-Command (status operation command) the ALIS status registers can be written or read via the µ-controller interface.

Bit	7	6	5	4	3	2	1	0
	PU 1	PU 0	RW	1	0	LSEL2	LSEL1	LSEL0

PU Power Up Operation Command (only with SOP write command)

PU = 0 0: ALIS will be set to Sleep Mode

PU = 0 1: ALIS will be set to Ringing Mode

PU = 1 0: ALIS will be set to Conversation Mode

PU = 1 1: ALIS will be set to Pulse Dialing Mode

RW Read/Write: Enables reading from the ALIS or writing information to the ALIS

RW = 0: Write to ALIS

RW = 1: Read from ALIS

LSEL Length select information (see also programming procedure)
This field identifies the number of subsequent data bytes

LSEL = 000: 1 byte of data is following (CR0)

LSEL = 001: 2 bytes of data are following (CR1, CR0)

LSEL = 010: 3 bytes of data are following (CR2. CR1, CR0)

LSEL = 011: 4 bytes of data are following (CR3, CR2. CR1, CR0)

LSEL = 100: 5 bytes of data are following (CR4, CR3, CR2, CR1, CR0)

LSEL = 101: 6 bytes of data are following (CR5, ..., CR1, CR0)[1)]

Note: If only one configuration register requires modification, for example CR3, this can be accomplished by setting LSEL=011 and releasing pin CS after CR3 is written.

6.2.1 CR0 Configuration Register 0 (filters)

Default value: 00H
Configuration register CR0 defines the basic ALIS settings, which are: enabling/ disabling the programmable digital filters and tone generators.

Bit	7	6	5	4	3	2	1	0
	TH	IM	FRX	FRR	AX	AR	RIP	CLK_ EXT

TH Enable TH (TransHybrid Balancing)-Filter

TH = 0: TH-filter disabled

TH = 1: TH-filter enabled

IM Enable IM (Impedance Matching)-Filter

IM = 0: IM-filter disabled

IM = 1: IM-filter enabled

FRX Enable FRX (Frequency Response Transmit)-Filter

FRX = 0: FRX-filter disabled

FRX = 1: FRX-filter enabled

FRR Enable FRR (Frequency Response Receive)-Filter

1 all other codes for testpurpose only

FRR = 0: FRR-filter disabled

FRR = 1: FRR-filter enabled

AX Enable AX (Amplification/Attenuation Transmit)-Filter

AX = 0: AX-filter disabled

AX = 1: AX-filter enabled

AR Enable AR (Amplification/Attenuation Receive)-Filter

AR = 0: AR-filter disabled

AR = 1: AR-filter enabled

RIP Enable RIP (Ringer Impedance)-Filter

RIP = 0: RIP-filter disabled

RIP = 1: RIP-filter enabled

CLK_EXT External clock signal

CLK_EXT = 0: Crystal Oscillator is enabled, clock will be generated by crystal

CLK_EXT = 1: Crystal Oscillator is disabled, clock has to be supplied by external source

6.2.2 CR1 Configuration Register 1 (dialing)

Default value: 00H
Configuration register CR01 selects tone generator modes and other operation modes

Bit	7	6	5	4	3	2	1	0
	E_ Tone2	E_ Tone1	P_ Tone2	P_ Tone1	Pulse	No_ auto_ ring	RMR	RM

E_Tone2 Enable programmable tone generator 2

E_Tone2= 0: programmable tone generator 2 is disabled

E_Tone2= 1: programmable tone generator 2 is enabled

E_Tone1 Enable programmable tone generator 1

E_Tone1= 0: programmable tone generator 1 is disabled

E_Tone1= 1: programmable tone generator 1 is enabled

P_Tone2 User programmed frequency or fixed frequency is selected

P_Tone2= 0: fixed frequency for tone generator 2 is selected

P_Tone2= 1: programmed frequency for tone generator 2 is selected

P_Tone1 User programmed frequency or fixed frequency is selected

P_Tone1= 0: fixed frequency for tone generator 1 is selected

P_Tone1= 1: programmed frequency for tone generator 1 is selected

Pulse Pulse dialing

Pulse = 1: Make for pulse dialing

Pulse = 0: Break for pulse dialing

No_auto_ring

No_auto_ring= 1:testmode to disable automatic switching from Sleep Mode to Ringing Mode, after valid ring.

No_auto_ring= 0:normal operating mode, ALIS switches automatically to ringing Mode after ring detection

RMR Result of Ringing Metering function (this bit can not be written)

RMR = 0: level detected was lower than the programmed[1)] reference

RMR = 1: level detected was higher than the programmed reference. See “Flow of Ring sequence and detection” on page 62

RM Ringing Metering function[2)]

RM = 0: Ringing metering function is disabled

RM = 1: Ringing metering function is enabled

6.2.3 CR2 Configuration Register 2 (caller ID)

Bit	7	6	5	4	3	2	1	0
	COT/R			IDR	Call_pon	Call_en	Call_I	Call_II

Default value: 00H

COT/R Selection of Cut Off Transmit/Receive Paths

0 0 0: Normal Operation

0 0 1: COR16 Cut Off Receive Path at 16 kHz (input of TH-Filter)

0 1 0: COR8 Cut Off Receive Path at 8 kHz

1 0 1: COT2M Cut Off Transmit Path at 2MHz (POFI-output)

1 1 0: COT64 Cut Off Transmit Path at 64 KHz (IM-filter input)

IDR Initialize Data RAM

IDR = 0: normal operation is selected

1 The threshold can be programmed in the CRAM. Coefficients See “Ring Detect” on page 78.

2 Explanation of the ringing metering function: The ring signal is rectified, and the voltage is measured. If the voltage exceeds a certain value the bit RMR is set to '1'.

IDR = 1: contents of Data RAM is set to 0 (for test purposes)

Call_pon Enable the Caller ID Path

Call_pon = 0: Caller ID Path disabled

Call_pon = 1: Caller ID Path enabled
(see Call_pctl in “CR3 Configuration Register 3 (testloops)” on page 40

Call_en Enable the Caller ID

Call_en = 1: Caller ID decoding is enabled

Call_en = 0: Caller ID decoding is disabled

Call_I Result of Caller ID decoding (this bit can not be written, test purpose only)

Call_I = 1: 1st tone of Caller ID detected

Call_I = 0: 1st tone of Caller ID not detected

Call_II Result of Caller ID decoding (this bit can not be written, test purpose only)

Call_II = 1: 2nd tone of Caller ID detected

Call_II = 0: 2nd tone of Caller ID not detected

6.2.4 CR3 Configuration Register 3 (testloops)

Bit	7	6	5	4	3	2	1	0
	Test-Loops				SEL	Call_ pctl	DHP-R	DHP-X

Default value: 00H

Test-Loops 4 bit field for selection of analog and digital loop backs

0101 ALB_CIF: Cap. interface loop the signal from the input circuit (CAP_B11/12 is connected to the output drivers (CAP_A11/12, CAP_C11/12)

1000 ALB-CID: Caller ID loop; the output signal from the caller ID comparator is connected to the output drivers of the capacative interface (CAP_A11/12, CAP_C11/12);

1001 DLB-2M: Loop via HW-filters;

1100 DLB-128k: Loop inside DSP;

1101 DLB-64k: Loop inside DSP;

1111 DLB-PCM: Loop via PCM-interface; the received data is sent back in the next frame;

SEL Test loop selection

SEL = 0: Test loops via impedance path are selected

SEL = 1: Test loops via receive path are selected

Call_pctl Caller ID Path control

Call_pctl = 0: Caller ID interface is enabled during ringing mode

Call_pctl = 1: Caller ID interface will be selected by the Call_pon bit in CR2

Note: For test purposes the path can be controlled manually. Must be '0' for normal operation.

DHP-X Disable highpass in transmit direction

DHP-X = 0: transmit high pass is enabled

DHP-X = 1: transmit high pass is disabled

DHP-R Disable highpass in receive direction

DHP-R = 0: receive high pass is enabled

DHP-R = 1: receive high pass is disabled

6.2.5 CR4 Configuration Register 4 (analog gain)

Bit	7	6	5	4	3	2	1	0
	AGR_ Z 1	AGR_ Z 0	AGR_ R 1	AGR_ R 0	AGX 1	AGX 0	Int_en	Fsc_ en

Default value: 00H

AGR_Z Analog gain in impedance loop (can be used as AGC)

AGR_Z = 00: analog gain A is disabled (0 dB amplification)

AGR_Z = 11: analog gain A is enabled (2.5 dB amplification)

AGR_Z = 10: analog gain A is enabled (6 dB amplification)

AGR_Z = 01: analog gain A is enabled (-3.5 dB amplification)[1)]

AGR_R Analog gain in receive direction (can be used as AGC)

AGR_R = 00: analog gain B is disabled (0 dB amplification)

AGR_R = 01: analog gain B is enabled (3.5 dB amplification)

AGR_R = 11: analog gain B is enabled (6 dB amplification)

AGX Analog gain in transmit direction (can be used as AGC)

AGX = 00: analog gain A is disabled (0 dB amplification)

1 Note: for stability reasons the sun of AGR_Z and AGX should be zero.

AGX = 01: analog gain A is enabled (-6 dB amplification)

AGX = 10: analog gain A is enabled (3.5 dB amplification)

AGX = 11: analog gain A is enabled (-2.5 dB amplification)

Int_en Interrupt enable

Int_en = 1: Enable interrupts

Int_en = 0: Disable interrupts

Fsc_en FSC signal source selection

Fsc_en = 0: FSC must be generated externally

Fsc_en = 1 FSC is generated internally

6.2.6 CR5 Configuration Register 5 (Version)

Bit	7	6	5	4	3	2	1	0
	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

V The actual version of the ALIS (this byte can not be written)

02H for ALIS V2.1

6.3 XOP Command

With the XOP command (extended operation command) the ALIS digital command/ indication interface to the line and external equipment is configured and evaluated. Also other common functions are assigned with this command.

Bit	7	6	5	4	3	2	1	0
	RST	0	RW	1	1	LSEL2	LSEL1	LSEL0

RST Software Reset (same as RESET-pin)

RST = 0: No reset

RST = 1: ALIS is reset to the default settings

RW Read / Write: Enables reading from the ALIS or writing to the ALIS

RW = 0: Write to ALIS

RW = 1: Read from ALIS

LSEL Length select information, specifies the number of subsequent data bytes

LSEL = 000 1 byte of data is following (XR0)

LSEL = 001   2 bytes of data are following (XR1, XR0)

:

LSEL= 111   8 bytes of data are following (XR7, ..., XR1, XR0)

6.3.1 XR0 Extended Register 0 (Interrupt Register)

Any interrupt indications can be monitored in the interrupt register. Interrupts can be signalled through a logic high at the INT-line. After an indication occurred further loading of the interrupt register is locked until its contents is read via the µ–Controller interface. Reading of the interrupt register XR0 releases the lock and the INT-line is set to low again. See “Interrupt Controller” on page 58 for more details.

In connection with XOP-Read commands

Bit	7	6	5	4	3	2	1	0
	0	Wake_ up	Ca- dence	RING	Caller _ID	VDD_ OK	SI_1	SI_0

Default value: 00H

Wake_up Wake_up Interrupt

Wake_up = 0: no Wake_up Interrupt

Wake_up = 1: if CLK_OFF bit is set (See “XR6 Extended Register 6 (Power State)” on page 47) and a ring signal occurs[1)] a Wake_up Interrupt is generated. To clear this interrupt the CLK_OFF bit must be reset and ALIS_D has to be supplied with a clock.

Cadence Cadence Interrupt

Cadence = 0: no Cadence Interrupt
(time between two ring bursts is available in XR4)

Cadence = 1: time between two ring bursts exceeds the programmed time
(see “XR2 Extended Register 2 (Cadence Time Out)” on page 45

RING Ring Interrupt

RING = 0: no Ring Burst

RING = 1: No_auto_ring= 0: this bit is set after the second valid Ring Burst
No_auto_ring= 1: ALIS stays in the Sleep Mode and waits for a command. This bit represents the Ring detection signal from the ALIS _A. See “CR1 Configuration Register 1 (dialing)” on page 38

1 any signal at the line with a voltage of more than 18 V. To decode a valid ring signal ALIS must be switched to the Ringing Mode.

Note: In this case a command is mandatory to avoid a deadlock.

Caller_ID Caller ID Interrupt

Caller_ID = 0: no Caller ID preamble detected

Caller_ID = 1: Caller ID preamble detected

VDD_OK Vdd at ALIS_A Interrupt

VDD_OK = 1: power supply for ALIS_A is available and connection between ALIS_A and ALIS_D is working

VDD_OK = 0: no power supply for ALIS_A or no connection between ALIS_A and ALIS_D

SI_0 status of pin SI_0 at ALIS_A is transferred to this register

SI_1 status of pin SI_1 at ALIS_A is transferred to this register

Note: The auxiliary pins (SO_0, SO_1, SI_0, SI_1) are isolated via the capacitive interface.

In connection with XOP-Write commands to control the Output pins SO

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	SO_2	SO_1	SO_0

SO_0 pin SO_0 at ALIS_A is set to the assigned value if ALIS is not in sleep mode

SO_1 pin SO_1Q at ALIS_A is set to the inverted assigned value if ALIS is not in sleep mode

SO_2 pin SO at ALIS_D is set to the assigned value

6.3.2 XR1 Extended Register 1 (Interrupt enable Register)

Bit	7	6	5	4	3	2	1	0
	0	M_Wake_up	M_Cadence	M_RING	M_Caller_ID	M_VDD_OK	M_SI_1	M_SI_0

Default value: 00H

M_Wake_up

M_Wake_up = 0:Disable Wake_up Interrupt

M_Wake_up = 1:Enable Wake_up Interrupt

M_Cadence

M_Cadence = 0:Disable Cadence Interrupt

M_Cadence = 1:Enable Cadence Interrupt

M_RING

M_RING = 0: Disable RING Interrupts

M_RING = 1: Enable RING Interrupts

M_Caller_ID

M_Caller_ID = 0:Disable Caller_ID Interrupt

M_Caller_ID = 1:Enable Caller_ID Interrupt

M_VDD_OK

M_VDD_OK = 0:Disable VDD Interrupt

M_VDD_OK = 1:Enable VDD Interrupt

M_SI_1

M_SI_1 = 0: Disable Interrupts of SI_1

M_SI_1 = 1: Enable Interrupts of SI_1

M_SI_0

M_SI_0 = 0: Disable Interrupts of SI_0

M_SI_0 = 1: Enable Interrupts of SI_0

6.3.3 XR2 Extended Register 2 (Cadence Time Out)

Bit	7	6	5	4	3	2	1	0
	CTO 7	CTO 6	CTO 5	CTO 4	CTO 3	CTO 2	CTO 1	CTO 0

Default value: 7DH

CTO ms

Programmable Cadence Time Out: if the time between the first two ring bursts exceeds the time progammed in this register a cadence interrupt is generated. The time out is programmable in steps of 64 ms up to 16 seconds.

Note: 00 means no Cadence timeout programmed - no interrupt will be generated.

6.3.4 XR3 Extended Register 3 (DC Characteristic)

Bit	7	6	5	4	3	2	1	0
	AGB1	AGB0	B_off	DCU 1	DCU 0	DCI	DCR 1	DCR 0

AGB analog gain for the analog transhybrid filter

AGB = 00: Gain for analog transhybrid - filter = 24.6 dB

AGB = 01: Gain for analog transhybrid - filter = 21.6 dB

AGB = 10: Gain for analog transhybrid - filter = 18.6 dB

AGB = 11: Gain for analog transhybrid - filter = 16.1 dB

B_off Enable analog Transhybrid filter

B_off = 0: analog transhybrid - filter on

B_off = 1: analog transhybrid - filter off

Note: the analog transhybrid filter is a analog Prefilter optimised for long loops with a transhybrid loss of about 10 dB.

DCU = 00: U0 for DC Characteristic is 0 V

DCU = 01: U0 for DC Characteristic is 1.5 V

DCU = 10: U0 for DC Characteristic is 3.5 V

DCU = 11: U0 for DC Characteristic is 7.2 V

Note: these values does not include the voltage drop at the external diodes see also “DC Characteristics” on page 80

DCI Limit current for the DC characteristic

DCI = 0: Limit current is 100mA

DCI = 1: Limit current is 50 mA

DCR Resistance of the DC characteristic

DCR = 00: R for DC Characteristic is 280 Ω

DCR = 01: R for DC Characteristic is 240 Ω

DCR = 10: R for DC Characteristic is 200 Ω

DCR = 11: R for DC Characteristic is 100 Ω

Note: If DCU is programmed to 7.2V (DCU = 11) R for DC Characteristic is always 70 Ω independent of the contents of DCR. See “DC Termination” on page 80

6.3.5 XR4 Extended Register 4 (Cadence)

Bit	7	6	5	4	3	2	1	0
	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

C ms (read only)

Contains the measured time between the two first ring bursts (time step 64 ms) if the time is below the cadence time- out as programmed in XR2.

6.3.6 XR5 Extended Register 5 (Ring timer)

Bit	7	6	5	4	3	2	1	0
	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0

Default value: 22H

T ms

Ring latency timer, programmable in steps of 2 ms

ALIS_A decodes any signal with more than 18 V at TIP/RING. This signal will be handled over to ALIS_D for further processing. This timer bridges the time when the sinewave of the ringsignal is below the noted 18 V to make sure that ALIS does not fall back into the sleep mode.

6.3.7 XR6 Extended Register 6 (Power State)

Bit	7	6	5	4	3	2	1	0
	0	0	0	CKL_ OFF	0	0	CPS1	CPS0

Default value: 00H

CPS Current Power State (read only)

CPS = 00 Power state is sleep

CPS = 01 Power state is ringing

CPS = 10 Power state is conversation

CPS = 11 Power state is pulse dialing

Note: the power mode can be programmed by the SOP command. In this register the current power state will be reflected.

CLK_OFF Turn off master clock (ALIS is programmed to deep- sleep mode)

CLK_OFF = 0 Master clock is not turned off internally

CLK_OFF = 1 Master clock is turned off internally

Note: the external clock can be turned off after setting the CLK_OFF bit. For programming ALIS the clock must be switched on.

Note: when a crystal is used it will be turned off automatically when the CLK_OFF bit is set. It will be switched on when the CS signal goes low. However the user must wait until the crystal is working before initiating a command.

6.3.8 XR7 Extended Register 7 (Vdd)

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	Vdd1	Vdd0	0

Default value: 00H

Vdd Current Power State

Vdd = 00 Vdd of ALIS_A is 4.25 V

Vdd = 01 Vdd of ALIS_A is 4.4 V (Test purpose only)

Vdd = 10 Vdd of ALIS_A is 3.85 V (Test purpose only)

Vdd = 11 Vdd of ALIS_A is 4 V

6.4 COP Command

With a COP Command the coefficients for the programmable filters can be written to ALIS Coefficient RAM or read from the Coefficient RAM via the µ-Controller interface for verification.

Bit	7	6	5	4	3	2	1	0
	0	0	RW	0	CODE 3	CODE 2	CODE 1	CODE 0

RW Read/Write

RW = 0 Subsequent data is written to ALIS

RW = 1 Read data from ALIS

CODE includes number of following bytes and filter-address

0	0	0	0	TH-Filter coefficients (part 1)	(followed by 8 bytes of data)
0	0	0	1	TH-Filter coefficients (part 2)	(followed by 8 bytes of data)
0	0	1	0	TH-Filter coefficients (part 3)	(followed by 8 bytes of data)
0	0	1	1	Ringer Impedance (part 1	(followed by 8 bytes of data)
0	1	0	0	IM-Filter coefficients (part 1)	(followed by 8 bytes of data)
0	1	0	1	IM-Filter coefficients (part 2)	(followed by 8 bytes of data)
0	1	1	0	Ringer Impedance (part 2)	(followed by 8 bytes of data)
0	1	1	1	FRR-Filter coefficients	(followed by 8 bytes of data)
1	0	0	0	FRX-Filter coefficients	(followed by 8 bytes of data)
1	0	0	1	AR-Filter coefficients	(followed by 4 bytes of data)
1	0	1	0	AX-Filter coefficients	(followed by 4 bytes of data)
1	0	1	1	Tone1- coefficients	(followed by 4 bytes of data)
1	1	0	0	Tone2- coefficients	(followed by 4 bytes of data)
1	1	0	1	Levelmetering Ringing	(followed by 4 bytes of data)
1	1	1	0	Caller ID 1st Tone	(followed by 8 bytes of data)
1	1	1	1	Caller ID 2nd Tone	(followed by 8 bytes of data)

6.5 CAO Command

With a CAO Command the decoded Caller ID can be read. A CAO Command is always followed by 512 bytes of data.

Bit	7	6	5	4	3	2	1	0
	0	1	RW	1	1	0	0	0

RW Read/Write

RW = 0 Subsequent data is written to ALIS (test purpose only)

RW = 1 Read data from ALIS

6.6 Register Summary

6.6.1 CR Registers:

Bit	7	6	5	4	3	2	1	0
CR0	TH	IM	FRX	FRR	AX	AR	RIP	CLK_EXT
CR1	E_Tone2	E_Tone1	P_Tone2	P_Tone1	Pulse	No_auto	RMR	RM
CR2	COT/R			IDR	Call_pon	Call_en	Call_I	Call_II
CR3	TestLoops				SEL	Cal_pctl	DHP-R	DHP-X
CR4	AGR_Z 1	AGR_Z 0	AGR_R1	AGR_R 0	AGX 1	AGX 0	Int_en	Fsc_en
CR5	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

Table 5: Summary of CR Registers

6.6.2 XR Registers:

Bit	7	6	5	4	3	2	1	0
XR0/R	0	Wake_up	Cadence	RING	Caller_ID	VDD_OK	SI_1	SI_0
XR0/W	0	0	0	0	0	SO_2	SO_1	SO_0
XR1	0	M_Wake_up	M_Cadence	M_RING	M_Caller_ID	M_VDD_OK	M_SI_1	M_SI_0
XR2	CTO 7	CTO 6	CTO 5	CTO 4	CTO 3	CTO 2	CTO 1	CTO 0
XR3	AGB1	AGB0	B_off	DCU 1	DCU 0	DCI	DCR 1	DCR0
XR4	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
XR5	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0
XR6	0	0	0	CLK_OFF	0	0	CPS1	CPS0
XR7	0	0	0	0	0	Vdd1	Vdd0	0

Table 6: Summary of CR Registers

7 ALIS Command Structure

7.1 SOP Commands

7.1.1 SOP - Write Commands

DIN	7	6	5	4	3	2	1	0	DOUT (7 6 5 4 3 2 1 0)
SOP-Write 1 Byte	x	x	0	1	0	0	0	0	Idle
CR0	Data								Idle

DIN	7	6	5	4	3	2	1	0	DOUT (7 6 5 4 3 2 1 0)
SOP-Write 2 Bytes	x	x	0	1	0	0	0	1	Idle
CR1	Data								Idle
CR0	Data								Idle

DIN	7	6	5	4	3	2	1	0	Bit	7 6 5 4 3 2 1 0	DOUT
SOP-Write 3 Bytes	x	x	0	1	0	0	1	0		Idle	
CR2	Data									Idle	
CR1	Data									Idle	
CR0	Data									Idle	

DIN	7	6	5	4	3	2	1	0	Bit	7 6 5 4 3 2 1 0	DOUT
SOP-Write 4 Bytes	x	x	0	1	0	0	1	1		Idle	
CR3	Data									Idle	
CR2	Data									Idle	
CR1	Data									Idle	
CR0	Data									Idle	

7.1.2 SOP - Read Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 1 Byte	x	x	1	1	0	0	0	0		Idle								
	Idle									1	0	0	0	0	0	0	1	ID
	Idle									Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 2 Bytes	x	x	1	1	0	0	0	1		Idle								
	Idle									1	0	0	0	0	0	0	1	ID
	Idle									Data								CR1
	Idle									Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 3 Bytes	x	x	1	1	0	0	1	0		Idle								
	Idle									1	0	0	0	0	0	0	1	ID
	Idle									Data								CR2

	Idle										Data								CR1
	Idle										Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 4 Bytes	x	x	1	1	0	0	1	1		Idle								
	Idle									1	0	0	0	0	0	0	1	ID
	Idle									Data								CR3
	Idle									Data								CR2
	Idle									Data								CR1
	Idle									Data								CR0

Note: x according to the description of the Power Up operation command see “SOP Command” on page 36

7.2 XOP Commands

7.2.1 XOP - Write Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Write 2 Bytes	0	0	0	1	1	0	0	1		Idle								
XR1	Data									Idle								
XR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Write 3 Bytes	0	0	0	1	1	0	1	0		Idle								
XR2	Data									Idle								
XR1	Data									Idle								
XR0	Data									Idle								

7.2.2 XOP - Read Commands

DIN	7	6	5	4	3	2	1	0 Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Read 1 Byte	0	0	1	1	1	0	0	0	Idle								
	Idle								1	0	0	0	0	0	0	1	ID
	Idle								Data								XR0

DIN	7	6	5	4	3	2	1	0 Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Read 2 Bytes	0	0	1	1	1	0	0	1	Idle								
	Idle								1	0	0	0	0	0	0	1	ID
	Idle								Data								XR1
	Idle								Data								XR0

DIN	7	6	5	4	3	2	1	0 Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Read 3 Bytes	0	0	1	1	1	0	1	0	Idle								
	Idle								1	0	0	0	0	0	0	1	ID
	Idle								Data								XR2
	Idle								Data								XR1
	Idle								Data								XR0

7.3 COP Command

7.3.1 COP - Write Commands

DIN	7	6	5	4	3	2	1	0 Bit	7 6 5 4 3 2 1 0	DOUT
COP-Write 4 Bytes	0	0	0	0	b	b	b	b	Idle	
Coeff. 3	Data								Idle	
Coeff. 2	Data								Idle	
Coeff. 1	Data								Idle	
Coeff. 0	Data								Idle	

DIN	7	6	5	4	3	2	1	0	Bit	7 6 5 4 3 2 1 0	DOUT
COP-Write 8 Bytes	0	0	0	0	b	b	b	b		Idle	
Coeff. 7	Data									Idle	
Coeff. 6	Data									Idle	
Coeff. 5	Data									Idle	
Coeff. 4	Data									Idle	
Coeff. 3	Data									Idle	
Coeff. 2	Data									Idle	
Coeff. 1	Data									Idle	
Coeff. 0	Data									Idle	

7.3.2 COP - Read Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP-Read 4 bytes	0	0	1	0	b	b	b	b		Idle								
	Idle									1	0	0	0	0	0	0	1	ID
	Idle									Data								Coeff.3
	Idle									Data								Coeff.2
	Idle									Data								Coeff.1
	Idle									Data								Coeff.0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP-Read 8 bytes	0	0	1	0	b	b	b	b		Idle								
	Idle									1	0	0	0	0	0	0	1	ID
	Idle									Data								Coeff.7
	Idle									Data								Coeff.6
	Idle									Data								Coeff.5
	Idle									Data								Coeff.4
	Idle									Data								Coeff.3
	Idle									Data								Coeff.2

Idle		Data	Coeff.1
Idle		Data	Coeff.0

Note: b: according to the description of the COP commend. See “COP Command” on page 48

7.4 CAO Command

7.4.1 CAO - Write Commands

DIN	7 6 5 4 3 2 1 0 Bit	7 6 5 4 3 2 1 0
CAO Write	0 1 0 1 1 0 0 0	Idle
	Caller ID 512	Idle
	Caller ID 511	Idle
	Caller ID 510	Idle
	...	Idle
	Caller ID 1	Idle

7.4.2 CAO - Read Commands

DIN	7 6 5 4 3 2 1 0 Bit	7 6 5 4 3 2 1 0	DOUT
CAO Read	0 1 1 1 1 0 0 0		
	Idle	1 0 0 0 0 0 0 1	ID
	Idle	Data	Caller ID 512
	Idle	Data	Caller ID 511
	Idle		...
	Idle	Data	Caller ID 1

7.5 Example for a Mixed Command

Every single command must begin with a falling edge of CS.

DIN	7 6 5 4 3 2 1 0 Bit	7 6 5 4 3 2 1 0	DOUT
SOP-Write 4 Bytes	x x 0 1 0 0 1 1	Idle	
CR3	Data	Idle	
CR2	Data	Idle	
CR1	Data	Idle	
CR0	Data	Idle	
XOP-Write 2 Bytes	0 0 0 1 1 0 0 1	Idle	
XR1	Data	Idle	
XR0	Data	Idle	
COP-Write 4 Bytes	0 0 0 0 b b b b	Idle	
Coeff. 3	Data	Idle	
Coeff. 2	Data	Idle	
Coeff. 1	Data	Idle	
Coeff. 0	Data	Idle	
SOP-Read 3 Bytes	x x 1 1 0 0 1 0	Idle	
	Idle	1 0 0 0 0 0 0 1	ID
	Idle	Data	CR2
	Idle	Data	CR1
	Idle	Data	CR0
COP-Read 4 Bytes	0 0 1 0 b b b b	Idle	
	Idle	1 0 0 0 0 0 0 1	ID
	Idle	Data	Coeff.3
	Idle	Data	Coeff.2
	Idle	Data	Coeff.1
	Idle	Data	Coeff.0
XOP-Read 1 Byte	0 0 1 1 1 0 0 0	Idle	
	Idle	1 0 0 0 0 0 0 1	ID
	Idle	Data	XR0

8 Interrupt Controller

There are seven different sources that can cause interrupts in ALIS. The status of these sources can be read in the interrupt- register XR0. Every interrupt source can be enabled individually in the interrupt enable register XR1.

For monitoring an interrupt source the corresponding bit must be set in XR1. The interrupt register is locked if an enabled interrupt- indication occurs. The lock is released by reading the interrupt- register. Any interrupt indication that occurs during a lock-period will be detected after releasing the lock.

The INT-pad can be used as indication for external hardware to read the interrupt register. If the Int_en bit (CR4) is set, the INT-pad goes to high whenever the interrupt register is locked.

The host must analyse the bits in the interrupt- register to determine the cause for the pending interrupt. All interrupt- sources that are not enabled must be ignored by the host for analysis. It is possible that several sources cause only one interrupt all together! (i.e. break- down of serial connection to ALIS_A: VDD_OK, SI_0, SI_1; if more interrupts occur during the lock- period). If the interrupt was caused by a CADENCE, RING, CALLER_ID or WAKE_UP interrupt the indication that caused the pending interrupt is reset by reading the interrupt register XR0.

As only one interrupt can be stored internally the host must respond immediately to avoid loss of interrupts.

8.1 Nature and sources of interrupts:

There are three different kinds of interrupt indications depending on their source:

8.1.1 Interrupt indication on signal change:

Interrupts:	SI_0, SI_1, VDD_OK;
Sources:	Signalling pins at ALIS_A (SI_0, SI_1); VDD_OK indicates that ALIS_A has power supply and that the serial connection via the cap. interface is working;
Interrupt indication:	Any change of the signals will generate an interrupt. The host must store the previous state of these bits to check which signal caused an interrupt.
Note:	These bits will go to '0' when there is no connection to ALIS_A via the cap. interface, which will cause interrupts!
Lock behaviour:	At *lock-release-time* the current signal is compared to the signal stored at *lock-time*. Any difference will cause another interrupt.

8.1.2 Interrupt indication on event:

Interrupts:	CALLER_ID, RING, CADENCE;
Sources:	CALLER_ID: complete marker sequence of caller ID detected; RING: depending on automatic mode-switching: - detection of more than 18 V at TIP/RING (No_auto_ring '1'); - 2nd valid ringing (No_auto_ring '0'); CADENCE: time-out for 2nd ring- burst; the time can be programmed in XR2 (No_auto_ring '0');
Interrupt indication:	These interrupts indicate that a certain event has happened. The bits are set from their source and can only be reset from the host by reading the interrupt register. Whenever one of these bits is set, this is an indication that this event has happened.
Lock behaviour:	If one of these events occurs during the register is locked another interrupt will be generated as soon as the lock is released.

8.1.3 Interrupt indication on high level:

If ALIS_D is set to the deep-sleep mode (XR6, CLK_OFF = ’1’) this interrupt indicates that there is a signal greater than 18 V at TIP/RING.

Interrupts:	WAKE_UP;
Source:	ring_detect signal from ALIS_A;
Interrupt indication:	more than 18 V at TIP/RING. It is cleared after reading the interrupt- register. Another interrupt is generated if the signal remains higher than 18 V.
Lock behaviour:	The interrupt will lock the register as soon as clock is turned on again! (If no clock signal is applied to ALIS_D the other interrupts cannot occur anyway.)

9 Operating Modes

9.1 Reset (Basic setting mode)

Condition: RESET low, MCLK can be down

ALIS _D:

After initial application of VDD or setting pin RESET to '0' during operation, or by software-reset (see XOP command), ALIS _D enters a basic setting mode. Basic setting means, that ALIS_ D configuration registers CR0... CR5 and XR0... XR7 are initialized to the default value (Sleep mode). All programmable filters are disabled.

If any voltage is applied to any input-pin before initial application of VDD, ALIS may not enter the basic setting mode. In this case it is necessary to reset ALIS or to initialize ALIS configuration registers to the default value.

ALIS _A:

When the plug is connected to TIP / RING and the hook switch is closed, ALIS _A generates its supply voltage out of the line current and does a power on reset.

9.2 Deep Sleep Mode

Condition: RESET high, MCLK can be switched off, CLK_OFF bit is set

Will be entered from any mode by programming the CLK_OFF bit in XR6. During The Deep Sleep mode the serial control interface is ready to receive and register commands only when the MCLK is switched on. See “XR6 Extended Register 6 (Power State)” on page 47. Incoming rings will be indicated by the Wake_up Interrupt.

9.3 Sleep Mode

Condition: RESET high, MCLK must run

After releasing the RESET-pin (RESET-state), ALIS will enter the Sleep Mode. ALIS is forced to Sleep Mode with the PU (power up) bits set to '00' in the SOP command. During Sleep Mode the serial control interface is ready to receive commands and transmit data. Received voice data on DAT_IN-pin will be ignored. ALIS configuration registers Caller ID Ram and coefficient Ram can be loaded and read back in this mode.

9.4 Ringing Mode

Condition: RESET high, MCLK must run

Will be entered automatically when bit No_auto_ring is set to 0 from Sleep mode after first ring pulse or with the PU bits set to '01' in the SOP command. In this mode ALIS will measure level, frequency and cadence of the ring signal. The cadence between the first two ring bursts is stored in XR4. If the bit Caller_en is enabled an incoming caller ID will be decoded and stored (see CAO command).

9.5 Conversation Mode

Condition: RESET high, MCLK must run

The operating mode is entered upon recognition of the PU bits set to '10' in a SOP command.

In Conversation mode AC impedance and the DC - Loops are switched on. The programmed AC and DC characteristics are realized by this loops. Receive and transmit path are on. The tonegenerators are available.

9.6 Pulse Dialing Mode

Condition: RESET high, MCLK must run, off-hook

The Pulse Dialing Mode is entered by setting the PU bits to '11' in a SOP command.

In Pulse Dialing Mode the external transistor T1 will be switched on and off according to the bit PULSE in CR1. The pulse timing must be controlled by the host.

9.7 Operating Flow Chart

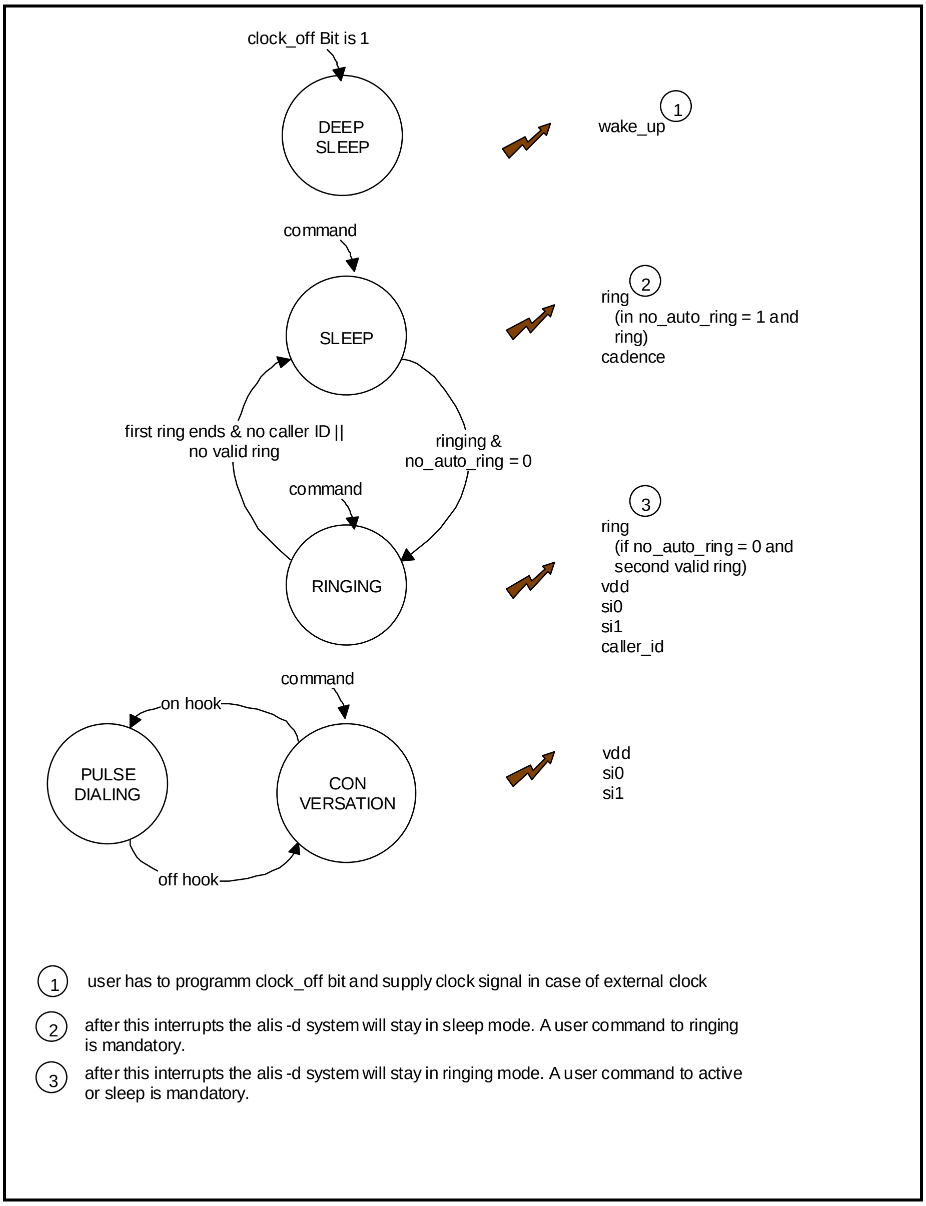


Figure 20:Operation modes transitions and Interrupts

9.8 Flow of Ring sequence and detection

Ring detection works in ALIS as a two step procedure.

As a first step ALIS_A will detect any AC signal at TIP and RING with a peak value of more than 18 V and generate the signal Ring_detect. This signal can either generate an interrupt or switch ALIS into the Ringing Mode depending on the No_auto_ring bit in CR1 (See “CR1 Configuration Register 1 (dialing)” on page 38) The current power mode can be read in “XR6 Extended Register 6 (Power State)” on page 47.

As a second step only if enabled by RM (See “CR1 Configuration Register 1 (dialing)” on page 38) in the Ringing Mode the TIP/RING Signal will be bandfiltered and compared to a programmable threshold. If the result is higher than this threshold the signal RMR-bit is set to one. Ring-threshold can be polled as RMR-bit in CR1. The following flow charts show these sequences in more detail.

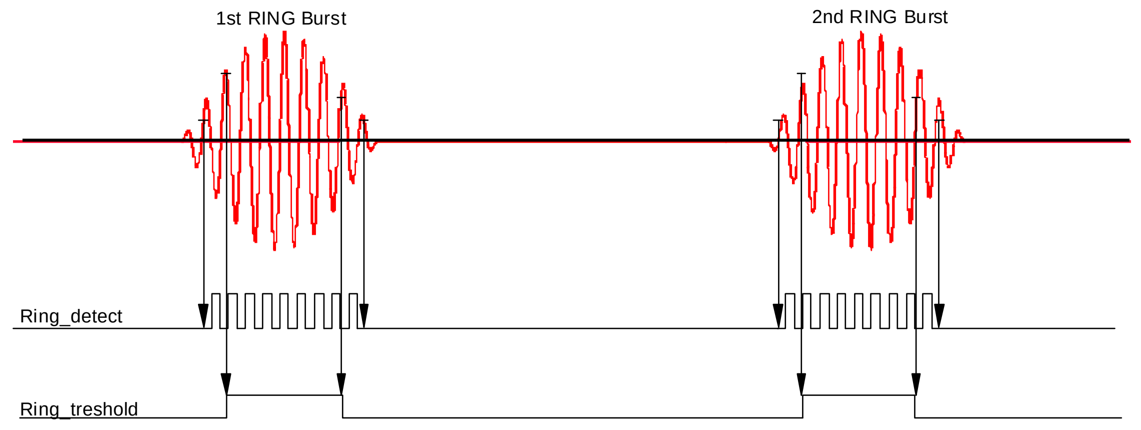
Note: The initial connection to TIP RING looks like a ring voltage to ALIS _A. ALIS_D reaction depends on auto_ring bit:
a) auto_ring: ALIS_D goes to ringing, since spike is no valid ringsignal after that ALIS_D goes to sleep mode.
b) No_auto_ring: ALIS_D generates a ring interrupt, stays in sleep mode and waits for a command. The user has to switch ALIS_D to ringing and poll the RMR bit. If ringing is not valid (RMR bit = 0) the chip can be set back to sleep mode.

To detect a valid ring signal and Caller ID ALIS automatically must be programmed to the following setting:

- set RM to ’1’ “CR1 Configuration Register 1 (dialing)” on page 38
- cadence timeout must programmed to PTT requirements “XR2 Extended Register 2 (Cadence Time Out)” on page 45
- ring latency timer must be programmed to a value higher four times of the ring period “XR5 Extended Register 5 (Ring timer)” on page 47
- valid ring coefficients
- set No_auto_ring to ’0’ “CR1 Configuration Register 1 (dialing)” on page 38
- enable Call_en “CR2 Configuration Register 2 (caller ID)” on page 39
- enable corresponding interrupts

9.8.1 Successful Ring_sequence, auto Ring enabled, No Caller ID

The following chart and diagram shows a successful flow of a ring-event detection with automatic power mode change (No_auto_ring = 0, Caller_en = 0, RM = 1). In this operation mode ALIS will not decode a Caller ID.



Line:	on hook	1st ring	on hook	2nd ring	on hook	off hook
Mode:	sleep	ringing	sleep	ringing		conv.
Counters		ringcounter	cadence counter	ringcounter		
Interrupts:		VDD_ok	VDD_ok	VDD_ok	VDD_ok ring	VDD_ok
Host CMDs:						close hook; conv.

Figure 21: successful Ring sequence, No_auto_ring = 0; Caller_en = 0

9.8.2 Successful Ring_sequence, auto Ring enabled, Caller ID

The following chart and diagram shows a successful flow of a ring-event detection with automatic power mode change (No_auto_ring = 0, Caller_en = 1, RM = 1). In this operation mode ALIS will decode and store a Caller ID.

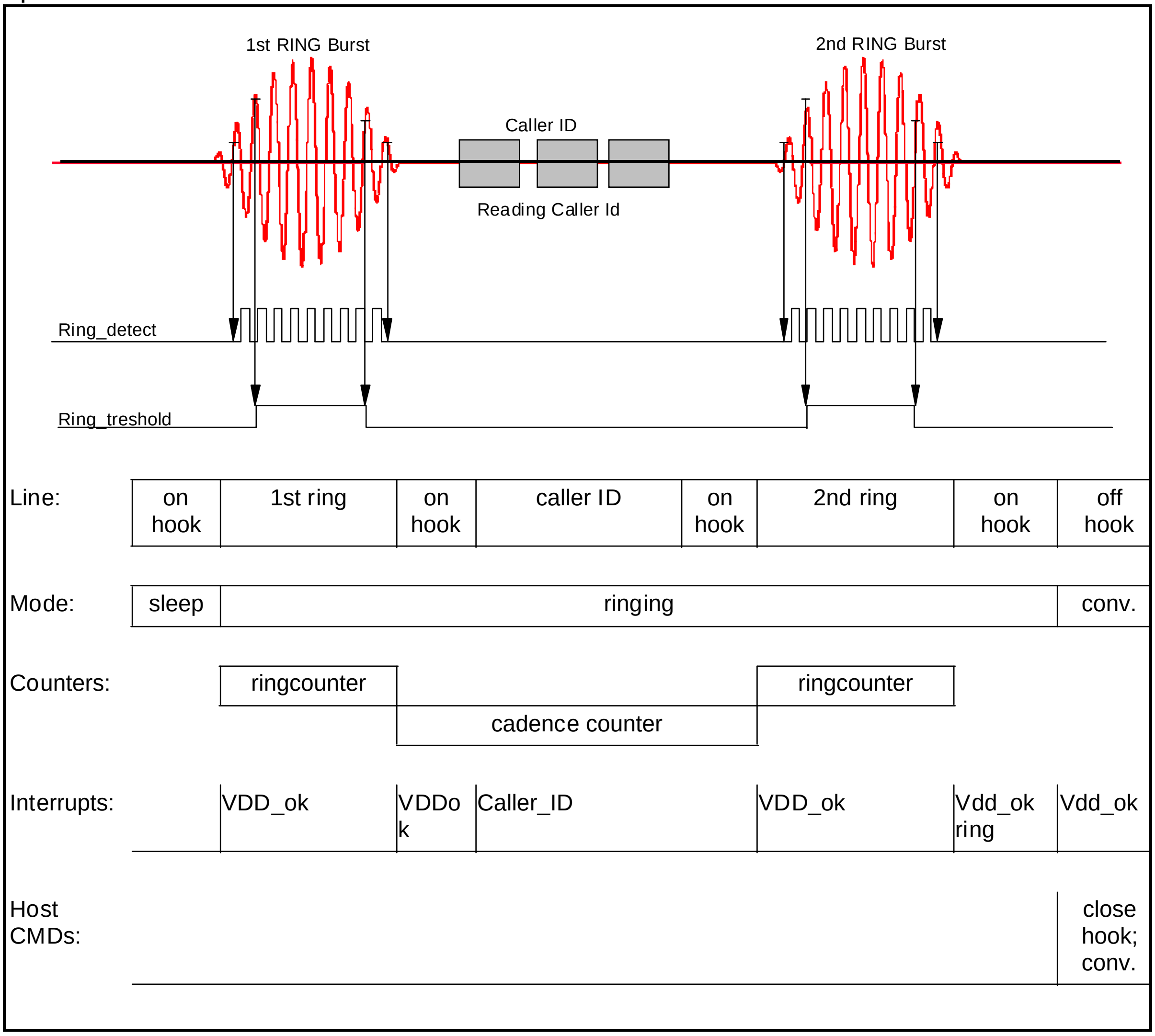


Figure 22: successful Ring sequence, No_auto_ring = 0; Caller_en = 1

9.8.3 Not successful Ring_sequence, auto Ring enabled, No Caller ID

The following chart and diagram shows a not successful flow of a ring-event detection because of no 2. ring with automatic power mode change (No_auto_ring = 0, Caller_en = 0, RM = 1).

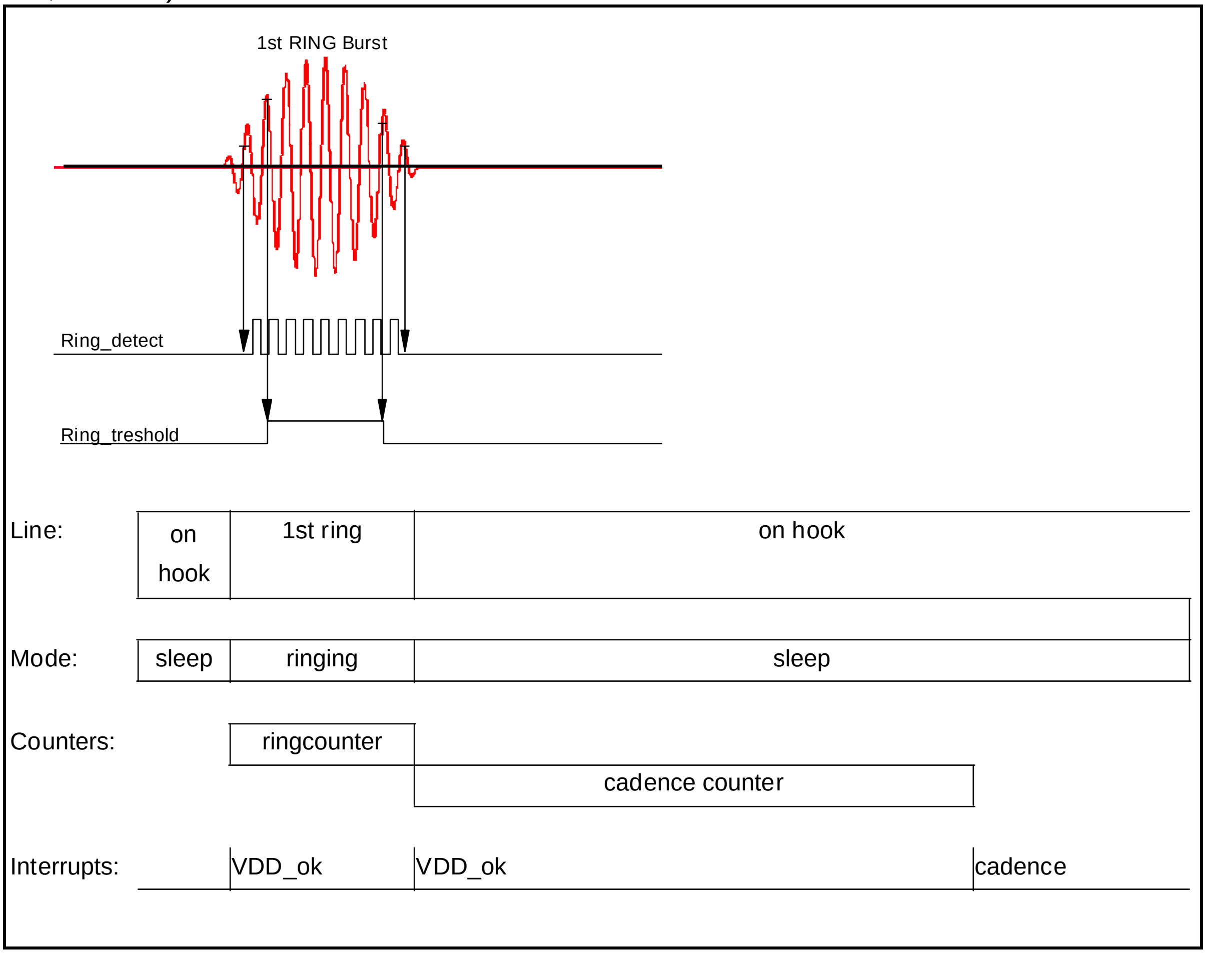


Figure 23: not successful Ring sequence, No_auto_ring = 0; Caller_en = 0

9.8.4 Not successful Ring_sequence, auto ring enabled, Caller ID

The following chart and diagram shows a not successful flow of a ring-event detection because of no 2. ring with automatic power mode change (No_auto_ring = 0, Caller_en = 1, RM = 1).

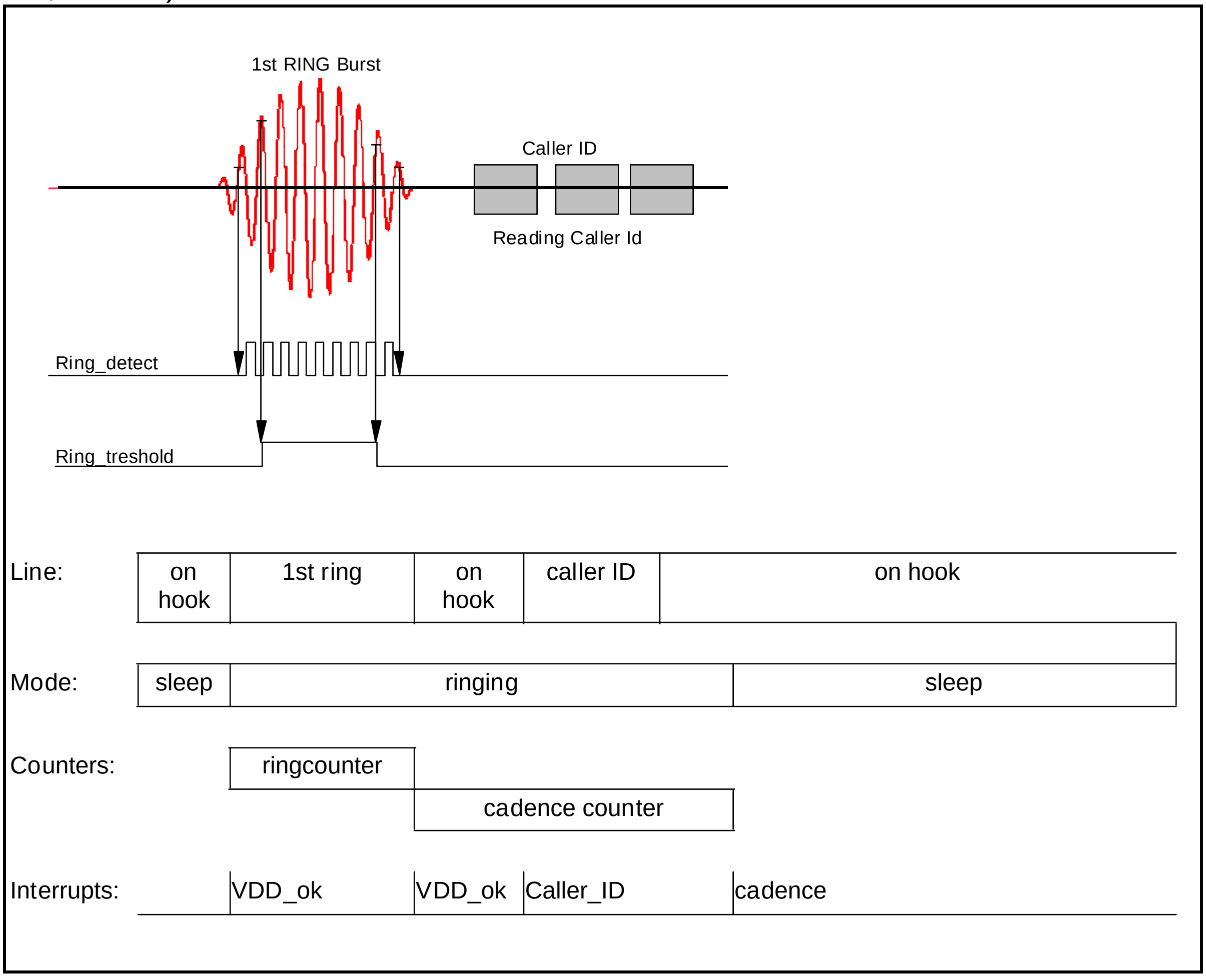


Figure 24: not successful Ring sequence, No_auto_ring = 0; Caller_en = 1

9.8.5 Successful Ring_sequence, auto Ring disabled, No Caller ID

The following chart and diagram show a successful flow of a ring-event detection with no automatic power mode change (No_auto_ring = 1, Caller_en = 0, RM = 1). In this operation mode ALIS will not decode the Caller ID.

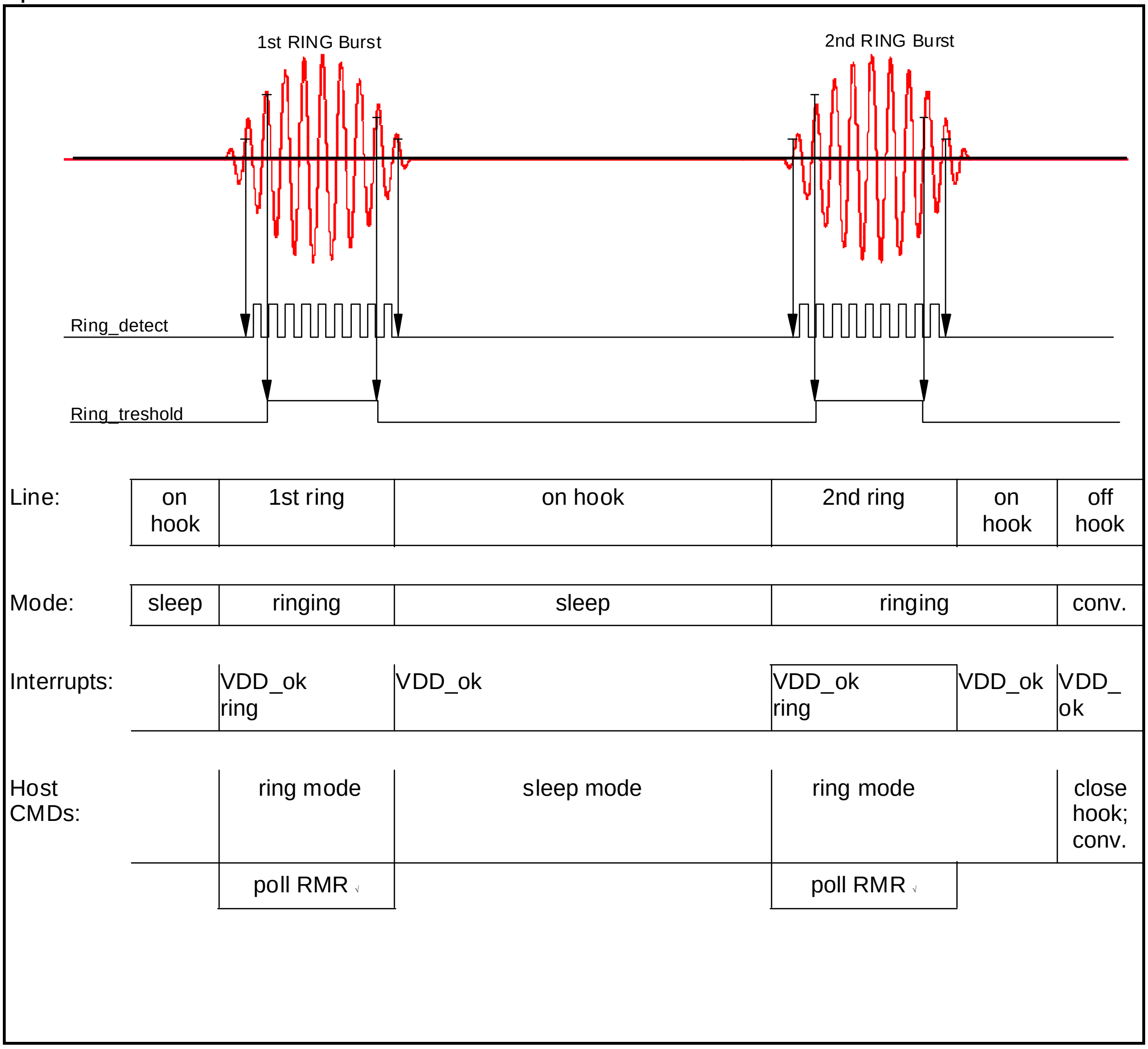


Figure 25: successful Ring sequence, No_auto_ring = 0; Caller_en = 0

Note: RMR bit must be polled by the host to verify that the ring signal is above the programmed threshold level and check VDD interrupts

9.8.6 Successful Ring_sequence, auto Ring disabled, Caller ID

The following chart and diagram show a successful flow of a ring-event detection with no automatic power mode change (No_auto_ring = 1, Caller_en = 1, RM = 1). In this operation mode ALIS will decode and store the Caller ID.

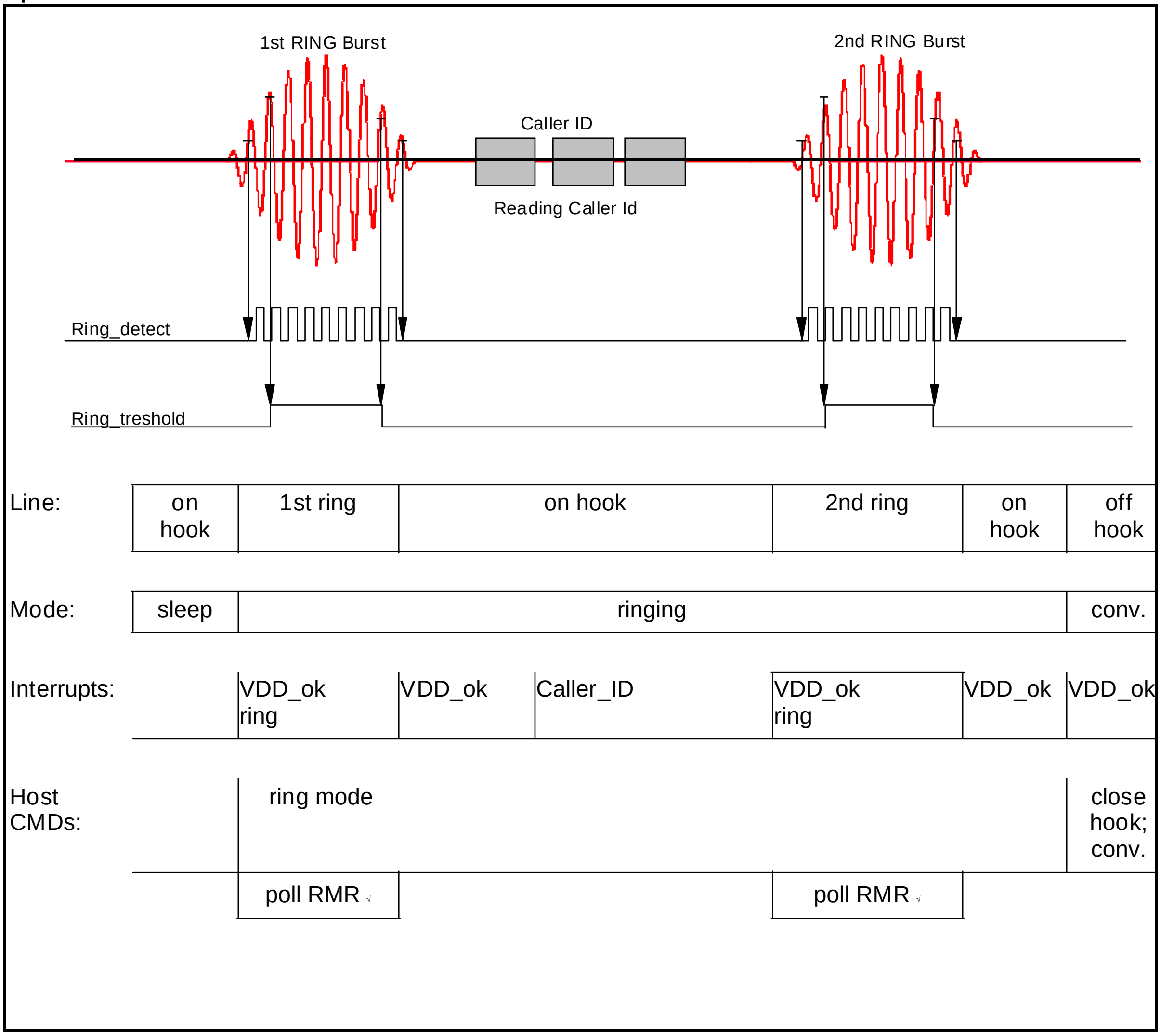
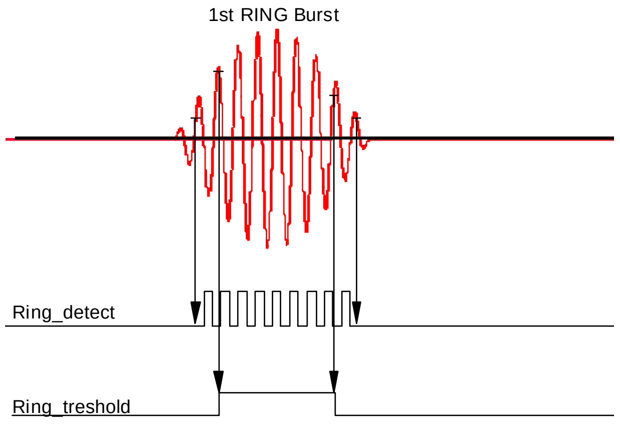


Figure 26: successful Ring sequence, No_auto_ring = 1; Caller_en = 1

Note: RMR bit must be polled by the host to verify that the ring signal is above the programmed threshold level.
Leaving ALIS in ringing mode after the first ring enables the detection and storage of the Caller ID.

9.8.7 Not successful Ring_sequence, auto Ring disabled, No Caller ID

The following chart and diagram show a not successful flow of a ring-event detection because of no 2. ring with no automatic power mode change (No_auto_ring = 1, Caller_en = 0, RM = 1).



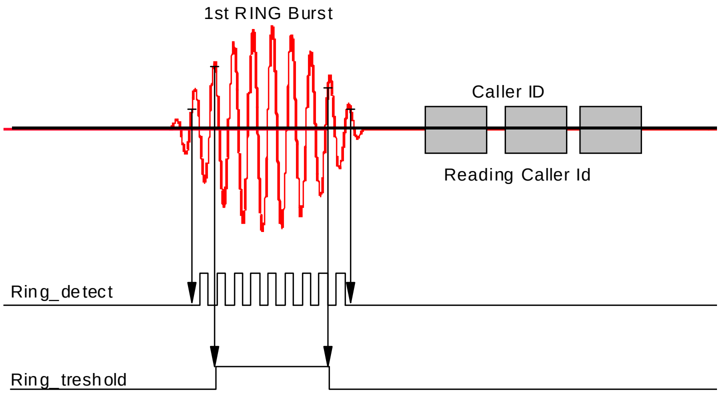
Line:	on hook	1st ring	on hook
Mode:	sleep	ringing	sleep
Interrupts:		VDD_ok ring	VDD_ok
Host CMDs:		ring mode	sleep mode
		poll RMR	

Figure 27: not successful Ring sequence, No_auto_ring = 1; Caller_en = 0

Note: RMR bit must be polled by the host to verify that the ring signal is above the programmed threshold level.
Cadence time and number of rings must be calculated by the host.

9.8.8 Not successful Ring_sequence, auto ring disabled, Caller ID

The following chart and diagram show a not successful flow of a ring-event detection because of no 2. ring with no automatic power mode change (No_auto_ring = 0, Caller_en = 1, RM = 1).



Line:	on hook	1st ring	on hook	caller ID	on hook
Mode:	sleep	ringing			
Interrupts:		VDD_ok ring	VDD_ok	Caller_ID	
Host CMDs:		ring mode			
		poll RMR			

Figure 28: not successful Ring sequence, No_auto_ring = 1; Caller_en = 1

Note: Cadence time and number of rings must be calculated by the host.

9.8.9 Not successful Ring_sequence, auto Ring enabled

The following chart and diagram shows a not successful flow of a ring-event detection because below the ring threshold level ring with automatic power mode change (No_auto_ring = 0, RM = 1).

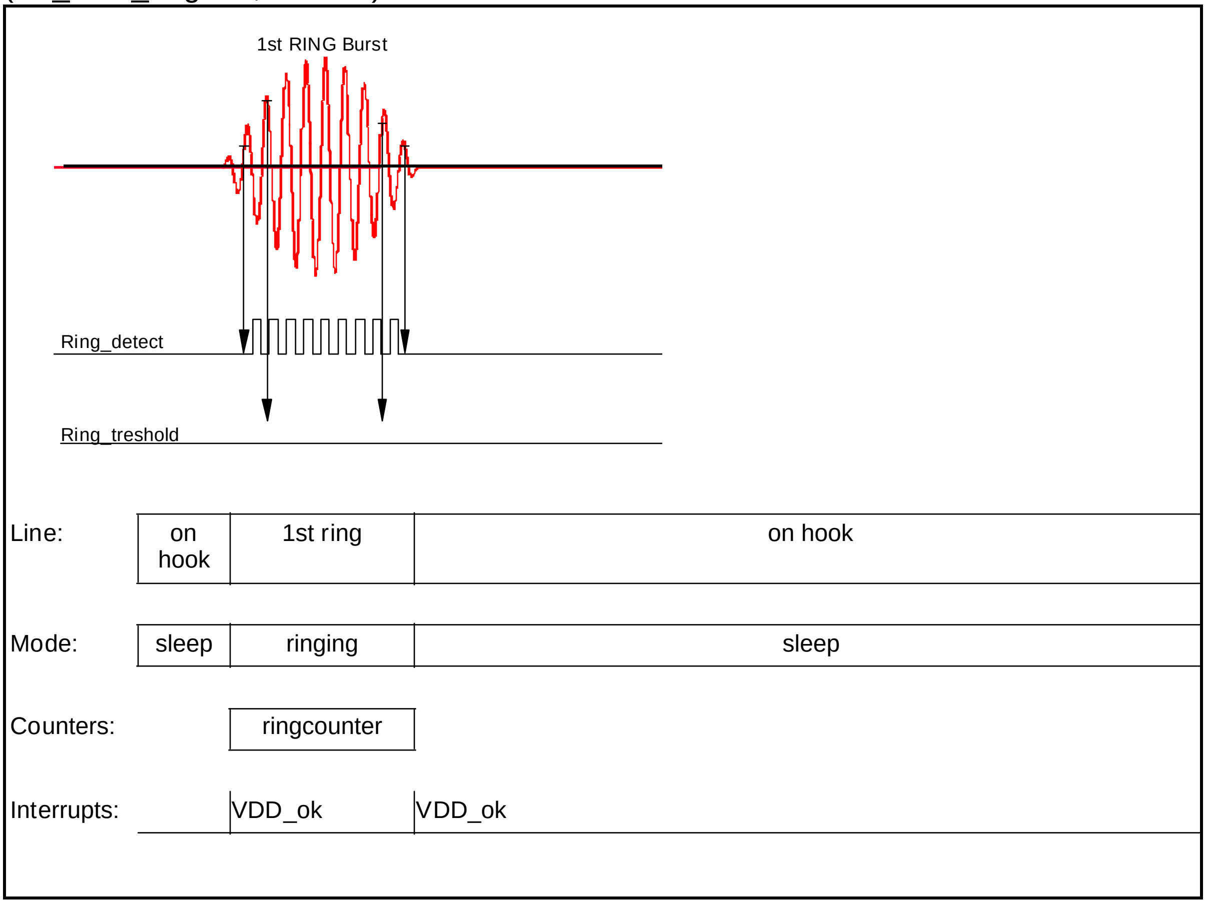


Figure 29: not successful Ring sequence, No_auto_ring = 0;

9.8.10 Not successful Ring_sequence, auto Ring disabled

The following chart and diagram show a not successful flow of a ring-event detection because ringing is below the ring threshold level ring with no automatic power mode change (No_auto_ring = 1, RM = 1).

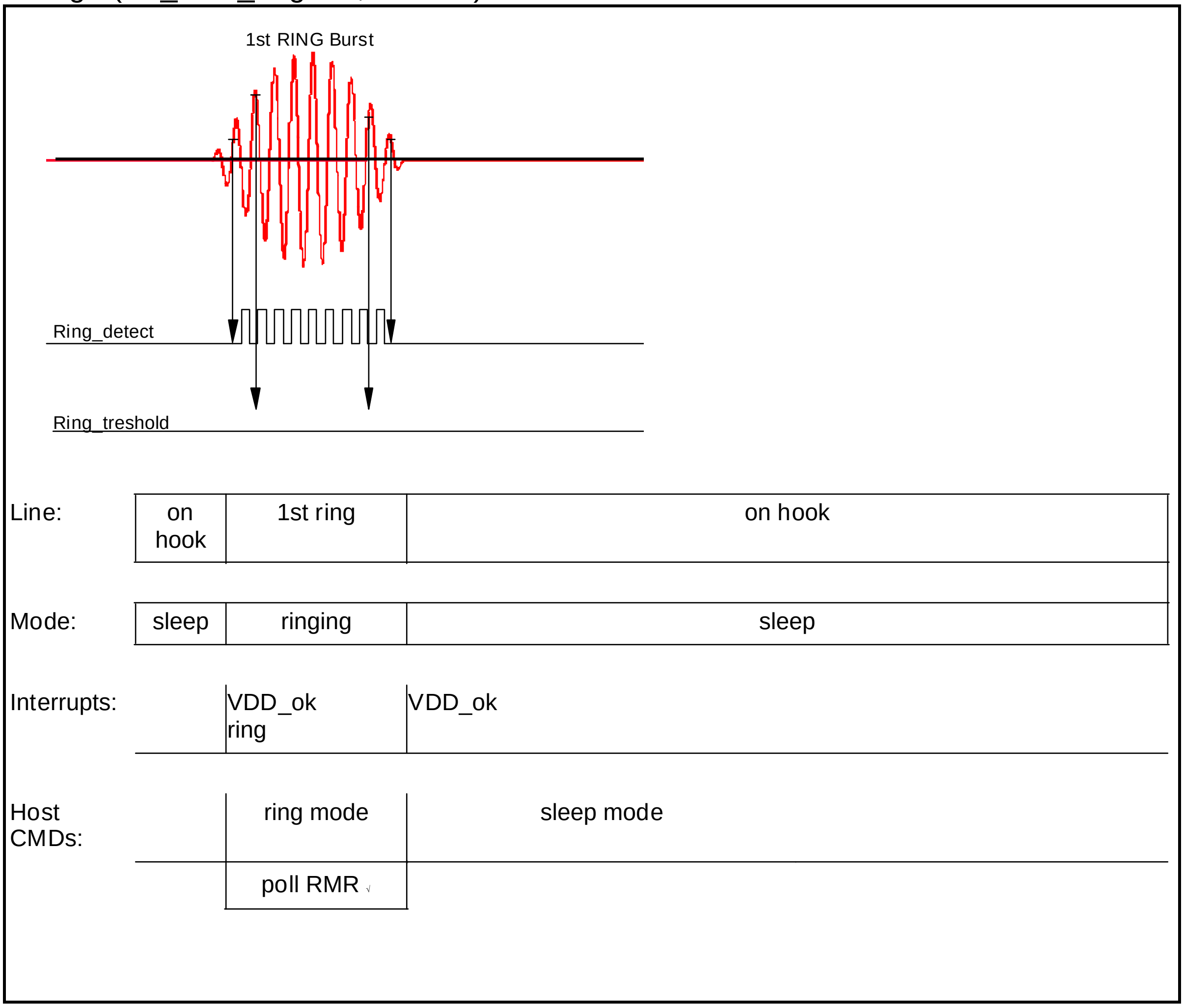
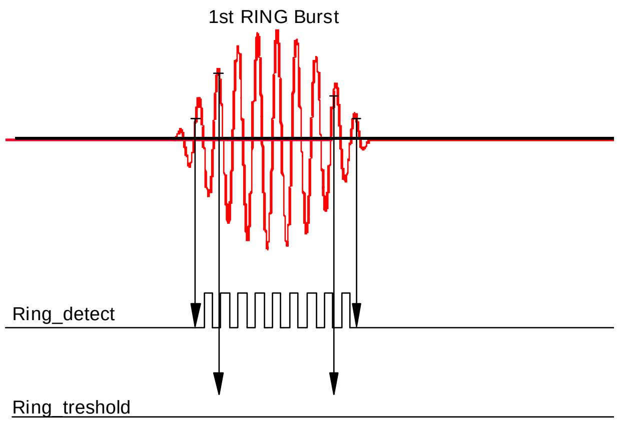


Figure 30: not successful Ring sequence, No_auto_ring = 0;

Note: RMR will not be '1'

9.8.11 Start from deep sleep mode

The following chart and diagram show a start-up procedure from deep sleep mode.



Line:	on hook	1st ring	
Mode:	deep sleep		
Interrupts:		Wake_up	
Host CMDs:		enable MCLK on board any power mode set CLK_OFF = 0	

Figure 31: deep sleep start

Note: after the wake_up interrupt any power mode and operation flow according to the previous chapters can be programmed.

10 Modem Functions

10.1 Pulse Dialing

Pulse dialing will be realized by shortening the line with the external transistor T1. Pulse timing has to be controlled by the host. Pulse shaping is realized in ALIS_A, the pulse shaping will conform to ETS 300 001

10.2 DTMF Dialing

DTMF Dialing is realized by two internal tone generators (See “Programming the ALIS DTMF Tone Generators” on page 75). Since the level of tone generator 2 is 3 dB higher

than that of tone generator 1, it should be used for the high frequency group. The frequency accuracy of the tone generators is better than ±1%. The absolute transmission level can be programmed using the AX filter. Software for computing the coefficients is available.
The tone generators can also be used to generate any inband sinewave for test or measurement purposes.

10.2.1 Programming the ALIS DTMF Tone Generators

Two independent tone generators are available. When one or both tone generators are turned on the voice signal is switched off automatically. To make the generated signal suitable for DTMF a programmable bandpass-filter is included. The default frequency for both tone generators is 2000Hz. Coefficients for other frequencies are generated by a software tool.

Byte sequences for programming both tone generators and the bandpass filters:

Frequency	Command	Byte 1	Byte 2	Byte 3	Byte 4
697 Hz	0B *)	11	B3	5A	2C
770 Hz	0B *)	12	33	5A	C3
852 Hz	0B *)	13	3C	5B	32
941 Hz	0B *)	1D	1B	5C	CC
1209 Hz	0C *)	32	32	52	B3
1336 Hz	0C *)	EC	1D	52	22
1477 Hz	0C *)	AA	AC	51	D2
1633 Hz	0C *)	9B	3B	51	25

*) 0B is used for programming Tone Generator 1
0C is used for programming Tone Generator 2

Table 7: Programming the Tone generators

The sinewave will be filtered by a bandpass, the Q factor of this bandfilter can be altered in the range from 0 to 7 and can be programmed by setting the first nibble of byte 3 to the corresponding value (always 5 in this table). The resulting signal amplitude can be set by programming the AR1 and AR2 filters.

10.3 Caller ID

The Caller ID interface is compatible to the Bellcore TR-NWT-000030 and SR-TSV-002476 on generic requirements for transmitting asynchronous voiceband data to Customers Premises Equipment (CPE) from a serving Stored Control Switching System (SPCS) or a Central Office (CO). In this service, the information about the calling party is embedded into the silent interval between the first and the second ring. During this period ALIS receives and stores up to 4096 bits of the 1200 baud FSK signal. The decoding matches as well BELL 202 and CCITT V.23 specifications. (See “Programming the ALIS Caller ID coefficients” on page 77)

10.3.1 Characteristics for Caller ID

Parameter	Sym bol	Limit Values			Unit	Reference
		min	typ	max		
Input detection level	Vin	-36 12.3		-9 275	dBm mV	
Detect frequencies Bell 202 1 (Mark) Bell 202 0 (Space) CCITT V.23 1 (Mark) CCITT V.23 0 (Space)		 1188 2178 1280.5 2068.5	 1200 2200 1300 2100	 1212 2222 1319.5 2131.5	 Hz Hz Hz Hz	 Bell 202 CCITT V.23
Input Noise Tolerance	SNR	20			dB	
Input Baud Rate		1188	1200	1212	Hz	

Table 8: Characteristics for Caller ID

10.3.2 Storage and reading of Caller ID

The storage of the decoded Caller ID is enabled after the first space following the mark state. This event will be indicated by the Caller ID interrupt. The maximimum storage size is 4096 bits. Start, stopbit and checksum decoding must be done by the host.

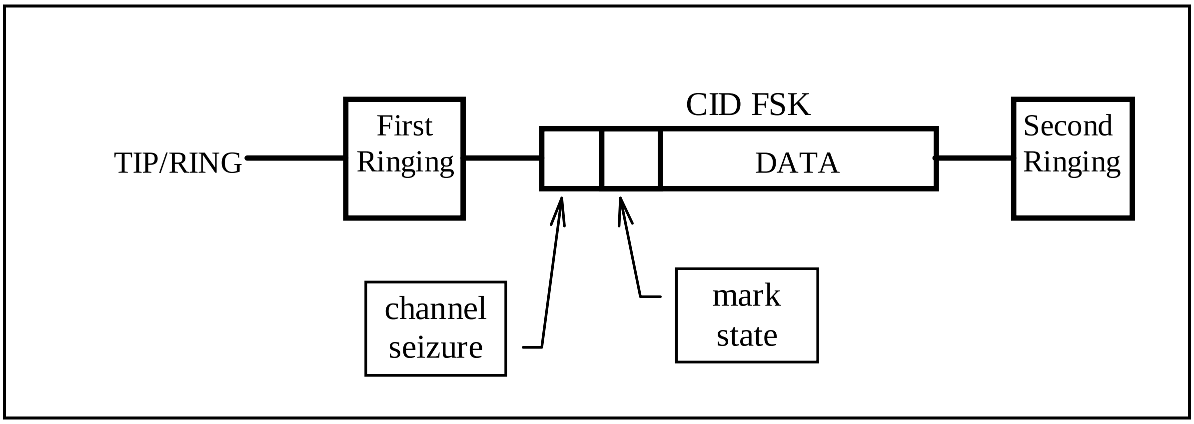


Figure 32: CID Input timing

When reading the ram with the CAO command the received bits will be sent from ALIS in the following order:

b0 is the first caller- ID data bit after the ‘0’ which is ending the marker sequence, b1 the second, b2 the third etc. ...

The host can read the caller- ID RAM at any time. Note that the read data may be erroneous when caller-ID data is received at the same time as old and new data might be mixed. However the received caller-id bits are stored correctly in the ram!

-> Try not to read the ram during caller-id is received!

10.3.3 Programming the ALIS Caller ID coefficients

Frequency	Command	Byte 1,2	Byte 3,4	Byte 5,6	Byte 7,8
BELL 202 / CCITT V.23	0E (CID1)	CA 0E	CA 09	99 99	99 99
	0F (CID2)	FD B5	BA 07	DA XX	XX XX

Table 9: Programming the ALIS Caller ID coefficients

10.4 Billing pulse

Billing pulse frequencies of 12 and 16 kHz will be filtered out by the digital part of ALIS, there are no external components for blocking necessary.

10.5 Ring Detect

10.5.1 Functional description

In Sleep Mode any signal greater then typical 18 volts will be detected. Depending on the No_auto_ring bit either an interrupt will occur or ALIS will be switched automatically into the Ringing Mode. In this mode the Ring Signal will be handed over to ALIS_D and decoded. If the Ring Burst does not meet the programmed requirements within a programmable time ALIS will return to the Sleep Mode. After a latency time ALIS will decode the Caller ID. When the second valid Ring Burst occurs a Ring interrupt is generated, signalling the incoming call to the host (see See “Flow of Ring sequence and detection” on page 62)

10.5.2 Programming the ALIS Ring Detect Coefficients

Frequency	Command	Byte 1	Byte 2	Byte 3	Byte 4
25 Hz 70Vrms 10 kΩ 1.0 µF	0D	AA	05	0F	8E
	Command	**Byte 1,2**	**Byte 3,4**	**Byte 5,6**	**Byte 7,8**
	03	1C B3	AB AB	54 2D	62 2D
	06	2D 62	A6 BB	2A 7D	0A D4

Table 10: Programming ALIS Ring Detect coefficients

Frequency	Command	Byte 1	Byte 2	Byte 3	Byte 4
50 Hz 50Vrms 10kΩ 0.6 µF	0D	22	15	B5	84
	Command	**Byte 1,2**	**Byte 3,4**	**Byte 5,6**	**Byte 7,8**
	03	1C A4	AA AB	BD 2B	A2 2D
	06	2B A2	A6 BB	2C 63	3A D4

Table 11: Programming ALIS Ring Detect coefficients

10.5.3 Ring Threshold in Sleep Mode

Parameter	Symbol	Limit Values			Unit	Reference
		min	typ	max		
Ring Threshold			12	18	Vrms	

Table 12: Ring Threshold in Sleep Mode

11 Electrical Characteristics

11.1 Programmable Filters

A set of programmable filters are used to adapt the whole system to:

- country standards
- board designs (EMI capacitors etc.)
- data pumps
- telephone lines

Note: All this coefficients will be computed by a coefficient program. Any change of these computed values may case a loss of performance or instability.

In detail the following filters are programmable:

- Transhybrid Balancing (TH)-Filter
- Transhybrid Prebalancing
- Impedance Matching (IM)-Filter
- Frequency Response Receive (FRR)-Filter
- Frequency Response Transmit (FRX)-Filter
- Ringer Impedance

Amplification/Attenuation Transmit (AX)-Filter

Gain for AX-Filter

range 3.. -14 dB: step size 0.02 .. 0.05 dB

range -14 .. -24 dB: step size 0.5 dB

Gain for AGX

range 3.5, 0 -2.5, -6

Amplification/Attenuation Receive (AR)-Filter

Gain for AR-Filter

range -3 .. 14 dB: step size 0.02 .. 0.05 dB

range 14 .. 24 dB: step size 0.5 dB

Gain for AGR_R:

range 0, 3.5, 6 dB

Gain for AGR_Z:

range -3.5, 0, 2.5, 6 dB

11.2 DC Characteristics

The Filtercoefficients are generated by a softwaretool including a high level model of ALIS and additional, user defined or application specific system components.

11.2.1 DC Termination

The DC termination is enabled in Conversation mode and disabled during Ringing Mode, Pulse Dialing Mode and Sleep Mode. The DC Termination can be programmed according the formula:

for i < Imax

$$i(u) = \frac{(u - Uo)}{R}$$

for i > Imax

$$i(u) = Imax$$

Note: U_0 is the sum of U listed in table 14 and the flow voltage of the diodes in the external bridge (typ. 2 x 0.4 V)

11.2.2 Programming ranges for DC Termination

Imax
50 mA
100 mA

Table 13: Programming range for Imax

U (DCU)
0 V
1.5 V
3.5 V
7.2 V

Table 14: Programming range for U

R (DCR)
70 Ω

100 Ω
200 Ω
240 Ω
280 Ω

Table 15: Programming range for R

Note: for programming details see See “XR3 Extended Register 3 (DC Characteristic)” on page 46

11.2.3 Input Current in Pulse Dialing Mode

Uab = 30 V DC

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Input current at break	Iin			500	µA

Table 16: Input current in pulse dialing

11.3 AC Termination

11.3.1 Ringer Impedance

The programming of the Ringer Impedance is supported by a software tool and the following table shows typical values.

Uab = 70 Vrms

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Ringer Impedance (20 Hz < f <60 Hz)[1)]	Rin		10		kΩ
	Δ Rin			tbd	%
Typical capacitors	Cin1		0.6		µF
	Cin2		1		µF
	Δ Cin			tbd	%
Ringer Impedance in other modes[2)]					

1) The frequency range can be changed

2) Ringer impedance is generated only in ring mode

Table 17: Ringer Impedance

11.4 ALIS Caller ID Interface

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Capacitance	Cin		50		nF
Tolerance between Cin1 and Cin2				tbd	%
Rin	Rin		50		kΩ
Tolerance between Rin1 and Rin2				tbd	%
Rfb	Rfb		200		kΩ
Tolerance between Rfb1 and Rfb2				tbd	%

Table 18: ALIS Caller ID interface

11.4.1 Ring Detect Levels and Frequencies

.

Parameter	Symbol	Limit Values			Unit	Tolerance
		min	typ	max		
Ring level detection program range	Vring	30		100	V	±10%
Ring level detection step size	Δ Vring			10	V	±10%
Ring Frequency detection program range[1)]	Fring	20		60	Hz	±10%

1) The exact range depends on the level programmed for detection

Table 19: Ring detect levels and frequencies

11.5 ALIS Cap Interface

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Capacitance	Cin	5	10	30	pF
Tolerance between CAP_x1 and CAP_x2				5	%
Inductance				10	nH
Isolation	tbd.				kV

Table 20: ALIS Cap interface

12 Electrical Performance Characteristic

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		Min	Max	
Digital Supply Voltage	VDD	-0.3	7.0	V
Analog Supply Voltage	VDDA	-0.3	7.0	V
Analog Input and Output Voltage	Vin, Vout	-0.3	VDDA + 0.3	V
Digital Input Voltages	VDin	-0.3	VDD + 0.3	V
DC Input and Output Current	Iin, Iout	-10	10	mA
Storage Temperature	TST	-60	125	°C
Ambient Temperature under Bias	TA	-10	80	°C
Max. Power Dissipation	PDmax		1	W

Note: Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and effect reliability.

Table 21: Absolute Maximum Ratings

12.2 Recommended Operating Conditions

Parameter	Symbol	Conditions			Unit
		Min	Typ	Max	
Digital Supply Voltage	VDD	4.75	5.0	5.25	V
Analog Supply Voltage ALIS_A (programmed to 4.25 V)	VDDA	4.00	4.25		V
Analog Supply Voltage ALIS_D	VDDA	4.75	5.0	5.25	V
Ambient Temperature under Bias	TA	0		70	°C
Operating Frequency	fclk		16.384	tbd.	MHz
Clock Duty Cycle		45	50	55	%
Signal Rise and Fall Time	tr, tf			20	ns

Note: Extended operation outside the recommended limits may degrade performance and effect reliability.

Table 22: Recommended Operating Conditions

12.3 DC Characteristics

12.3.1 ALIS_A

VDDA= 4.25V progr.; TA=0 - 70°C

Parameter	Symbol	Conditions	Spec. Limits			Unit
			Min	Typ	Max	
Power-Up Time	tPU	tbd			tbd	ms
VDDA Supply Current[1)]						
Ringing Mode[2)]	IDDA1	Vring=60V DC + 90Vrms, fring=25 - 50Hz		2.5	tbd	mA
Conversation Mode[3)]	IDDA2	fCLK=16.384MHz		7	tbd	mA
Pulse Dialing Mode	IDDA3	Vab=30 V DC			500	µA
Digital Interface						
Low-Level Input Voltage	VIL[4)]				0.8	V

High-Level Input Voltage	VIH[4)]		2.0			V
Low-Level Output Voltage	VOL[5)]	IOL=5mA			0.5	V
High-Level Output Voltage	VOH[5)]	IOH=-5mA	3.5			V
Input Current Low	IIL	VIL=GNDA			±1	µA
Input Current High	IIH	VIH=VDDA			±1	µA
Input Resistance						
Sleep Mode	Rin	@100 V DC	1			MΩ
Conversation Mode	Rin	see 10.2.3				Ω
Pulse Dialing Mode	Rin	Interpulsing Period (Make)			200	Ω
Ring Threshold	VRThresh	VDDA=4.25V ext.			15	VRMS
Power Supply Rejection	PSRR	Ripple: 0-150kHz; 70mVrms				
either supply/direction		300Hz - 3.4kHz	tbd			dB
VDD receive guaranteed		3.4kHz - 150kHz	tbd			dB
VDD receive Target		3.4kHz - 150kHz	tbd			dB

1) Will be taken from TIP/RING when the hook switch is open

2) in Ringing mode the ringer impedance will be synthesized. Therefore a current according to this impedance will flow from TIP/RING. This current is taken out of the ring burst as an ac current.

3) in Conversation mode the DC characteristic will be syntesized and a current according to this characteristic will flow from TIP/RING.

4) Digital Inputs: Test, SI_0, SI_1

5) Digital Outputs: SO_0, SO_1Q

Table 23: DC Characteristics ALIS_A

12.3.2 ALIS_D

VDD = VDDA= 5V± 5%; TA=0 - 70°C

Parameter	Symbol	Conditions	Spec. Limits			Unit
			Min	Typ	Max	
Supply Current		VDD=5V, no loads				
Deep Sleep Mode	IDD0				tbd	µA
Sleep Mode	IDD1			1	1	mA
Ringing Mode	IDD2			3	3	mA
Conversation Mode	IDD3			10	15	mA
Pulse Dialing Mode	IDD4			10	15	mA
Low-Level Input Voltage	VIL1[1)] VIL2[2)] VIL3[3)]				0.8 1.5 1.5	V
High-Level Input Voltage	VIH1[1)] VIH2[2)] VIH3[3)]		2.0 3.5 3.5			V
Low-Level Output Voltage	VOL[4)]	IOL=5mA			0.5	V
High-Level Output Voltage	VOH[4)]	IOH=-5mA	VDD-0.5			V
Input Current Low	IIL[1,2)]	VIL=GND			±1	µA
Input Current High	IIH[1,2)]	VIH=VDD			±1	µA
Tristate Current Low	IOZL[5)]	VIL=GND			±1	µA
Tristate Current High	IOZH[5)]	VIH=VDD			±1	µA

1) TTL Inputs: DCLK, CS, DIN, DAT_CLK, DAT_IN, MODE, FSC

2) CMOS Input: RESET

3) Clock Input: MCLK1

4) Outputs: DOUT, INT, DAT_OUT, FSC

5) Tristates, Bidirectionals: DOUT, FSC

Table 24: DC Characteristics ALIS_D

12.4 AC Transmission Characteristics

Unless otherwise stated, the transmission characteristics are guaranteed within the following test conditions:

TA=0 °C to 70 °C

VDD=5V ±5%

VDDA=4.25V (generated from ALIS_A)

Line impedance ZL = 600 ± 0.1% Ohms

Termination impedance ZM = 600 Ohms

digital: 0dBm0 = -3 dB FS

analog: 0 dBm is equal to the voltage of 0.775 Vrms when loaded with 600 Ohms

0 dBm = 0dBm0

f=1004Hz.

12.4.1 Absolute Gain Error

AGX=AGR=0 dB

Parameter	Symbol	Limit Values			Unit	Test condition
		min	typ	max		
Absolute gain error receive	AE_R					-10 dBm
TA=25 °C; VDDA=4.25V		-1	±0.5	+1	dB	
TA=0-70 °C; VDDA=4.25V		-1.2	±0.7	+1.2	dB	
Absolute gain error transmit	AE_X					-10 dBm0
TA=25 °C; VDDA=4.25V		-1	±0.5	+1	dB	
TA=0-70 °C; VDDA=4.25V		-1.2	±0.7	+1.2	dB	

Table 25: Absolute Gain Error

12.4.2 Gain Tracking

AGX=AGR=0dB

Parameter	Symbol	Limit Values			Unit	Test condition
		min	typ	max		
Gain tracking receive	GT_R	-0.15		0.15		0 to -10 dBm
		-0.15		0.15		-30 to -40 dBm
		-0.3		0.3		-40 to -50 0.dBm
Gain tracking transmit	GT_X	-0.5		0.5		0 to -10 dBm0
		-0.1		0.1		-10 to -40 dBm0
		-0.5		0.5		-40 to -50 dBm0

Table 26: Gain Tracking

12.4.3 Harmonic Distortion plus Noise

-10 dBm0; ZL= 600 Ω; f=1004 Hz

Parameter	Symbol	Limit Values			Unit	Test condition
		min	typ	max		
HDN receive	THD+N_R	tbd	tbd		dB	C-weighted
HDN transmit	THD+N_T	tbd	tbd		dB	
HDN receive		tbd	tbd		dB	linear-weighted
HDN transmit		tbd	tbd		dB	
HDN of echo signals via TIP/RING		tbd	tbd		dB	C-weighted[1)]

1) measured with digital loop back via TIP/RING

Table 27: Harmonic Distortion plus Noise

12.4.4 Harmonic Distortion

-10 dBm0; ZL= 600 Ω; f=1004 Hz, 2nd and 3rd Harmonic

Parameter	Symbol	Limit Values			Unit	Test condition
		min	typ	max		
HD of echo signals via TIP/RING		80			dB	linear-weighted[1)]

1) measured with digital loop back via TIP/RING

Table 28: Harmonic Distortion

12.4.5 Return Loss

The return loss at a level of 0 dBm0, will be better than 16 dB in a 300-3600 Hz bandwidth using the following set of defined impedances

600 Ohms

220 Ohms + (820 Ohms in parallel with 115 nF)

120 Ohms + (820 Ohms in parallel with 110 nF)

370 Ohms + (620 Ohms in parallel with 310 nF)

12.4.6 Frequency Response

12.4.6.1 Receive

Reference frequency 1kHz, input signal level 0dBm0

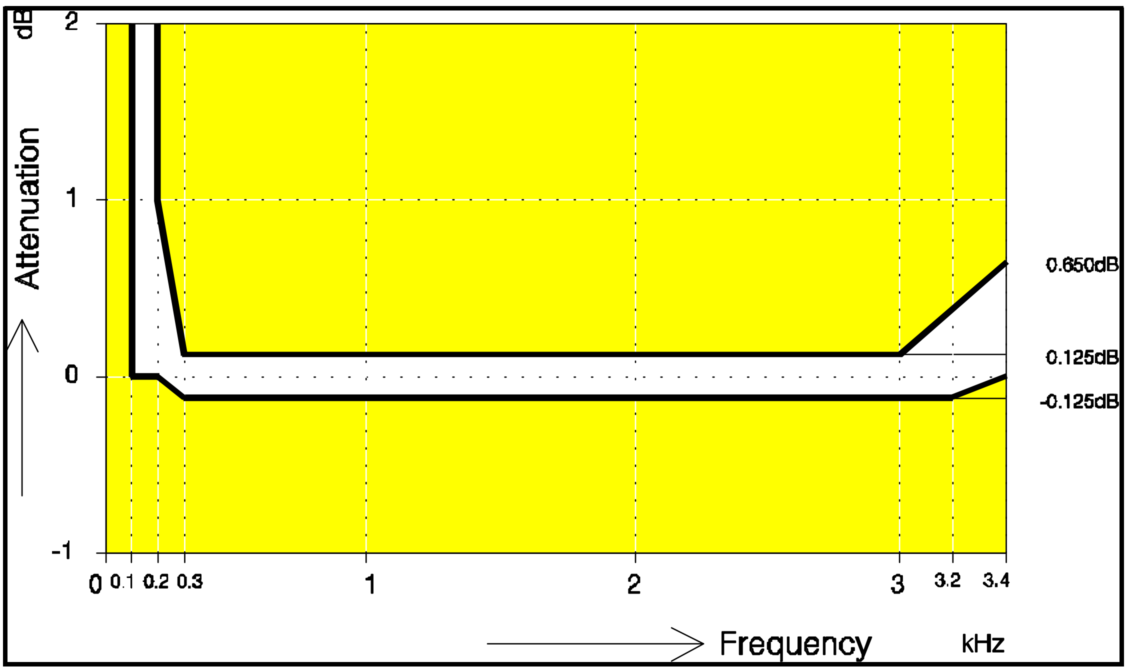


Figure 33: Frequency Response Receive

12.4.6.2 Transmit

Reference frequency 1kHz, input signal level 0dBm0

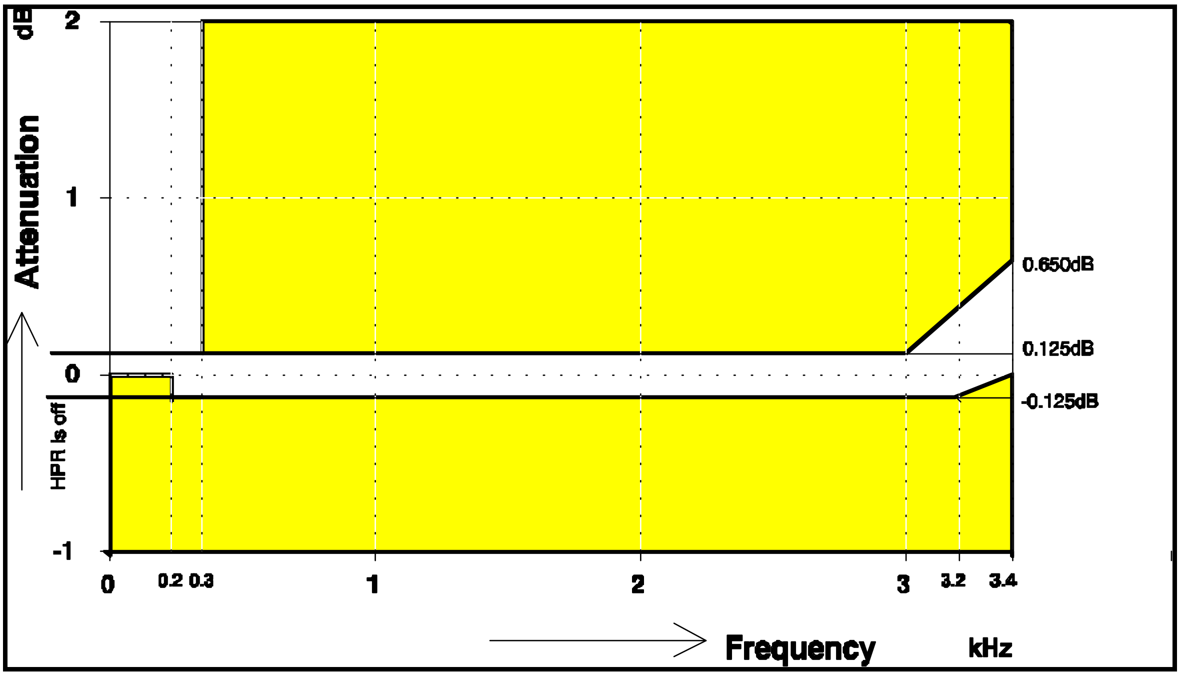


Figure 34: Frequency Response Transmit

12.4.7 Group Delay

Maximum delays when ALIS is operating with H(TH)=H(IM)=0 and H(FRR)=H(FRX)=1 including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group Delay deviations stay within the limits in the figures below.

12.4.7.1 Group Delay Absolute Values

Parameter	Symbol	Limit Values			Unit	Reference
		min	typ	max		
Receive delay	DRA			340	µs	Input signal level 0 dBm0
Transmit delay	DXA			400	µs	

Table 29: Group Delay

12.4.7.2 Group Delay Distortion Receive

Input signal level 0dBm0

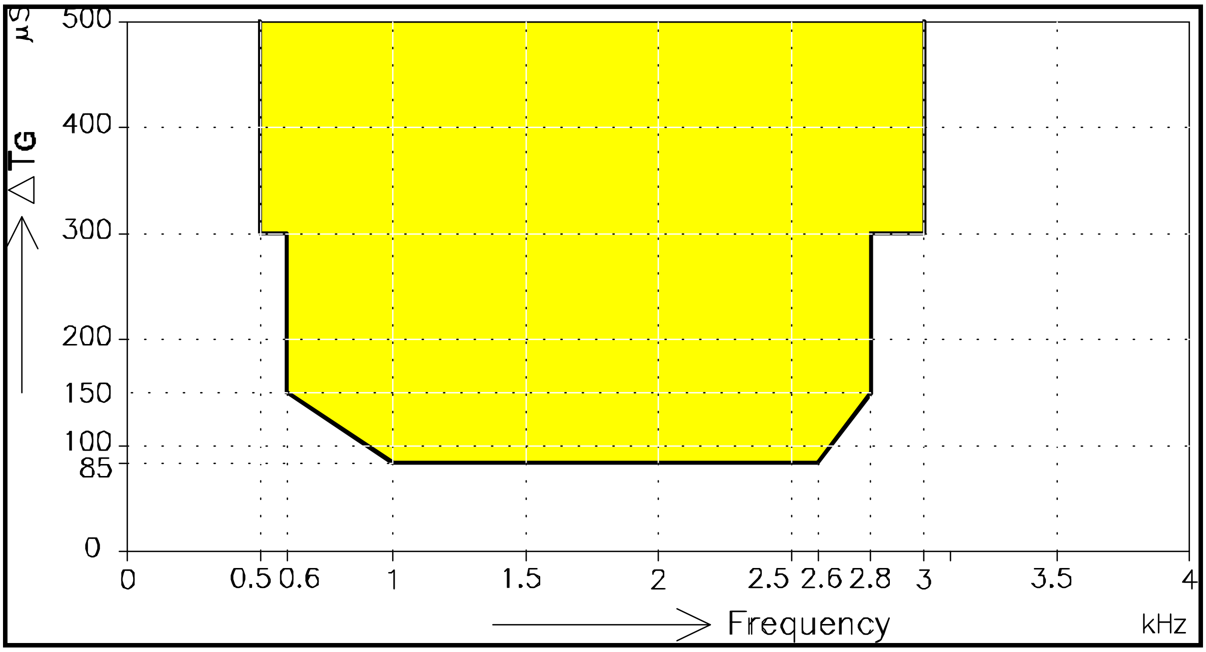


Figure 35: Group Delay Distortion Receive

12.4.7.3 Group Delay Distortion Transmit

Input signal level 0dBm0 [1])

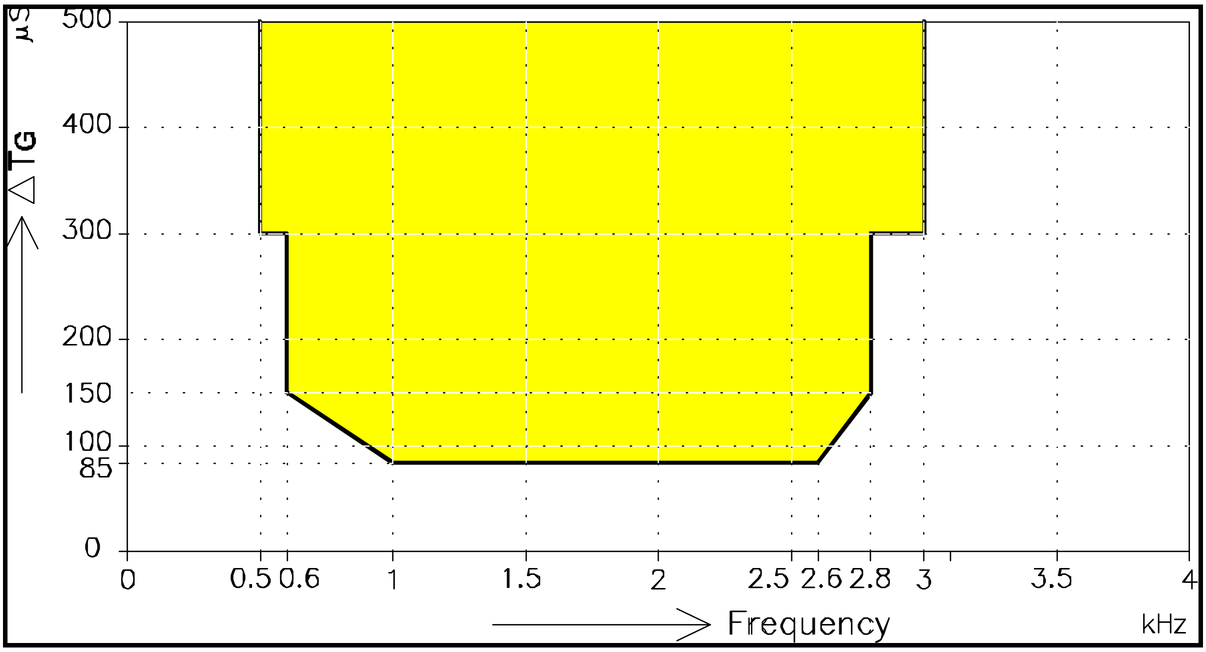


Figure 36: Group Delay Distortion Transmit

12.4.8 Out-of-Band Signals at TIP/RING Receive

With an 0dBm0 out-of-band sine wave signal with a frequency of (<<100Hz or 3.4kHz to 100kHz) applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0dBm0, 1kHz sine wave reference signal at the analog input.[2])

[1] R is switched on: reference point is at TGmin
HPR is switched off: reference point is at 1.5 kHz
[2] Poles at 12 kHz ± 150 Hz and 16 kHz ± 150 Hz will be provided

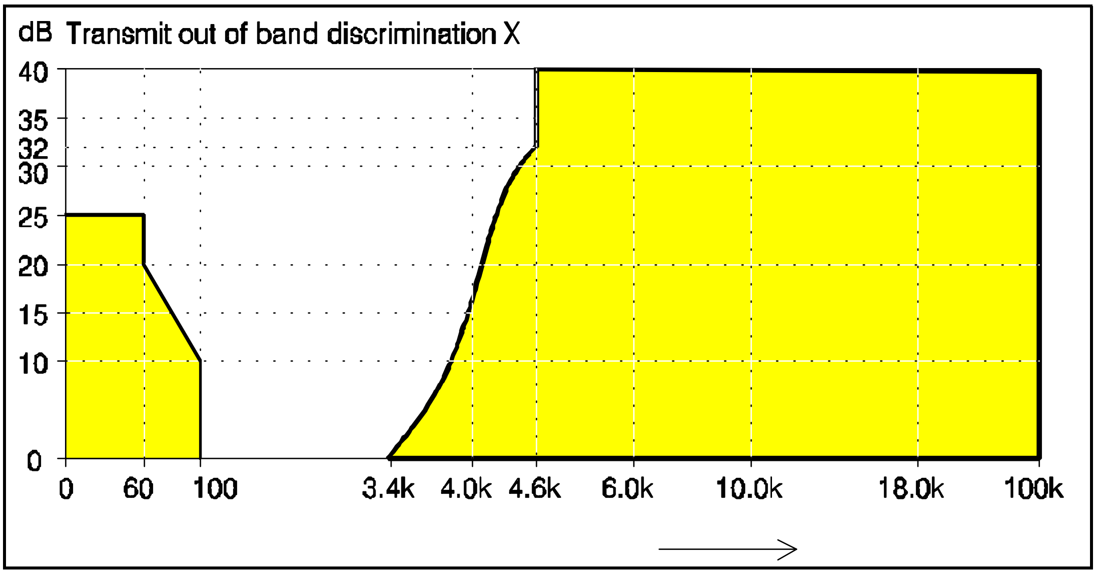


Figure 37: Out of Band Receive

12.4.9 Out-of-Band Signals at TIP/RING Transmit

With a 0 dBm0 sine wave with a frequency of (300Hz to 3.99kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0 1 kHz sine wave reference signal at the analog output.

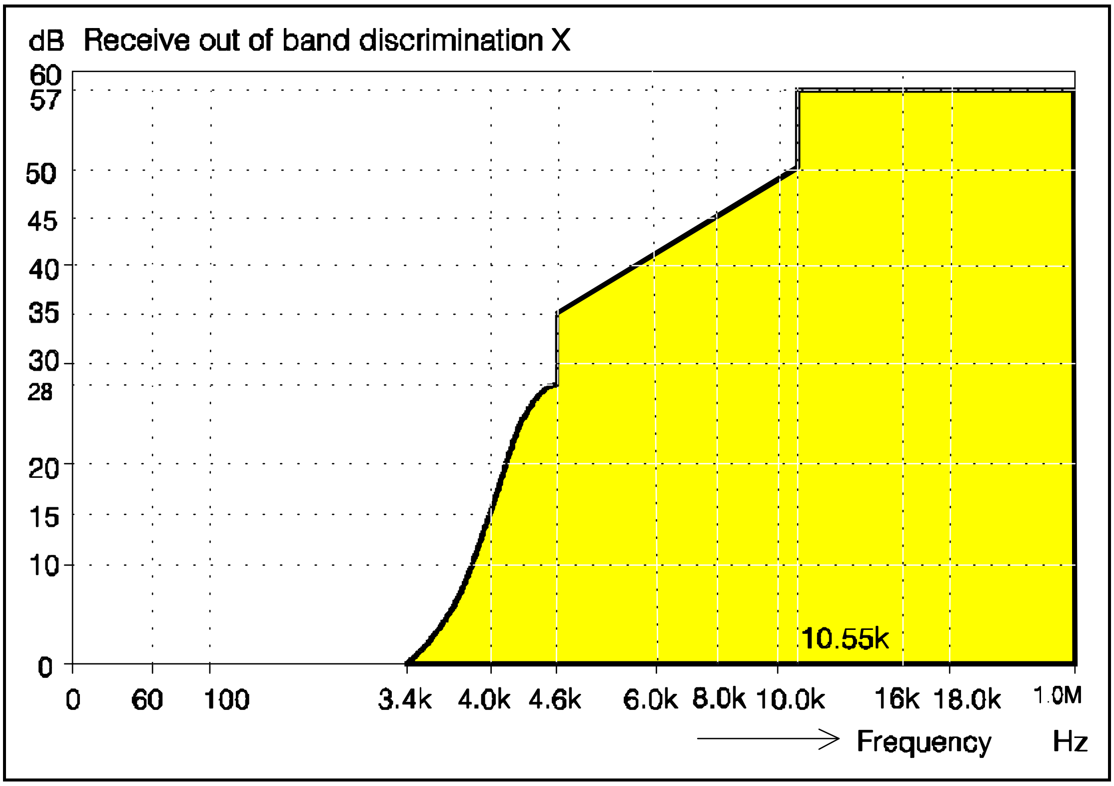


Figure 38: Out of Band Transmit

12.4.10 Transhybrid Loss

The quality of Transhybrid-Balancing is very sensitive to deviations in gain and group delay - deviations inherent to ALIS A/D- and D/A-converters as well as to all external components used.
Measurement of ALIS Transhybrid-Loss: A 0dBm0 sine wave signal and a frequency in the range between 300 - 3400 Hz is applied to the digital input. The resulting analog output signal VOUT at TIP RING is received and cancelled by the TH Filter. The programmable filters FRR, AR, FRX, AX and IM and the balancing filter TH is enabled with coefficients optimised.
The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below. (Filter coefficients will be provided)

Parameter	Symbol	Limit Values		Unit	Test condition
		min	typ		
Transhybrid Loss at					

300 Hz	THL 300	27	40	dB	TA=25° C; VDDA=4.25V;
500 Hz	THL 500	33	45	dB	
2500 Hz	THL2500	29	40	dB	
3000 Hz	THL3000	27	35	dB	
3400 Hz	THL3400	27	35	dB	

Table 30: Transhybrid Loss

The listed values for THL correspond to a typical variation of the signal amplitude and delay in the analog blocks.

Amplitude =typ. ±0.8 dB

Delay =typ. ±0.5 µs

12.5 AC Timing Characteristics

12.5.1 Input/ Output Waveform for AC Tests

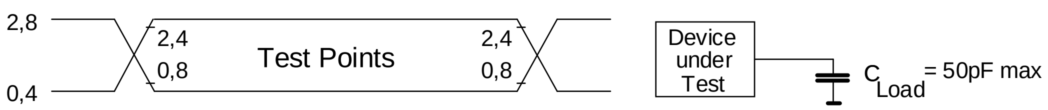


Figure 39: Waveform for AC Tests

12.5.2 Reset Timing

To reset ALIS to basic setting mode, negative pulses applied to the RESET pin have to be lower than 1.5 Volts (CMOS-Schmitt-Trigger Input) and longer than 500ns. Signals shorter than 100ns are ignored.

12.5.3 Control Interface Timing

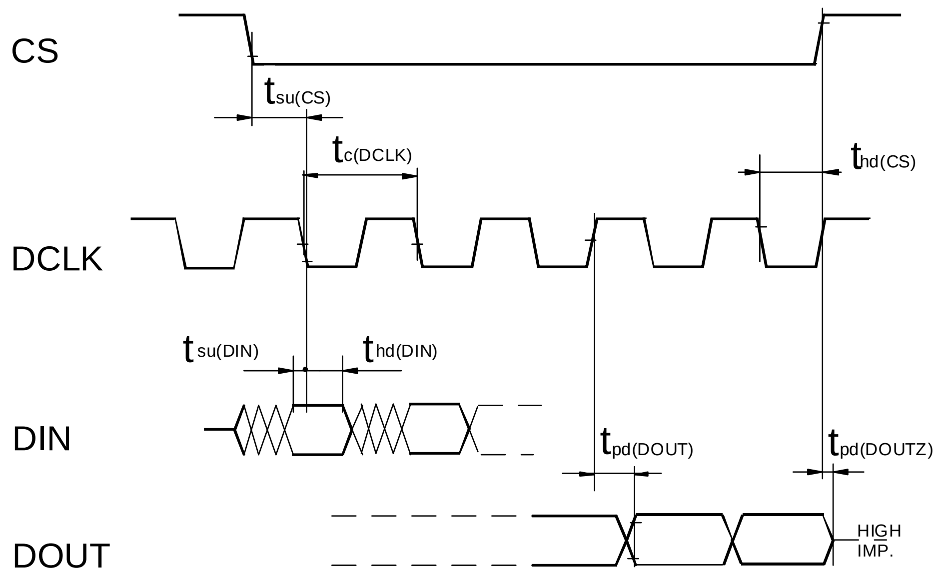


Figure 40: Control Interface Timing

VDD=VDDA= 5V± 5%; TA= 0 - 70°C

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Clock Cycle Time	tc(DCLK)	1/1024		1	ms
Clock Duty Cycle		45	50	55	%
Setup Time, CS↓ before DCLK↓	tsu(CS)	50			ns
Hold Time, CS↑ after DCLK↓	thd(CS)	50			ns
Setup Time, DIN before DCLK↓	tsu(DIN)	50			ns
Hold Time, DIN after DCLK↓	thd(DIN)	50			ns
Delay Time, DCLK↑, to DOUT	tpd(DOUT)			100	ns
Delay Time, CS↑ to DOUTZ	tpd(DOUTZ)			100	ns

Table 31: Control Interface Switching Characteristics

12.5.4 Data Interface Timing

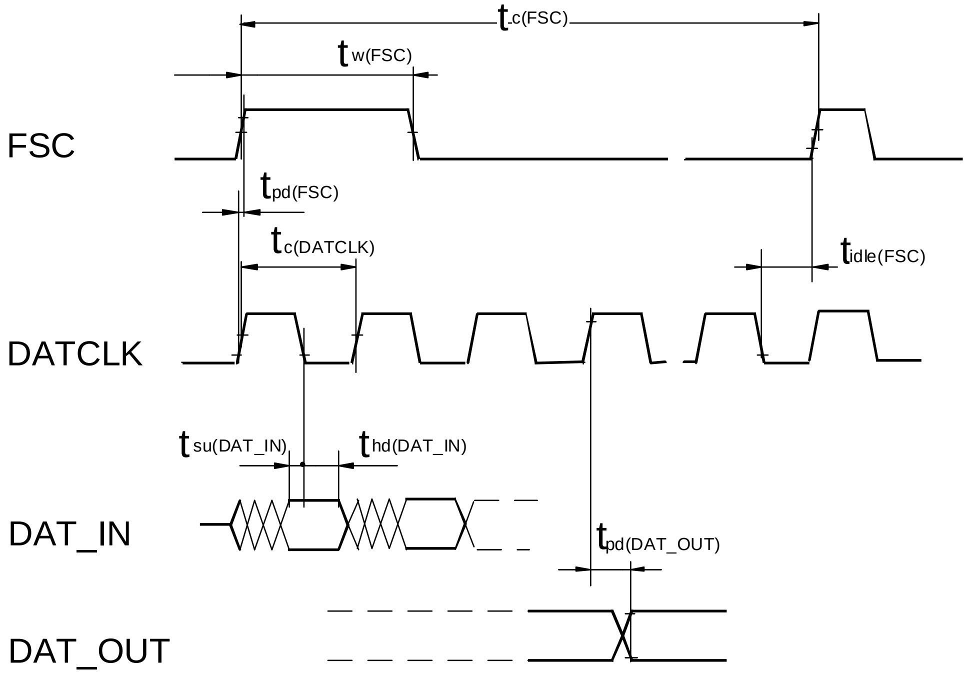


Figure 41: Data Interface Timing

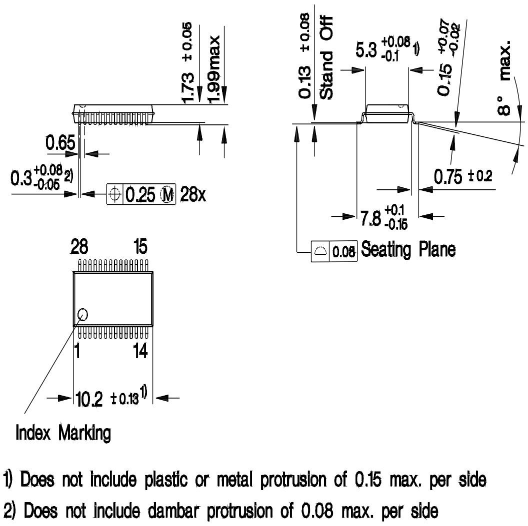
VDD=VDDA= 5V± 5%; TA=0 - 70°C

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Data Clock Cycle Time	tc(DATCLK)	1/ 1024		1/ 128	ms
Data Clock Duty Cycle		45	50	55	%
Frame Synch Clock Cycle Time	tc(FSC)		125		µs
FSC Pulse Width (as Input)	tw(FSC)	500			ns
FSC Pulse Width (as Output)	tw(FSC)		1.4		µs
Setup Time, DAT_IN before DATCLK↓	tsu(DAT_IN)	50			ns
Hold Time, DAT_IN after DATCLK↓	thd(DAT_IN)	50			ns
Delay Time, DATCLK↑ to DAT_OUT	tpd(DAT_OUT)			100	ns
Idle Time, DATCLK↓ to FSC↑	tidle(FSC)	488			ns
Delay Time, DATCLK↑ to FSC↑	tpd(FSC)	0			ns

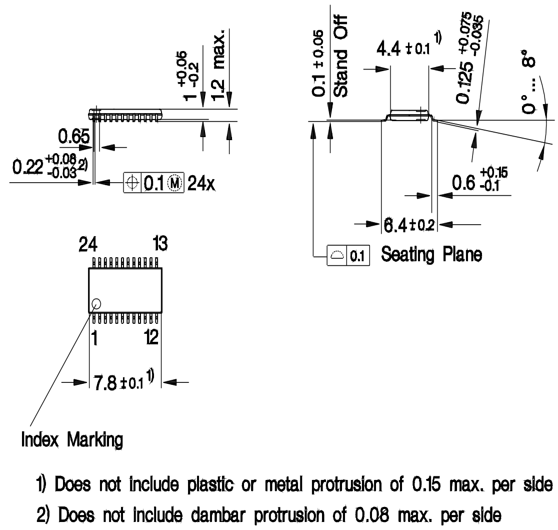
Table 32: Data Interface Switching Characteristics

12.5.5 CPackage Outlines

P-SSOP28
(Plastic Metric Quad Flat Package)



P-TSSOP24
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm