SIEMENS

ICs for Communications

Subscriber Access Controller for U_{pn}-Interface Terminals
SmartLink-P

PSB 2197

Addendum to User's Manual 08.95

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Subscriber Access Controller for U_{pn}-Interface Terminals SmartLink-P **PSB 2197**

This addendum contains additions to the User's Manual 02.95,
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1.1 Pin Definitions and Functions

Pin No.	TE-Mode		TR-Mode		HDLC-Controller Mode		Function
P-DSO-28	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	
2	$\overline{\text{RST}}$	I/O(OD)	$\overline{\text{RST}}$	I	$\overline{\text{RST}}$	I/O(OD)	**RESET.** Low active reset output and input (TE, HDLC, open drain output), low active reset input in TR mode.

Note: The possibility to use the undervoltage detection in HDLC controller mode is listed for completeness. The pulse width of the reset output in HDLC controller mode if the undervoltage detection is used is not specified in the electrical characteristics but may be as short as 200 ns.

If $\overline{\text{RST}}$ is configured as reset input, it must be driven to a valid V_{IL} during power-up.

The first note on page 14 is incorrect in regards to pin 7. All V_{DD} pins are internally connected via the chip substrate.

The second note on page 14 is for information only, and the series resistors referred to have no effect on the AC and DC characteristics shown in chapter 5**.**

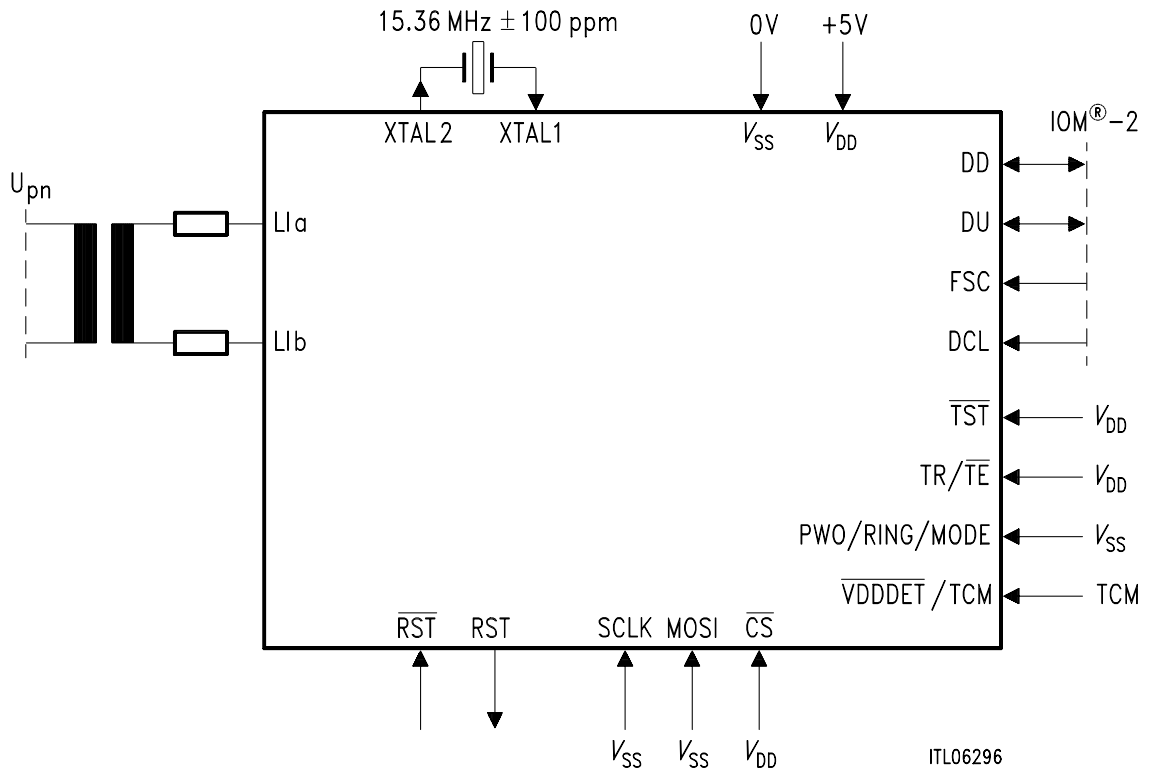


Figure 2
Logic Symbol of the SmartLink-P TR-Mode

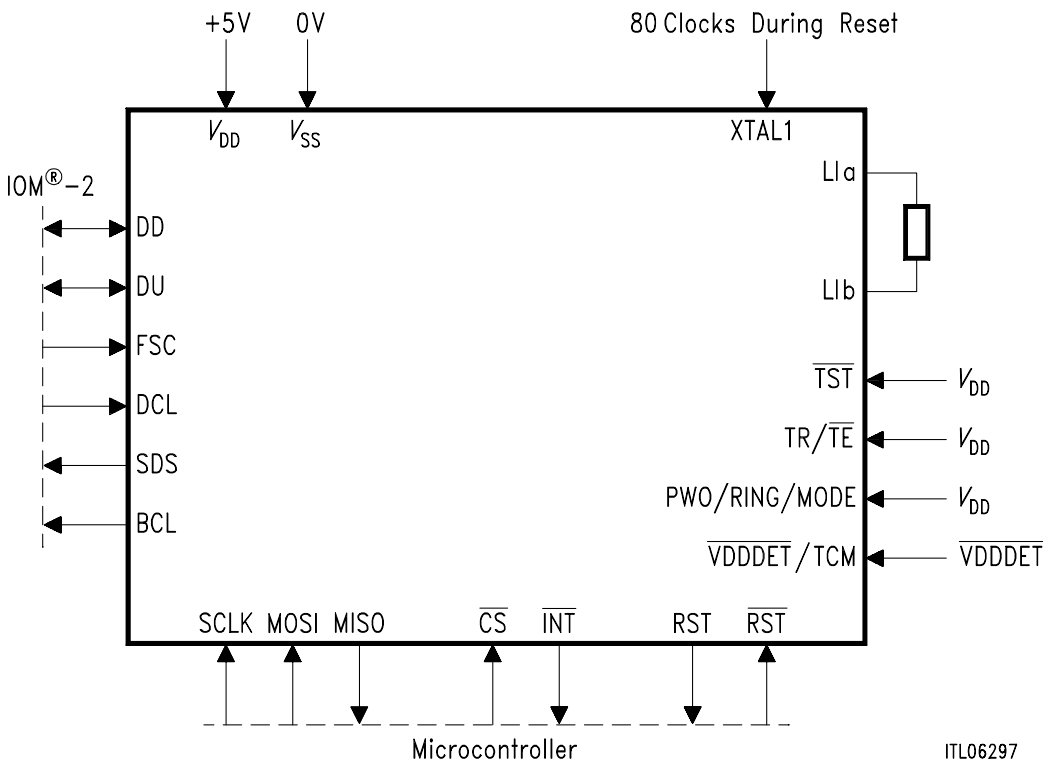


Figure 3
Logic Symbol of the SmartLink-P HDLC-Controller Mode

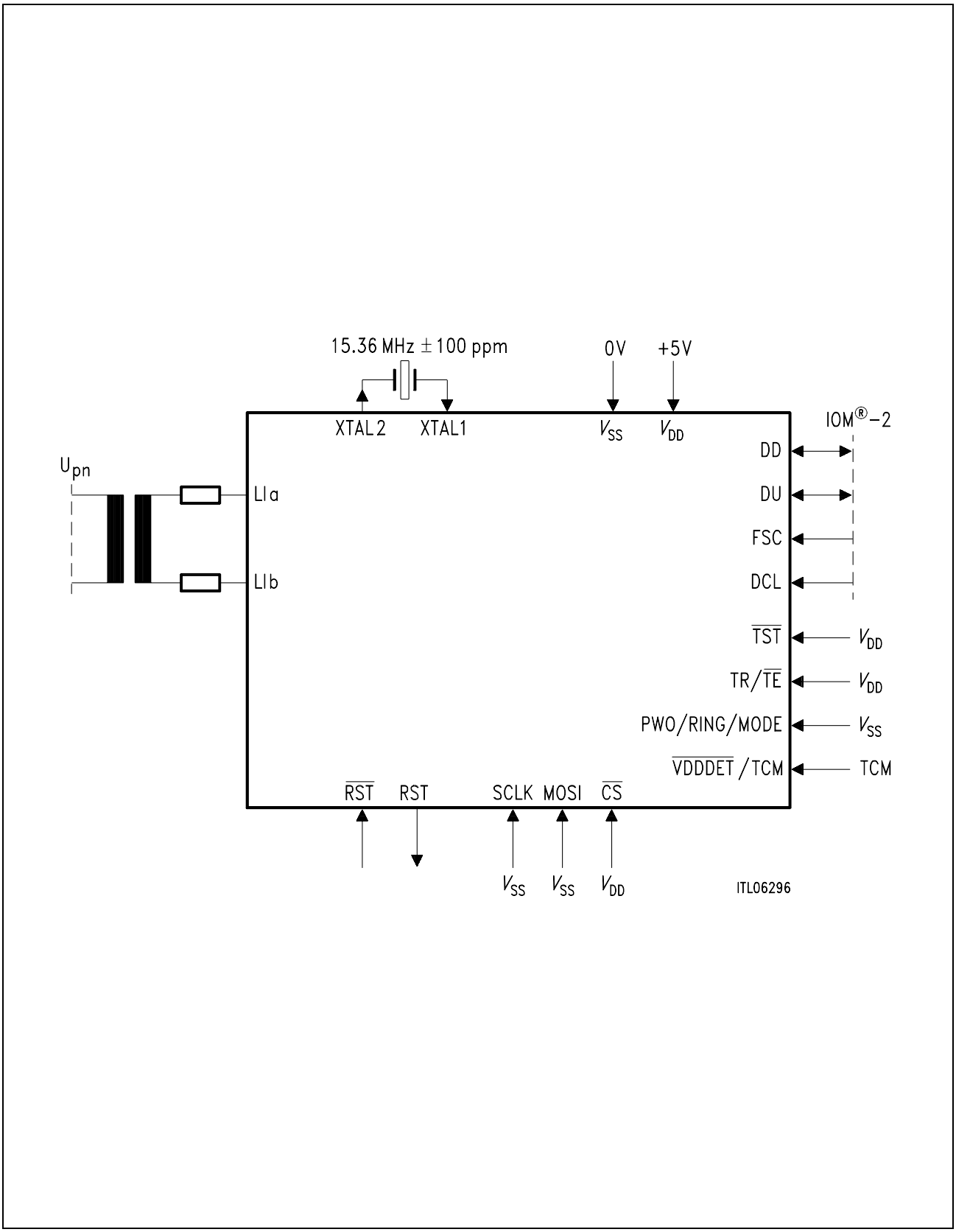
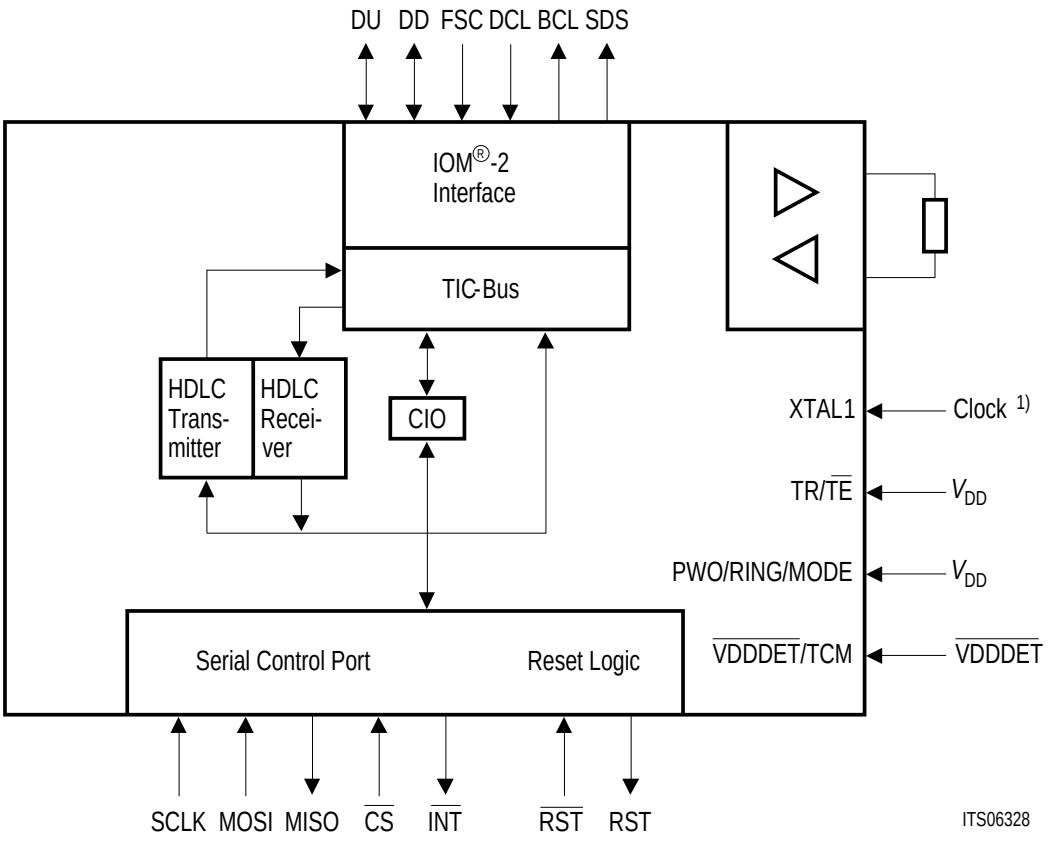


Figure 32
Device Architecture in TR Mode



1) Clocks required as specified in section 2.3.6.

Figure 38
Device Architecture of the SmartLink-P in HDLC-Controller Mode

2.1.2.1 Jitter (TE Mode)

Jitter on IOM®-2

The IOM-2 clocks are derived from a receive PLL which adjusts the clock to all pulses that are received. The receive PLL recovers bit timing from a comparator output signal. The comparator has a threshold of 80 % with respect to the signal stored by the peak detector. The RPLL adjust the IOM clocks by one oscillator period (65 ns) every four positive pulses that are offset in the same direction. At maximum four oscillator periods may be adjusted in one IOM-2 frame if every bit of the U_{pn} frame is a '1' (38 frame bits with every second positive pulse result in an average of 19 pulses, 19/4 = 4). Due to the scrambler it is very unlikely that continuous pulses occur, thus the actual adjustment will be less than the maximum.

In the following IOM-2 frame, no adjustment is done since the SmartLink transmits in uplink direction.

Jitter on U_{pn}

Jitter on U_{pn} is directly related to the crystal tolerance. There is no transmit PLL involved.

Jitter on MCLK, Pulse Width Modulator, LCD Contrast

Jitter on these clocks is directly related to the crystal tolerance. Only clock dividers are involved.

2.2.2.1 Jitter (TR Mode)

Jitter on U_{pn}

Jitter on U_{pn} is directly related to the jitter on the IOM-2 clocks. A fixed divider is used to generate the U_{pn} data rate of 384 kbit/s.

2.3.6 Reset

The HDLC-controller mode is reset by applying a reset pulse to the $\overline{\text{RST}}$ input.

To bring the U_{pn}-transceiver to a low power state, the following requirements must be fulfilled: While reset is active, at least 40 clock pulses must be applied to XTAL1. After reset is released, another 10 clock pulses are required. The U_{pn}-transceiver enters its low power deactivated state after 6 IOM-frames which are generated after the 50 clock pulses on XTAL1 have elapsed.

This procedure is necessary only after power-cycle. Resetting SmartLink while the power remains active doesn't require the procedure to be performed again.

3.1.2.5 TE-Mode State Description

Level Detect, Resynchronization

During the first period of receiving info 2 or under severe disturbances on the line the U_{pn}-receiver recognizes the receipt of a signal but is not (yet) synchronized. In extremely rare situations of severe line disturbances, the U_{pn}-receiver might become locked in this state. To avoid this, it is recommended that the software issue an RES command to restart activation if SmartLink remains in this state longer than an acceptable period. This timeout period should be at least 110 ms, but the exact period should be chosen by the user based on system concerns.

Analog Loop 2

The states for analog loop 2 are identical to the states of the regular TE operation. The analog loop 2 indications are output if the S-bit of the U_{pn}-frame is ‘1’.

State	S-bit = 0	S-bit = 1
Synchronized	AR	ARL2
Activated	AI	AIL2

3.1.3 Operation of the Serial Control Interface

The first falling edge of SCLK will force the state machine to load the current value of STA1 into the shift register and output the MSB. The following clocks shift the contents of STA1 over the MISO line. At the same time, the MOSI line receives the value of CTRL1. Its value is stored in the CTRL1 register with the rising edge of the last clock period.

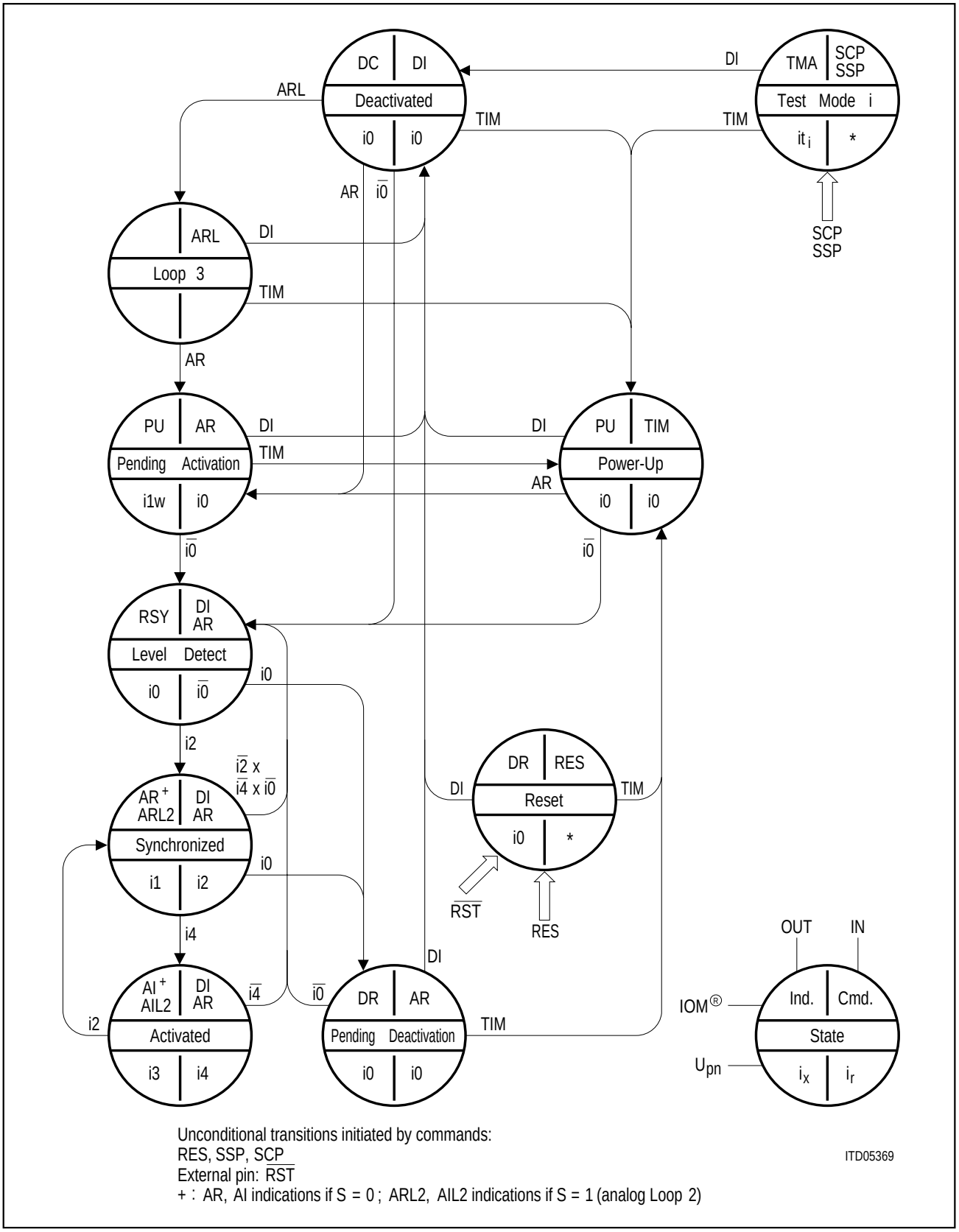


Figure 43
State Diagram TE-Mode

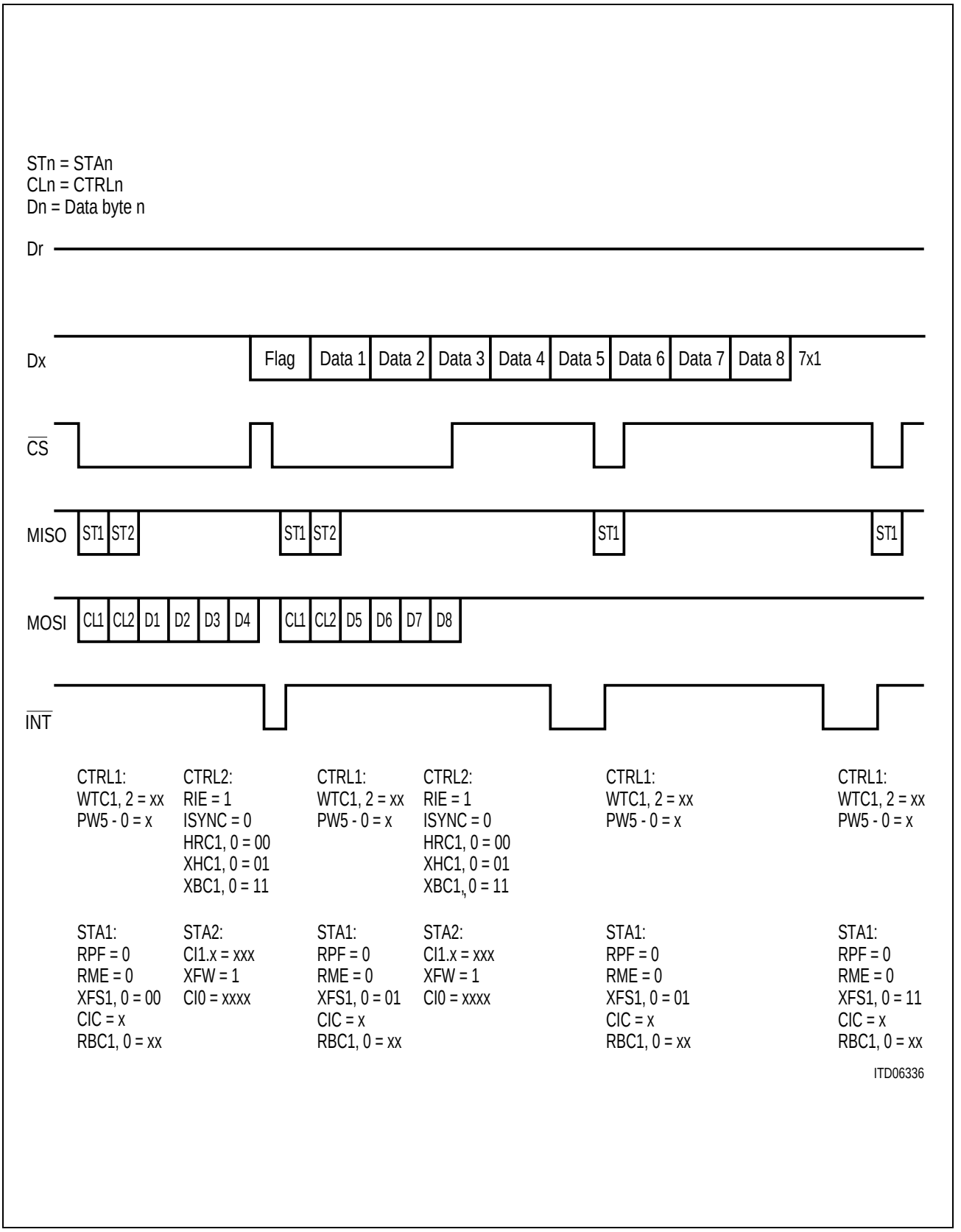


Figure 48
Transmit Data Underrun

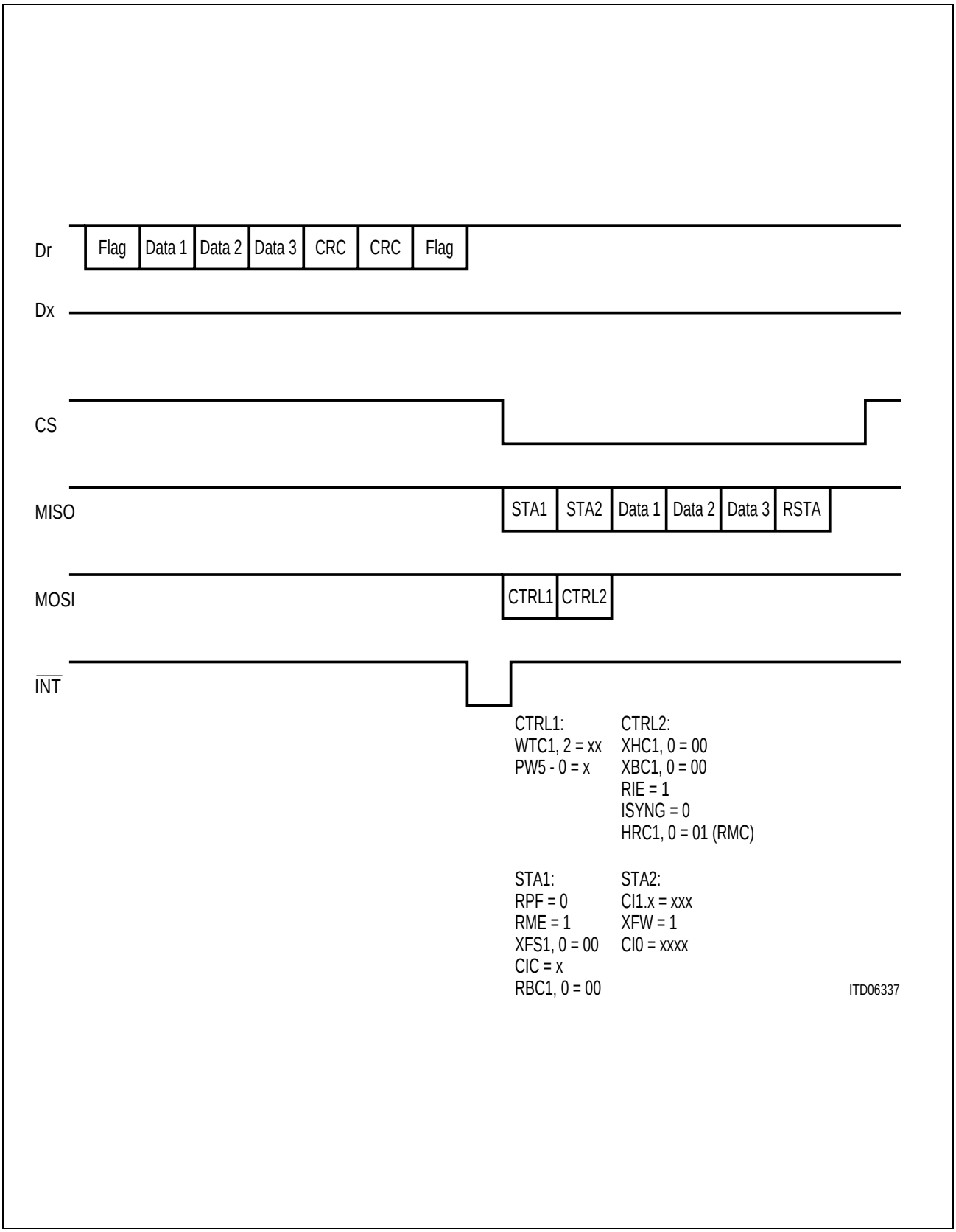


Figure 49a
Reception of Frames

3.1.5 Reset

Reset Logic

Table 3
Reset State of the SmartLink-P Registers

Register	Value after Reset	Meaning
STA1	00_H	No C/I-change, no status change, no data in RFIFO.
STA2	$0F_H$ (00_H)	C/I is '1111' ('0000' if undervoltage detection is used, see Note)
CTRL1	00_H	MCLK = 3.84 MHz, Watchdog disabled, PW = '000000'.
CTRL2	00_H	No HDLC-controller operation, no XFIFO-data.
CTRL3	00_H	Permanent D-channel access, permanent access to C/I0 and D-channel. T-channel mapped on S/G, PW-output operates as LCD-contrast, TIC-bus access during D-channel transmission only, TAD = '000'.
CTRL4	00_H	Normal operation of DU-line, Serial Strobe = '000' (OFF), CI0 = '0000'.

Note: If the undervoltage detection is used to generate the reset signal for SmartLink, the value in STA2 will read "00". Please refer to **figure 21** for details.

3.2.1.2 Layer-1 Command/Indication Codes in TR Mode

In TR mode, the U_{pn}-interface is activated if the C/I code Activate Request (AR, ARL2) or Activate Indication (AI, AIL2) has been detected in downstream direction. It stays activated until the C/I code Deactivation Confirmation (DC) is received in downstream direction.

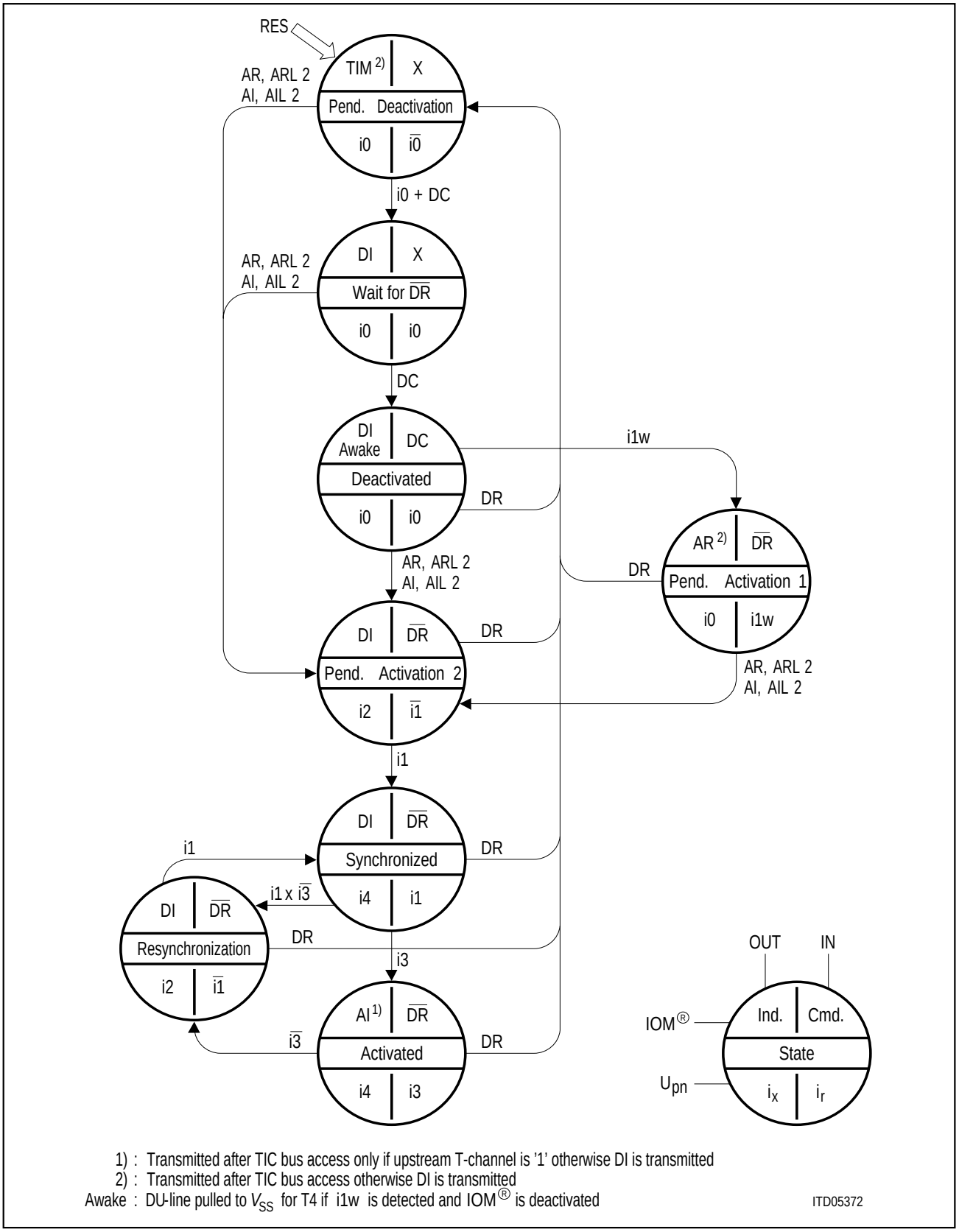


Figure 52
State Diagram TR-Mode

5 Electrical Characteristics

DC-Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition	Remarks
		min.	typ.	max.			
H-output voltage	V_{OH}	4.5			V	I_{OH} = 100 µA	XTAL2
L-output voltage	V_{OL}			0.4	V	$C_{LD} \leq$ 60 pF I_{OL} = 100 µA $C_{LD} \leq$ 60 pF	XTAL2
Input leakage current	I_{LI}			1	µA	0 V < V_{IN} < V_{DD}	All pins except LIa, LIb, XTAL1, XTAL2, $\overline{TST}$, RST, MCLK, BCL, SDS
Output leakage current	I_{LO}			1	µA	0 V ≤ $V_{OUT} \leq V_{DD}$	

All power consumption values are integrated values and not instantaneous currents. The currents for LIa and LIb in the remarks column of the power consumption parameters are instantaneous values.

All HDLC power consumption values are measured after the U_{pn}-transceiver is in the power-down state.

Capacitances
T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input capacitance I/O-capacitance	C_{IN} $C_{I/O}$		7 7	pF pF	All pins except Lla, Llb
Output capacitance	C_{OUT}		25	pF	Lla, Llb
Load capacitance	C_{LD}		60	pF	XTAL1, XTAL2

XTAL1,2 Recommended **typical** crystal parameters.

Parameter	Symbol	Limit Values		Unit	Remarks
		typ.			
Motional capacitance	C_1	20		fF	
Shunt	C_0	7		pF	
Load	C_L	≤ 30		pF	
Resonance resistor	R_r	≤ 65		Ω	

Note: The crystal tolerance of ± 100 ppm is the total tolerance required including adjustment, temperature and aging tolerances.
Start-up of the oscillator has been simulated and works with crystals which meet the above specifications.

AC Characteristics

There are no requirements regarding rise and fall times of input signals as long as all other AC timing requirements are met.

Serial Control Interface Timing

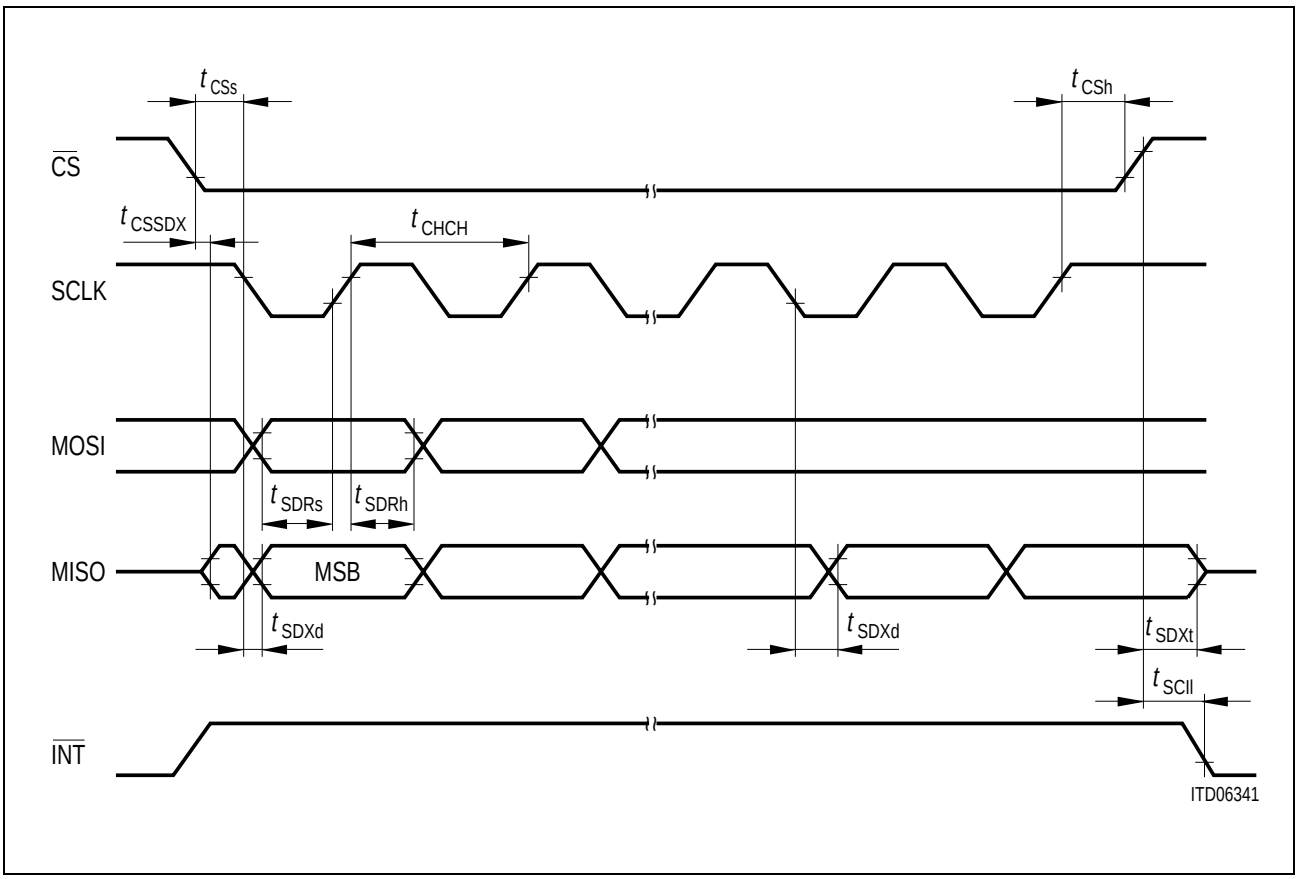


Figure 56
SCI-Switching Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Chip select setup time	t_{CSs}	15		ns
Chip select hold time	t_{CSh}	25		ns
CSQ high to MISO tristate	t_{SDXt}		70	ns

IOM®-2 Bus Switching Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Bit clock delay	t_{bcd}	– 20	50	ns

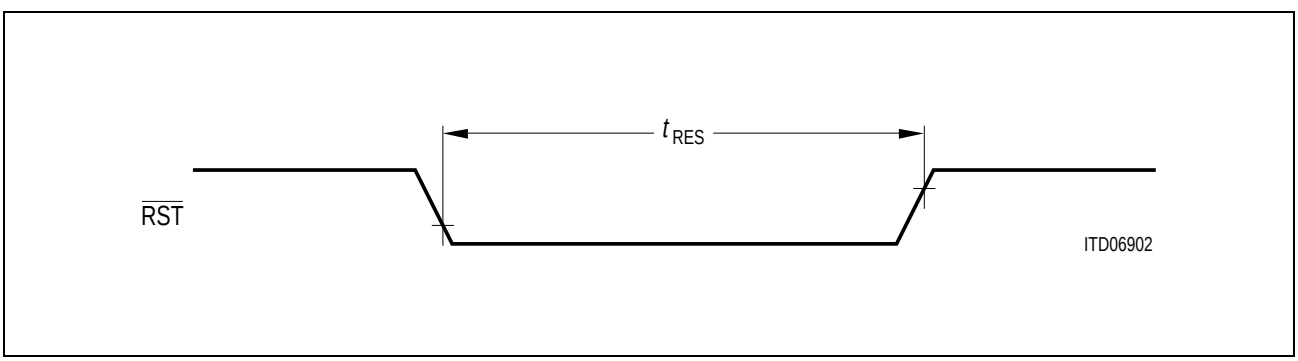
MCLK-Timing

The MCLK generator is designed to start with a complete clock cycle. Thus the minimum high or low period is n (n = 1, 2, 4, 8) × oscillator period (65 ns). Only if the undervoltage detection is active and it generates a reset signal due to voltage drop, MCLK will immediately be stopped at the same time the reset outputs become active. As a result, for that MCLK period, the minimum pulse width may be as low as 0 ns (see Reset Timings).

Reset Timings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Hysteresis	V_{HH}-V_{HL}	50	230	mV

External Reset Timings



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Reset pulse width	T_{RES}	2		µs

Note: If $\overline{RST}$ is configured as reset input, it must be driven to a valid V_{IL} during power-up.