SIEMENS

ICs for Communications

Digital Answering Machine

SAM

PSB 2168 Version 2.0

Delta Sheet 05.97

T2168-XV20-L1-7600

PSB 2168 Revision History:	Current Version: Version 2.0
Previous Version:	

Edition 05.97

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
HL IT

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Delta Sheet for Target Specification 03.97

This Delta Sheet states the differences between the chip version 2.0 and the chip version 2.1 as described by the Target Specification 03.97.

1 Support for KM29W8000, KM29N16000, KM29N32000

The PSB 2168 V2.0 does not support these memory devices.

2 Support for multiple KM29N040

The PSB 2168 V2.0 does not detect more than one device.

3 Status Register

The least three bits (0,1 and 2) are not set to zero but undefined.

These bits do not contain information. They can be either ignored or masked by the microcontroller. These bits do not generate an interrupt.

4 Activation of DRAM

If DRAM is selected as external memory the command *Activate* may return a wrong result if no DRAM is connected at all. This problem can be solved by connecting a pullup resistor (approx. 10 kΩ) to MD_0.

If DRAM is selected as external memory the command *Activate* returns a wrong result if the DRAM contains all zeroes within the first page. Table 1 shows the correct value (PSB 2168 V2.1) and the incorrect value (PSB 2168 V2.0).

Table 1

Register	PSB 2168 V2.0	PSB 2168 V2.1
FCTL	0	1
FDATA	0	memory size

Therefore the microcontroller should check FDATA for zero instead of checking FCTL for one.

Note: This problem does not occur with ARAM or flash memory.

5 Garbage Collection

The garbage collection may fail if the following conditions are true:

1. the memory is full
2. a *new* file has been opened

There are two workarounds for this problem (only one must be implemented).

1. Do not open a new file when the memory is full.
2. Close the file and mark it for deletion before issueing the garbage collection command.

6 Recompression with flash memory

The PSB 2168 V2.0 uses always the same block of the flash device during recompress. For each audio block of a message that is recompressed (30 ms) this block is used once. Table shows the life span of a flash device depending on its guaranteed endurance.

Table 2

Endurance (cycles)	Life span (seconds for recompression)
100.000	3.000
1.000.000	30.000

7 Memory full during record

If the memory becomes full while recording a message the length of the file is undefined. The microcontroller should therefore monitor the file pointer while a recording is in progress. If the filepointer indicates an almost full memory (e.g. only a few audio blocks left) the microcontroller should stop the recording actively.

8 Memory access in binary mode

For each word transferred to or from the PSB 2168 V2.0 in binary mode a delay of 30 ms is incurred.

9 CPT detector

In cooked mode (CPTCTL:MD=1) the minimum number of cycles (CPTTR:NUM) is two. Setting CPTTR:NUM to zero or one will result in a detected signal (STATUS:CPT) regardless of the actual signal. The encoding for CPPTR:NUM is shown below.

15			0
NUM	0	SN	MIN

NUM Number of Cycles

15	14	13	cooked mode	raw mode
0	0	0	reserved	0
0	0	1	reserved	reserved
0	1	0	2	reserved
...	...	...	...	reserved
1	1	1	7	reserved

10 DTMF detector

The minimum time for a rejected signal is 2 ms instead of 23 ms.

11 CNG detector

The calling tone detector accumulates all time periods during which it detects a calling tone while it is enabled. If the accumulated time exceeds the threshold programmed in CNGBT:TIME a calling tone will be detected.

Therefore the microcontroller should enable the CNG detector only for a short time (e.g. 1 s) at the beginning of an incoming call.

12 Automatic gain control of coder

The maximum value of the SPEEDH parameter in register AGC2 may not be sufficient to prevent clipping in case of a very fast transition from low to high signal levels.

13 Master Frame Sync Selection (MFS) in HWCONFIG1

The PSB 2168 V2.0 reports an abort (STATUS:ABT) after wake-up if HWCONFIG:MFS =1. In order to avoid the abort, the microcontroller should set HWCONFIG:MFS by the following procedure:

1. Wake up PSB 2168 V2.0 with HWCONFIG:MFS=0
2. Enable the SDI interface by setting SDCONF:SDE=1
3. Set HWCONFIG:MFS=1

14 Hardware Configuration Read Access

The command word for reading a hardware configuration register has a different format. The address field *R* has been expanded and moved from bit 0 to bits 9,10 and 11. Please refer to the corrected table in section 15.

15 Hardware Configuration Registers

The PSB 2168 V2.0 does not have the hardware configuration registers HWCONFIG 2 and HWCONFIG 3. However, some of the configuration bits of the missing registers can be found in the undocumented hardware configuration registers HWCONFIG 12 and HWCONFIG 13. In order to access these registers the tables 56, 57 and 58 (page 67) must read as follows:

Table 56
Command words for register access

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Status Register	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Read Register	0	1	0	1	REG											

Table 56
Command words for register access

Write Register	0	1	0	0	REG									
Read Configuration Reg.	0	1	1	1	R	0	0	0	0	0	0	0	0	0
Write Configuration Reg.	0	1	1	0	W	DATA								

In case of a configuration register write, W determines which configuration register is to be written (table 57):

Table 57
Address field W for configuration register write

11	10	9	8	Register
0	0	0	0	HWCONFIG 0
0	0	0	1	HWCONFIG 1
1	1	0	0	HWCONFIG 12
1	1	0	1	HWCONFIG 13

In case of a configuration register read, R determines which pair of configuration registers is to be read (table 58):

Table 58
Address field R for configuration register read

11	10	9	Register pair
0	0	0	HWCONFIG 0 / HWCONFIG 1
1	1	0	HWCONFIG 12/ HWCONFIG 13

The following table shows the mapping of the hardware configuration registers for the two versions:

Register Mapping HWCONFIG0-HWCONFIG3

PSB 2168 V2.1		**PSB 2168 V2.0**	
Register	Bits	Register	Bits
HWCONFIG0	0-7	HWCONFIG0	0-7
HWCONFIG1	0-7	HWCONFIG1	0-7
HWCONFIG2	0,1	not implemented	
HWCONFIG2	2,3	not implemented	
HWCONFIG2	4	not implemented	

Register Mapping HWCONFIG0-HWCONFIG3

PSB 2168 V2.1		PSB 2168 V2.0	
HWCONFIG2	5	HWCONFIG12	0
HWCONFIG2	6	HWCONFIG12	1
HWCONFIG2	7	HWCONFIG13	2
HWCONFIG3	0-7	not implemented	

Do not change any other bits within HWCONFIG12 and HWCONFIG13 (perform a read, modify, write cycle to ensure the original values for the other bits).

16 Auxiliary Clock Generation

The PSB 2168 V2.0 does not support auxiliary clock generation as described in chapter 2.3.9. Therefore the connection of a simple codec requires an external clock source.

As an example figure 1 shows the connection of an MC 145480 to the PSB 2168 V2.1 and figure 2 shows a workaround for the PSB 2168 V2.0.

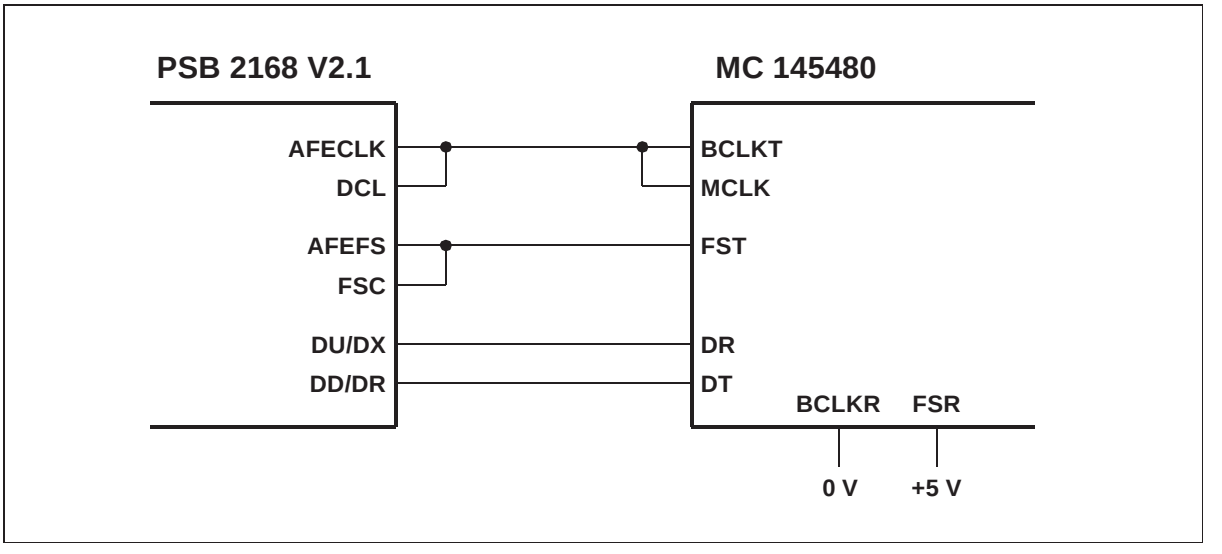

Figure 1
Connection of MC 145480 to PSB 2168 V2.1

In this example the PSB 2168 V2.1 generates the data clock (512 kHz) at AFECLK and the frame synchronization signal (8 kHz) at AFEFS. Both clocks are synchronized by the PSB 2168 V2.1. The MC 145480 is operated in General Circuit Interface mode (selected by BCLKR = 0 V). Data is transmitted and received in timeslot 2 (selected by FSR = +5 V) and double clock mode is used.

The PSB 2168 V2.0 does not supply any clock at AFEFS of AFECLK. Therefore the synchronized clocks must be supplied by external circuitry as shown in figure 2.

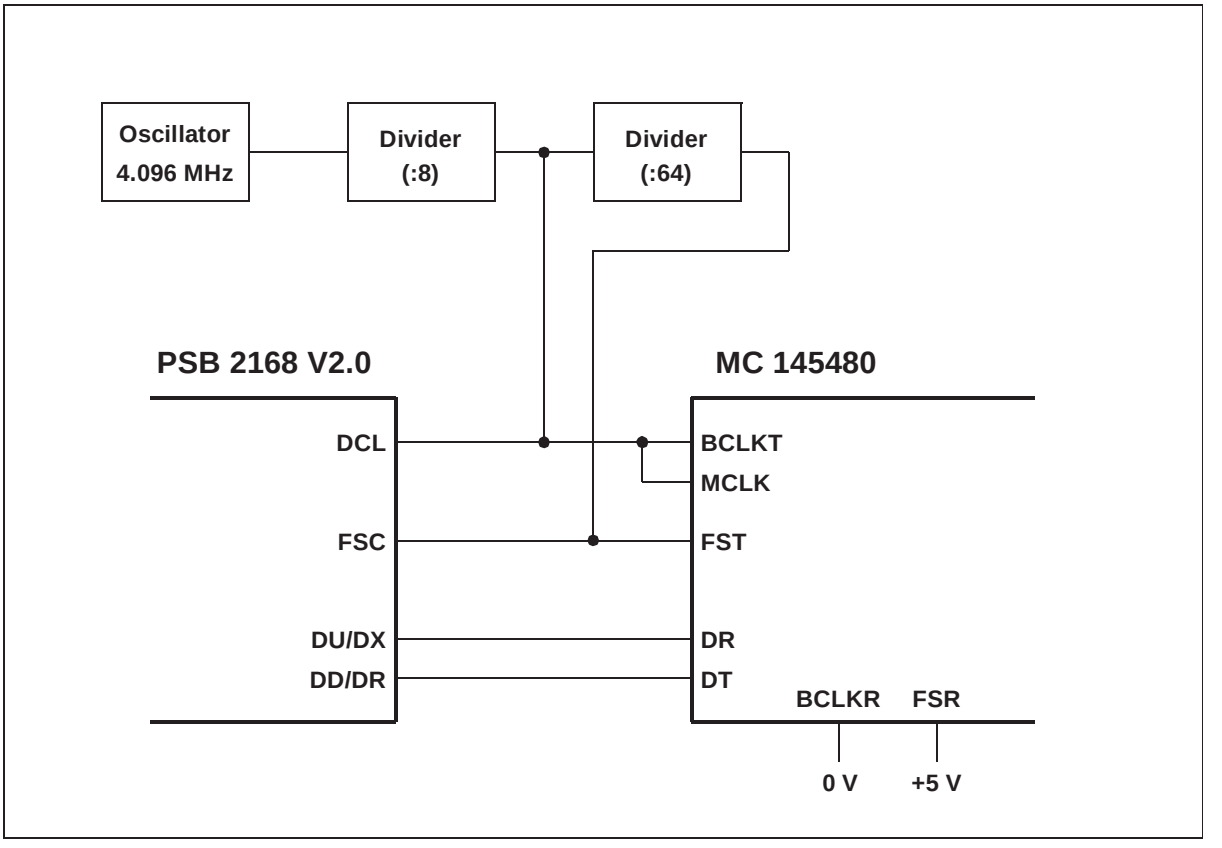

Figure 2
Connection of MC 145480 to PSB 2168 V2.0

17 Register CCTL (Chip Control)

The correct description of this register is given below. Bit RFM has changed position, bit CS9 is flipped and bit MQ is now described.

15														0
0	0	0	0	MV	0	0	PD	0	0	RFM	MQ	MT	CS9	SAS

MV Voice Prompt EPROM

0: not available

1: available

PD Power Down

0: PSB 2168 is in active mode

1: enter power-down mode

RFM Refresh Mode

0: normal

1: battery backup

MQ Memory Quality

0: ARAM

1: DRAM

MT Memory Type

3	2	Description
0	0	ARAM/DRAM
0	1	Intel flash memory
1	1	Samsung flash memory

CS9 CAS selection

0: other memory

1: 256kx4 or 512kx8 memory

SAS Split Address Space

0: other ARAM/DRAM

1: two 2Mx8 devices

18 Register SDCONF (Serial Data Interface Configuration)

The field NTS of this register is described incorrectly. The correct description of this register is given below.

15										0
0	0	NTS		0	0	0	0	0	DCL	0	EN

NTS Number of Timeslots

11	10	9	8	7	6	Description
0	0	0	0	0	0	1
0	0	0	0	0	1	2
...	...	...	...	...	...	...
1	1	1	1	1	1	64

DCL Double Clock Mode

0: Single Clock Mode

1: Double Clock Mode

EN Enable Interface

0: Interface is disabled (both channels)

1: Interface is enabled (depending on separate channel enable bits)