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ICs for Communications

Digital Answering Machine
SAM

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Data Sheet 11.97

DS 1

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1 Overview

The PSB 2168 provides a solution for an embedded answering in an IOM®-2 based system.

The chip features recording by DigiTape™, a family of high performance algorithms. Messages recorded with DigiTape™ can be played back with variable speed without pitch alteration. Messages recorded with a higher bitrate can be converted into messages with a lower bitrate arbitrarily. Current members of DigiTape (TM) span the range from 3.3 kbit/s to 10.3 kbit/s.

Furthermore the PSB 2168, V2.1 has a a caller ID decoder, DTMF recognition and generation and call progress tone detection. The frequency response of cheap microphones or loudspeakers can be corrected by a programmable equalizer.

Messages and user data can be stored in ARAM/DRAM or flash memory which can be directly connected to the PSB 2168. The PSB 2168 also supports a voice prompt EPROM for fixed announcements.

The PSB 2168 provides an IOM®-2 compatible interface with two channels for speech data.

Alternatively to the IOM®-2 compatible interface the PSB 2168 supports a simple serial data interface (SSDI) with separate strobe signals for each direction (linear PCM data, one channel).

The chip is programmed by a simple four wire serial control interface and can inform the microcontroller of new events by an interrupt signal. For data retention the PSB 2168 supports a power down mode where only the real time clock and the memory refresh (in case of ARAM/DRAM) are operational.

The PSB 2168 supports interface pins to +5 V levels.

SIEMENS

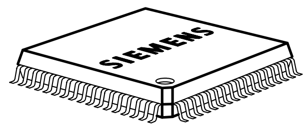
Digital Answering Machine
SAM

PSB 2168

Version 2.1

CMOS

1.1 Features



P-MQFP-80

Digital Functions

- High performance recording by DigiTape™
- Selectable compression rate (3.3 kbit/s, 10.3 kbit/s)
- Variable playback speed
- Support for ARAM or Flash Memory
- Optional voice prompt EPROM
- DTMF generation and detection
- Call progress tone detection
- Caller ID recognition
- Direct memory access
- Real time clock
- Equalizer
- Automatic gain control
- Automatic timestamp
- Auxiliary parallel port
- Ultra low power refresh mode

General Features

- SSDI/IOM®-2 compatible interface
- Serial control interface for programming
- Master clock generation for common codecs

Type	Package
PSB 2168	P-MQFP-80

1.2 Pin Configuration

(top view)

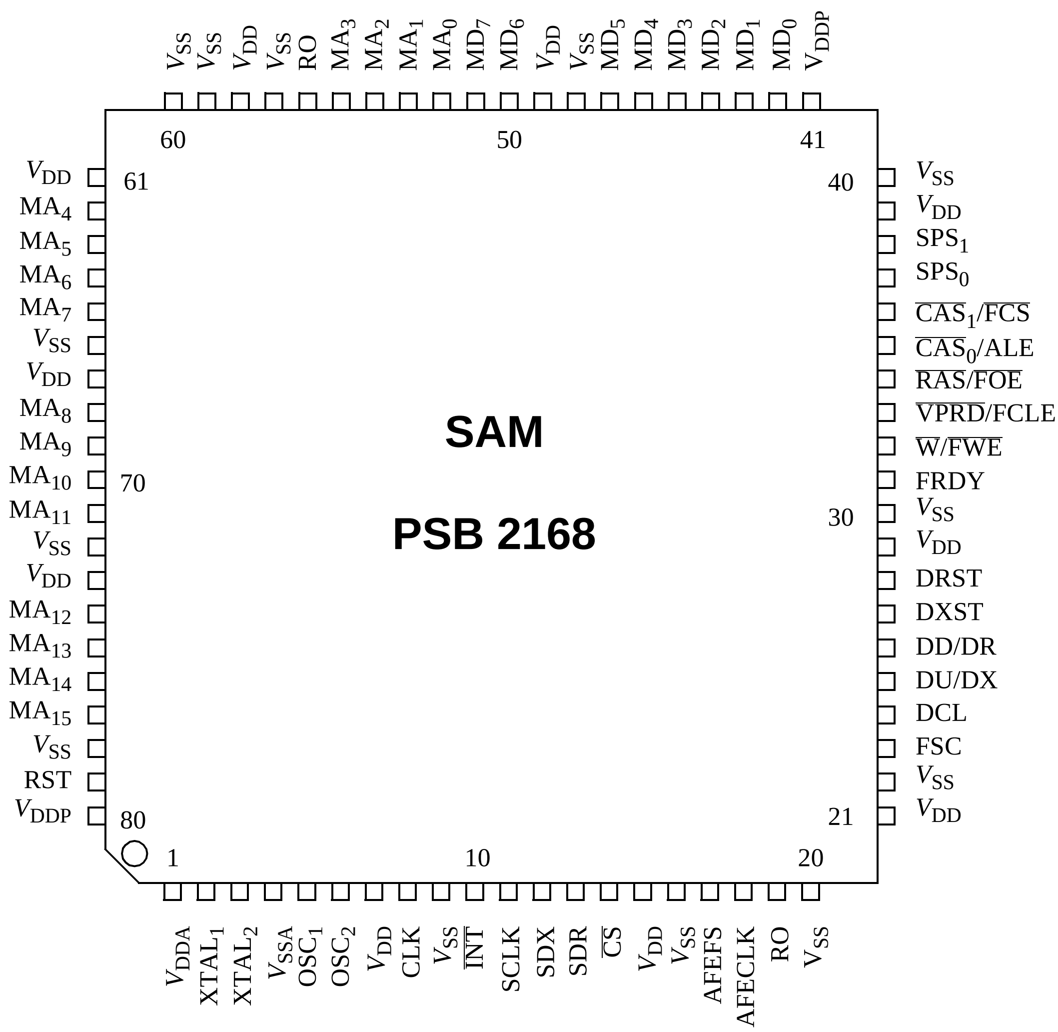


Figure 1 Pin Configuration of PSB 2168

1.3 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin No. P-MQFP-80	Symbol	Dir.	Reset	Function
41, 80	V_{DDP}	-	-	**Power supply (5V ±10 %)** Power supply for the interface.
7, 15, 21, 29, 39, 49, 58, 61, 67, 73	V_{DD}	-	-	**Power supply (3.0 V - 3.6 V**) Power supply for logic.
1	V_{DDA}	-	-	**Power supply (3.0 V - 3.6 V)** Power supply for clock generator.
4	V_{SSA}	-	-	**Power supply (0 V)** Ground for clock generator.
9, 16,20, 22, 30, 40, 48, 57, 59, 60, 78, 66, 72	V_{SS}	-	-	**Power supply (0 V)** Ground for logic and interface.
17	AFEFS	O	L	**Analog Frontend Frame Sync:** 8 kHz frame synchronization signal for the analog front end.
18	AFECLK	O	L	**Analog Frontend Clock:** Clock signal for the analog front end.
79	RST	I	-	**Reset:** Active high reset signal.
23	FSC	I	-	**Data Frame Synchronization:** 8 kHz frame synchronization signal (IOM®-2 and SSDI mode).
24	DCL	I	-	**Data Clock:** Data Clock of the serial data interface.
26	DD/DR	**I**/OD I	-	**IOM®-2 Compatible Mode:** Receive data from IOM®-2 controlling device. **SSDI Mode:** Receive data of the strobed serial data interface.

Table 1 Pin Definitions and Functions

25	DU/DX	**I**/OD O/ OD	-	**IOM®-2 Compatible Mode:** Transmit data to IOM®-2 controlling device. **SSDI Mode:** Transmit data of the strobed serial data interface.
27	DXST	O	L	**DX Strobe:** Strobe for DX in SSDI interface mode.
28	DRST	I	-	**DR Strobe:** Strobe for DR in SSDI interface mode.
14	$\overline{CS}$	I	-	**Chip Select:** Select signal of the serial control interface (SCI).
11	SCLK	I	-	**Serial Clock:** Clock signal of the serial control interface (SCI).
13	SDR	I	-	**Serial Data Receive:** Data input of the serial control interface (SCI).
12	SDX	O/ **OD**	H	**Serial Data Transmit:** Data Output of the serial control interface (SCI).
10	$\overline{INT}$	O/ **OD**	H	**Interrupt** New status available.
52 53 54 55 62 63 64 65 68 69 70 71 74 75 76 77	MA_0 MA_1 MA_2 MA_3 MA_4 MA_5 MA_6 MA_7 MA_8 MA_9 MA_{10} MA_{11} MA_{12} MA_{13} MA_{14} MA_{15}	I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O** I/**O**	L[1)] L L L L L L L L L L L L L L L	**Memory Address 0-15:** Multiplexed address outputs for ARAM, DRAM access. Non-multiplexed address outputs for voice prompt EPROM. **Auxiliary Parallel Port:** General purpose I/O.

Table 1 Pin Definitions and Functions

42 43 44 45 46 47 50 51	MD_0 MD_1 MD_2 MD_3 MD_4 MD_5 MD_6 MD_7	I/O I/O I/O I/O I/O I/O I/O I/O	- - - - - - - -	**Memory Data 0-7:** Memory (ARAM, DRAM, Flash Memory, EPROM) data bus.
35 36	$\overline{CAS_0}$/ ALE $\overline{CAS_1}$/ $\overline{FCS}$	O O	H[2)	**ARAM, DRAM:** Column address strobe for memory bank 0 or 1. **Flash Memory:** Address Latch Enable for address lines A_{16}-A_{23}. Chip select signal for Flash Memory
34	$\overline{RAS}$/ $\overline{FOE}$	O	H[2)	**ARAM, DRAM:** Row address strobe for both memory banks. **Flash Memory:** Output enable signal for Flash Memory.
33	$\overline{VPRD}$/ FCLE	O	H[2)	**ARAM, DRAM:** Read signal for voice prompt EPROM. **Flash Memory:** Command latch enable for Flash Memory.
32	$\overline{W}$/$\overline{FWE}$	O	H[2)	**ARAM, DRAM:** Write signal for all memory banks. **Flash Memory:** Write signal for Flash Memory.
31	FRDY	I	-	**Flash Memory Ready** Input for Ready/Busy signal of Flash Memory
5 6	OSC_1 OSC_2	I O	- Z	**Auxiliary Oscillator:** Oscillator loop for 32.768 kHz crystal.
8	CLK	I	-	**Alternative AFECLK Source** 13,824 MHz
2 3	$XTAL_1$ $XTAL_2$	I O	- Z	**Oscillator:** $XTAL_1$: External clock or input of oscillator loop. $XTAL_2$: output of oscillator loop for crystal.

Table 1 Pin Definitions and Functions

37 38	SPS_0 SPS_1	O O	L L	**Multipurpose Outputs:** General purpose, address lines or status
19, 56	RO	O	-	**Reserved Output** Must be left open.

1) These lines are driven low with 125 µA until the mode (address lines or auxiliary port) is defined.

2) These lines are driven high with 70 µA during reset.

1.4 Logic Symbol

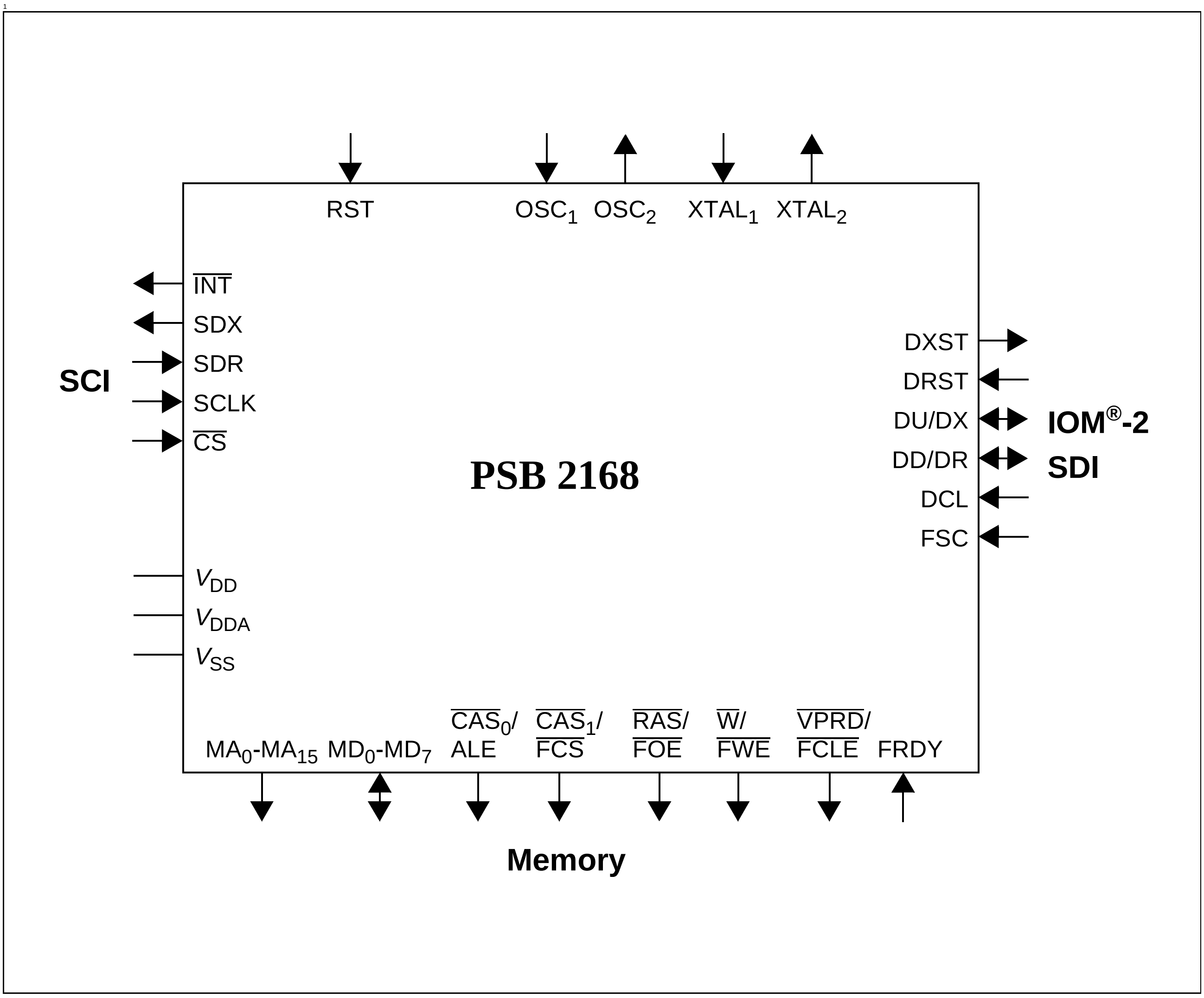


Figure 2 Logic Symbol of PSB 2168

1.5 Functional Block Diagram

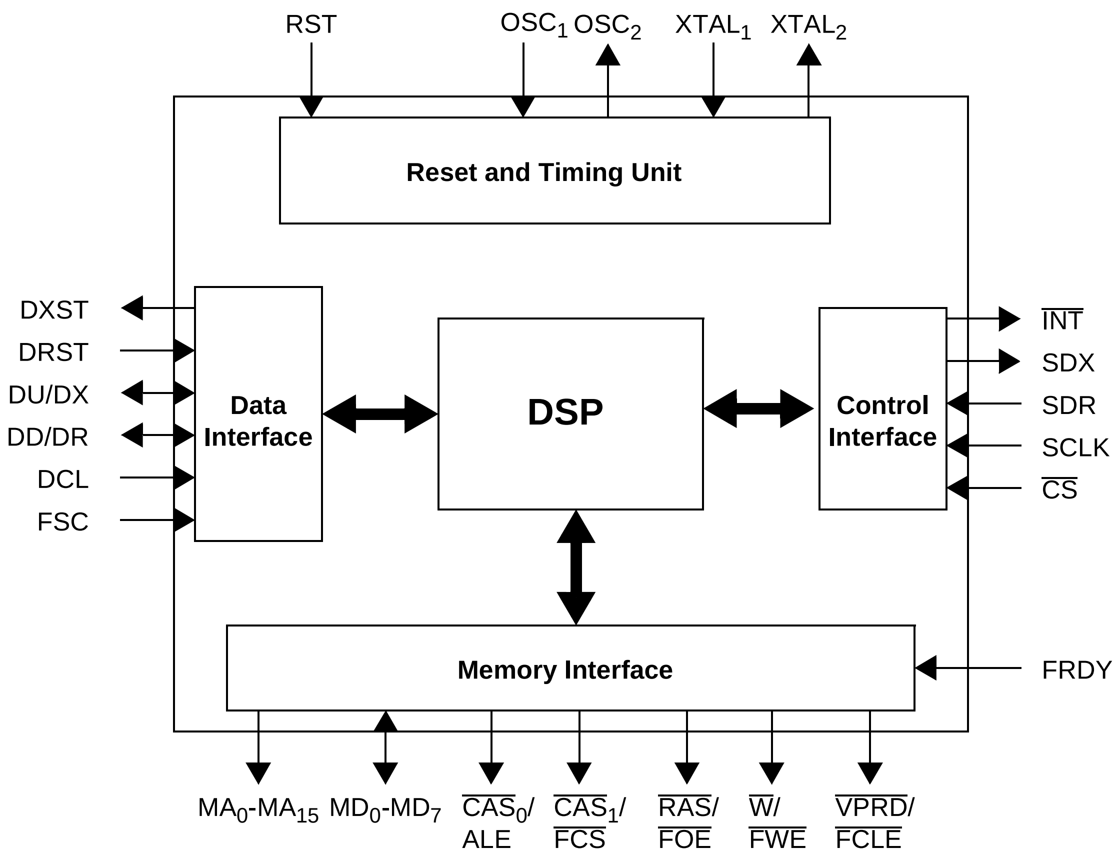


Figure 3 Block Diagram of PSB 2168

1.6 System Integration

The integration into an ISDN terminal is shown in figure **4**. All voice data is transferred by the IOM®-2 compatible interface. The PSB 2168 is programmed by the SCI interface. The PSB 2163 is programmed by the IOM®-2 interface. The microcontroller can access the memory attached to the PSB 2168. This is useful for storing system parameters or phonebook entries.

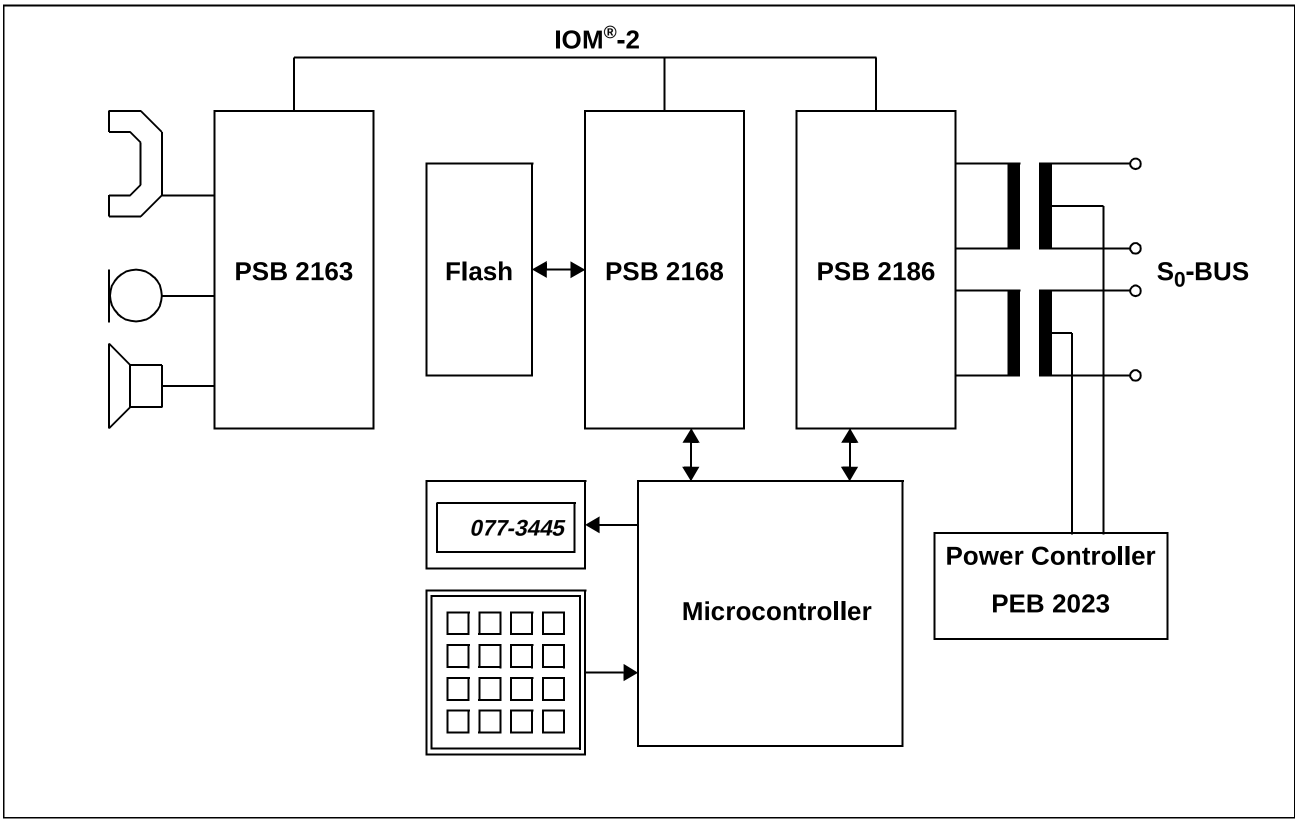


Figure 4 Featurephone with Answering Machine for ISDN Terminal

1.6.1 Stand-Alone Answering Machine

The PSB 2168 can also be used in conjunction with a simple codec for a stand-alone answering machine (figure **5**). In this application the PSB 2168 generates the necessary clocks for the simple codec at the pins AFECLK and AFEFS. Therefore the simple codec can be connected without further glue logic.

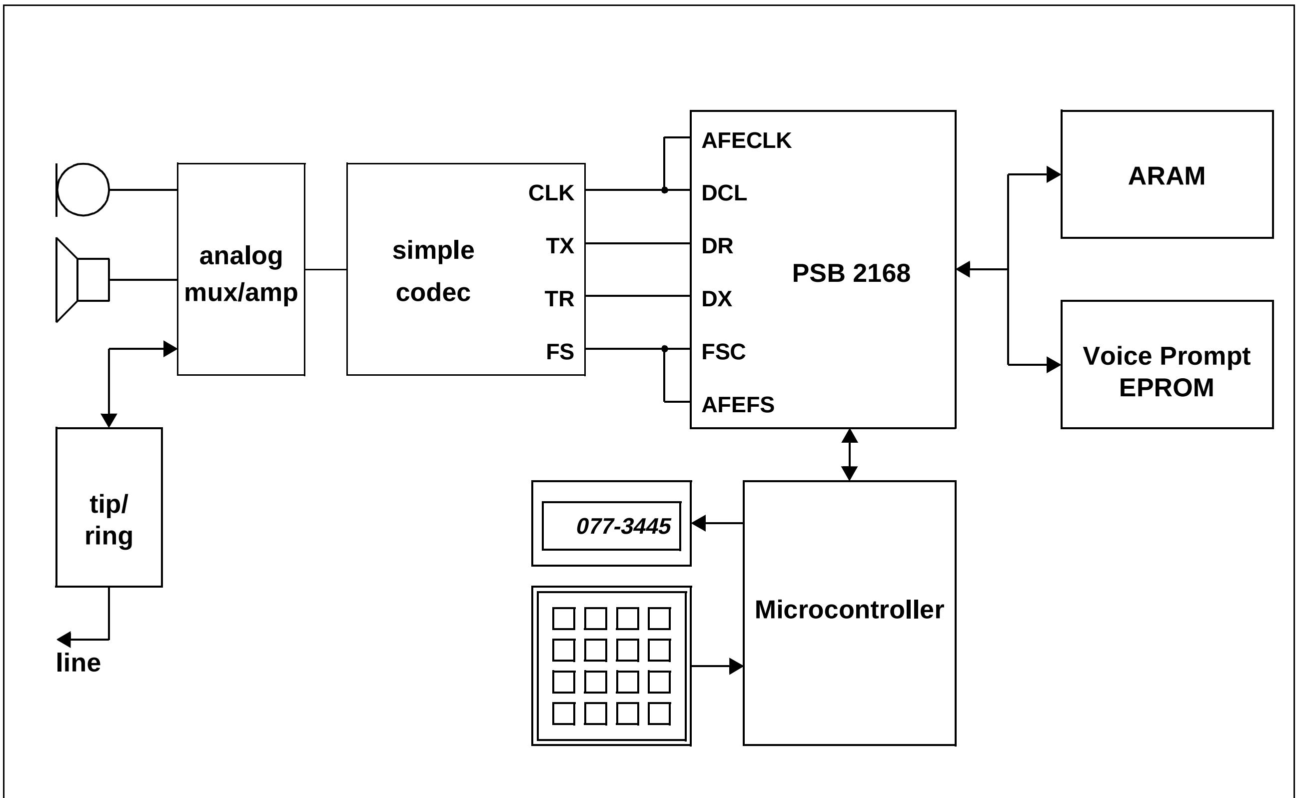


Figure 5 Stand-Alone Answering Machine with ARAM/EPROM

Furthermore the PSB 2168 can be used to scan the keyboard and drive the display if instead of ARAM/DRAM and EPROM flash memory devices (SAMSUNG mode) are used for storage (figure **6**).

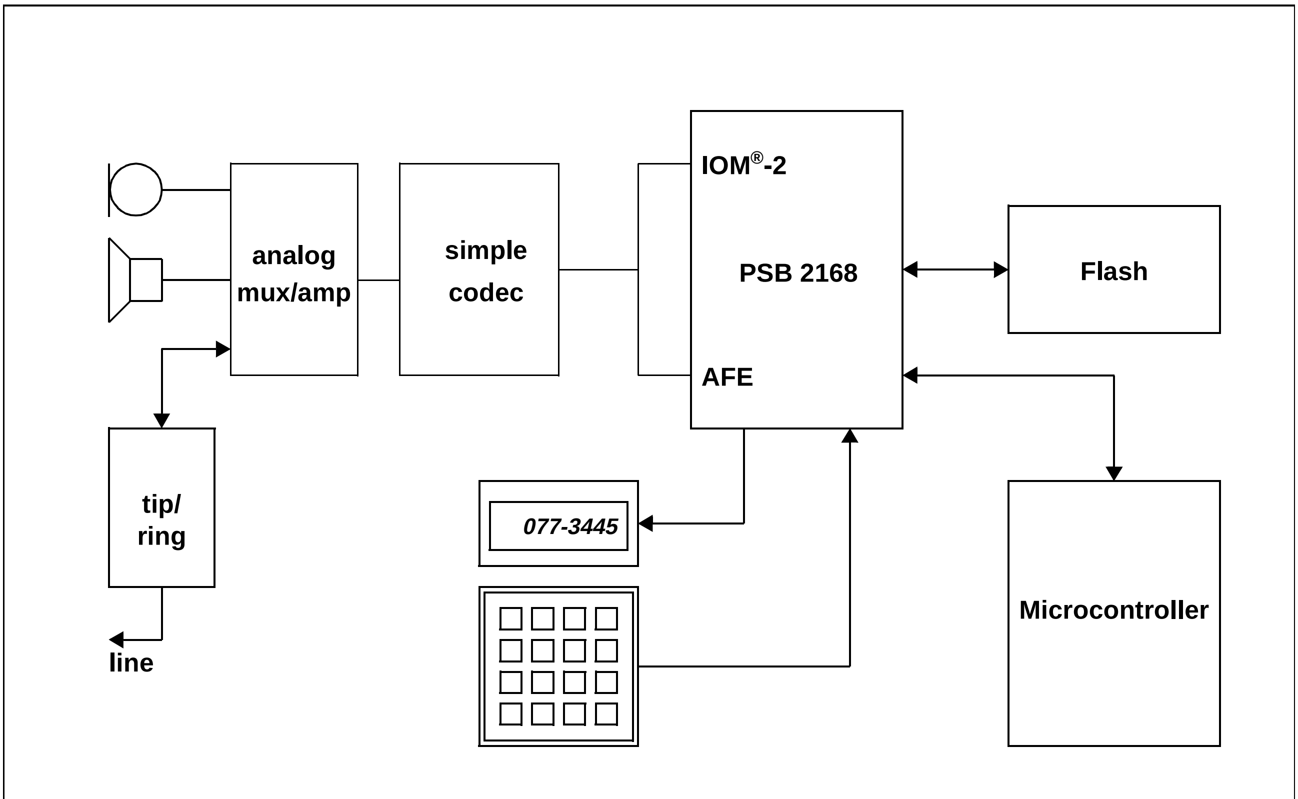


Figure 6 Stand-Alone Answering Machine with Flash Memory

In either case all features of the PSB 2168 can be used (e.g. caller id).

2 Functional Description

The PSB 2168 contains several functional units that can be combined with almost no restrictions to perform a given task. Figure **7** gives an overview of the important functional units.

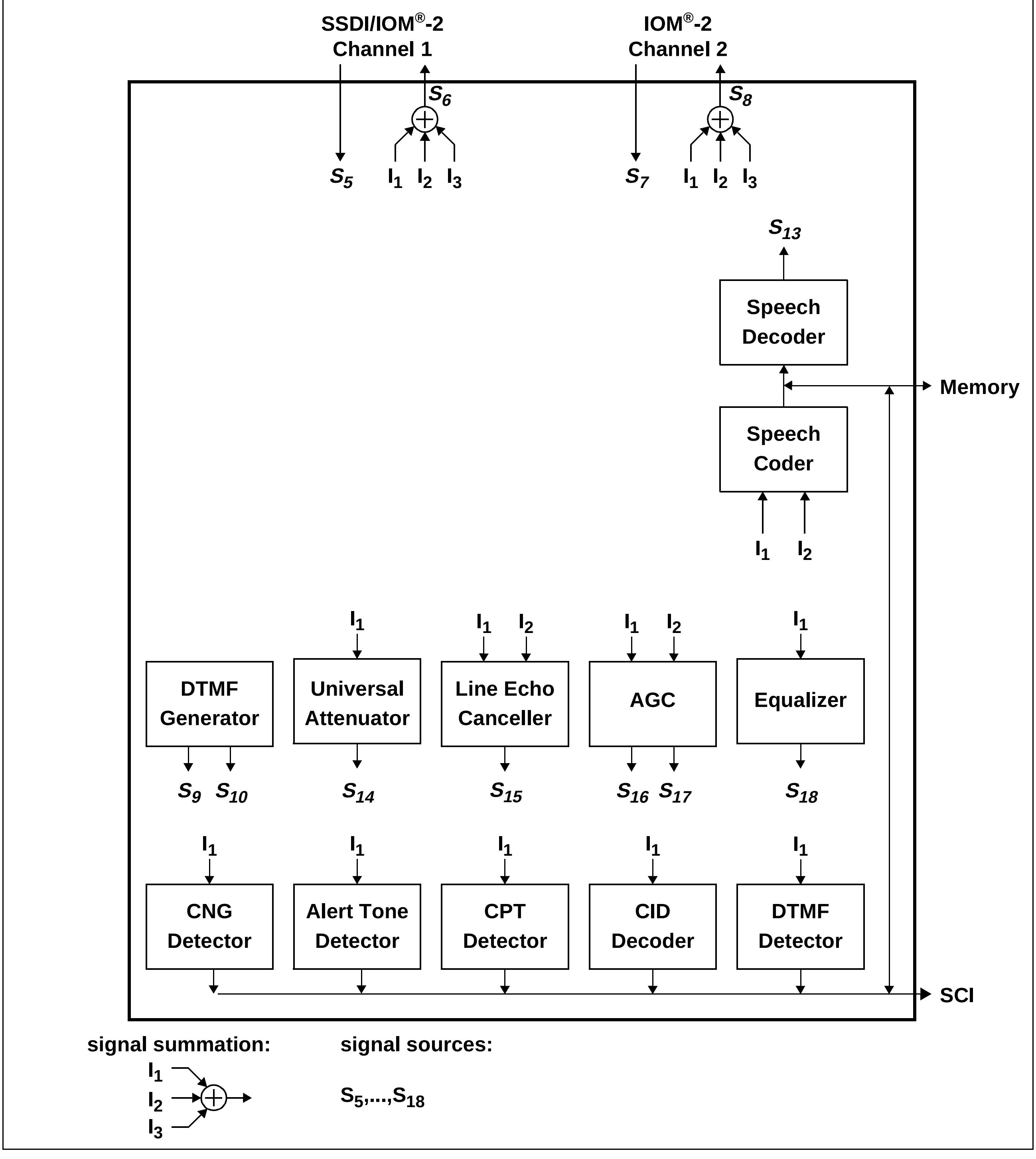


Figure 7 Functional Units - Overview

Each unit has one or more signal inputs (denoted by I). Most units have at least one signal output (denoted by S). Any input I can be connected to any signal output S. In addition to the signals shown in figure **7** there is also the signal S_0 (silence), which is useful at signal summation points. Table **2** lists the available signals within the PSB 2168 according to their reference points.

Table 2 Signal Summary

Signal	Description
S_0	Silence
S_1	Reserved
S_2	Reserved
S_3	Reserved
S_4	Reserved
S_5	Serial interface input, channel 1
S_6	Serial interface output, channel 1
S_7	Serial interface input, channel 2
S_8	Serial interface output, channel 2
S_9	DTMF generator output
S_{10}	DTMF generator auxiliary output
S_{11}	Reserved
S_{12}	Reserved
S_{13}	Speech decoder output
S_{14}	Universal attenuator output
S_{15}	Line echo canceller output
S_{16}	Automatic gain control output (after gain stage)
S_{17}	Automatic gain control output (before gain stage)
S_{18}	Equalizer output

The following figures show the connections for a typical state during operation. Units that are not needed are not shown. Inputs that are not needed are connected to S_0 which provides silence (denoted by 0). In figure **8** a phone conversation is currently in progress. The speech coder is used to record the signals of both parties. The alert tone detector is used to detect an alerting tone of an off-hook caller id request while the CID decoder decodes the actual data transmitted in this case.

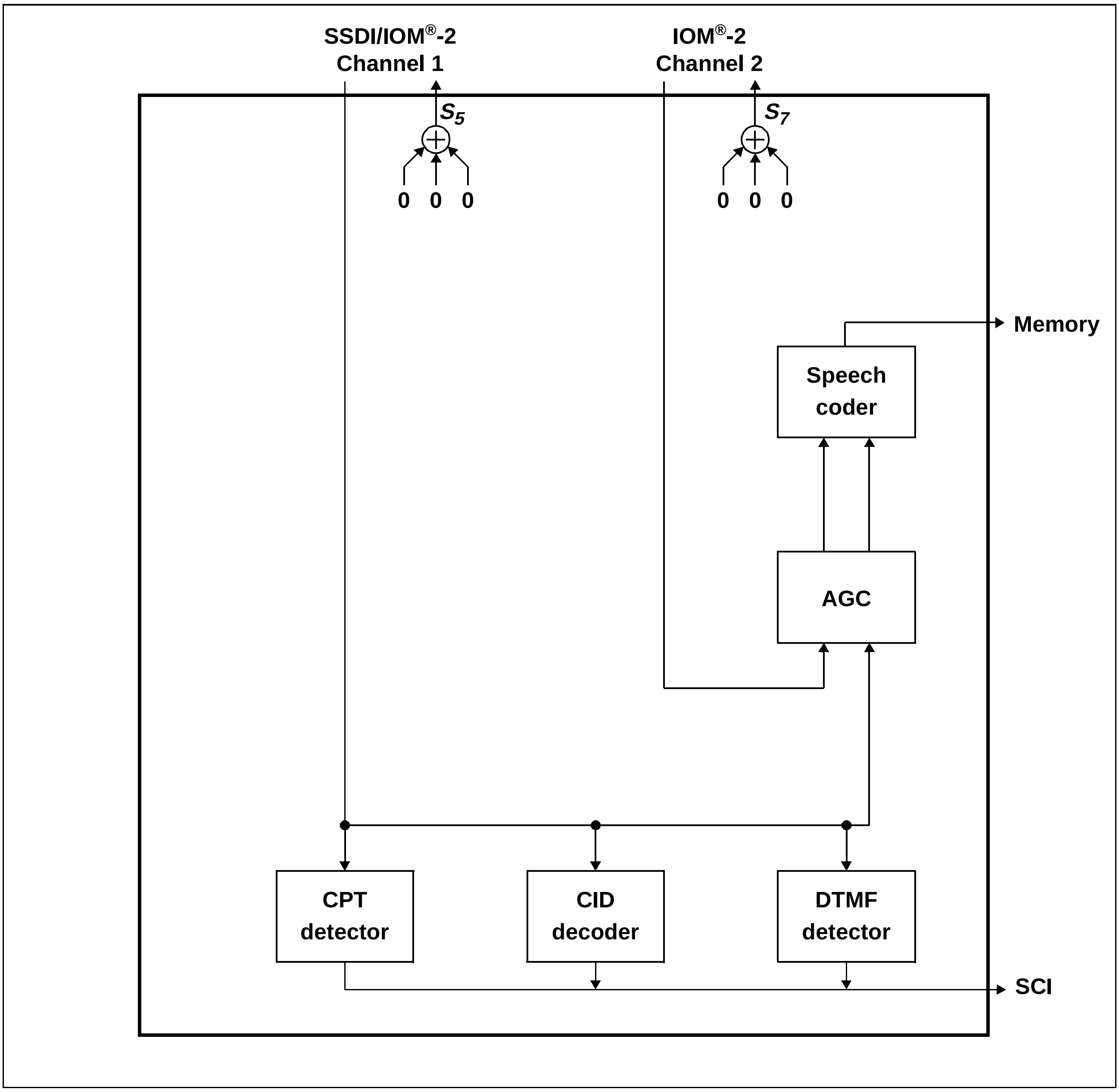


Figure 8 Functional Units - Recording a Phone Conversation

2.1 Functional Units

In this section the functional units of the PSB 2168 are described in detail. The functional units can be individually enabled or disabled.

2.1.1 Line Echo Canceller

The PSB 2168 contains an adaptive line echo cancellation unit for the cancellation of near end echoes. The unit has two modes: normal and extended. In normal mode, the maximum echo length is 4 ms. This mode is always available. In extended mode, the maximum echo length is 24 ms. Extended mode cannot be used while the speech encoder or slow playback is active.

The line echo cancellation unit is especially useful in front of the various detectors (DTMF, CPT, etc.). A block diagram is shown in figure **9**.

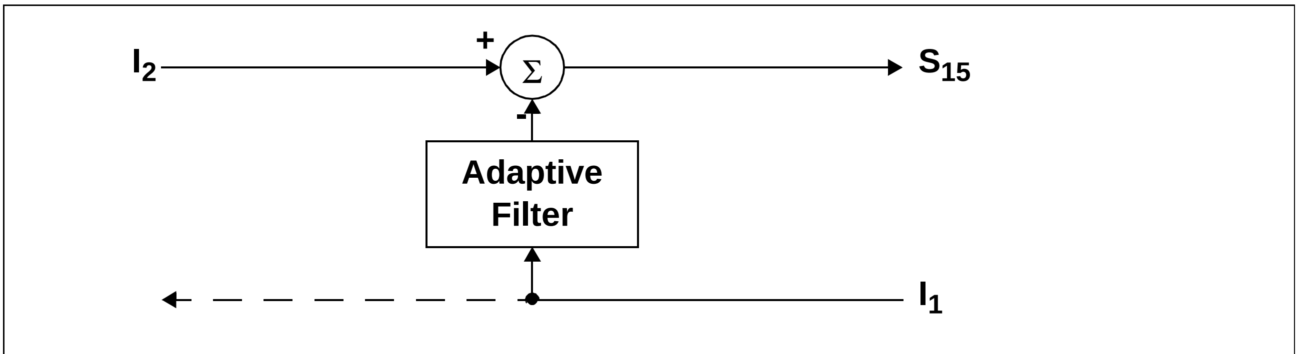


Figure 9 Line Echo Cancellation Unit - Block Diagram

The line echo canceller provides only one outgoing signal (S_{15}) as the other outgoing signal would be identical with the input signal I_1.

Input I_2 is usually connected to the line input while input I_1 is connected to the outgoing signal.

In normal mode the adaption process can be controlled by three parameters: MIN, ATT and MGN. Adaption takes only place if both of the following conditions hold:

1. $I1 > MIN$
2. $I1 - I2 - ATT + MGN > 0$

With the first condition adaption to small signals can be avoided. The second condition avoids adaption during double talk. The parameter ATT represents the echo loss provided by external circuitry. The adaption stops if the power of the received signal (I2) exceeds the power of the expected signal (I1-ATT) by more than the margin MGN.

Table **3** shows the registers associated with the line echo canceller.

Table 3 Line Echo Cancellation Unit Registers

Register	# of Bits	Name	Comment	Relevant Mode
LECCTL	1	EN	Line echo canceller enable	both
LECCTL	1	MD	Line echo canceller mode	
LECCTL	5	I2	Input signal selection for I_2	both
LECCTL	5	I1	Input signal selection for I_1	both
LECLEV	15	MIN	Minimal power for signal I_1	normal
LECATT	15	ATT	Externally provided attenuation (I_1 to I_2)	normal
LECMGN	15	MGN	Margin for double talk detection	normal

2.1.2 DTMF Detector

Figure **10** shows a block diagram of the DTMF detector. The results of the detector are available in the status register and a dedicated result register that can be read via the serial control interface (SCI) by the external controller. All sixteen standard DTMF tones are recognized.

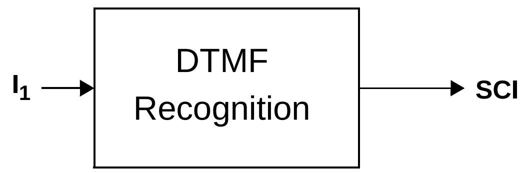


Figure 10 DTMF Detector - Block Diagram

Table **4** to **6** show the associated registers.

Table 4 DTMF Detector Control Register

Register	# of Bits	Name	Comment
DDCTL	1	EN	DTMF detector enable
DDCTL	5	I1	Input signal selection

As soon as a valid DTMF tone is recognized, the status word and the DTMF tone code are updated (table **5**).

Table 5 DTMF Detector Results

Register	# of Bits	Name	Comment
STATUS	1	DTV	DTMF code valid
DDCTL	5	DTC	DTMF tone code

DTV is set when a DTMF tone is recognized and reset when no DTMF tone is recognized or the detector is disabled. The code for the DTMF tone is placed into the register DDCTL. The registers DDTW and DDLEV hold parameters for detection (table **6**).

Table 6 DTMF Detector Parameters

Register	# of Bits	Name	Comment
DDTW	15	TWIST	Twist for DTMF recognition
DDLEV	6	MIN	Minimum signal level to detect DTMF tones

2.1.3 CNG Detector

The calling tone (CNG) detector can detect the standard calling tones of fax machines or modems. This helps to distinguish voice messages from data transfers. The result of the detector is available in the status register that can be read via the serial control interface (SCI) by the external controller. The CNG detector consists of two band-pass filters with fixed center frequency of 1100 Hz and 1300 Hz.

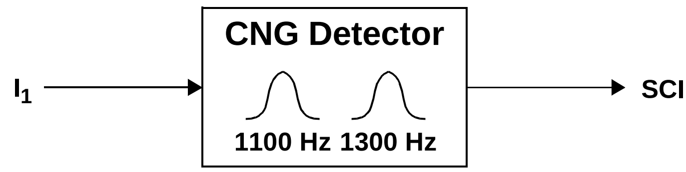


Figure 11 CNG Detector - Block Diagram

Table **7** shows the available parameters.

Table 7 CNG Detector Registers

Register	# of Bits	Name	Comment
CNGCTL	1	EN	CNG detector enable
CNGCTL	5	I1	Input signal selection
CNGLEV	16	MIN	Minimum signal level
CNGBT	16	TIME	Minimum time of signal burst
CNGRES	16	RES	Input signal resolution

Both the programmed minimum time and the minimum signal level must be exceeded for a valid CNG tone. Furthermore the input signal resolution can be reduced by the RES parameter. This can be useful in a noisy environment at low signal levels although the accuracy of the detection decreases. As soon as a valid tone is recognized, the status word of the PSB 2168 is updated. The status bits are defined as follows:

Table 8 CNG Detector Result

Register	# of Bits	Name	Comment
STATUS	1	CNG	Fax/Modem calling tone detected

2.1.4 Alert Tone Detector

The alert tone detector can detect the standard alert tones (2130 Hz and 2750 Hz) for caller id protocols. The results of the detector are available in the status register and the dedicated register ATDCTL0 that can be read via the serial control interface (SCI) by the external controller.

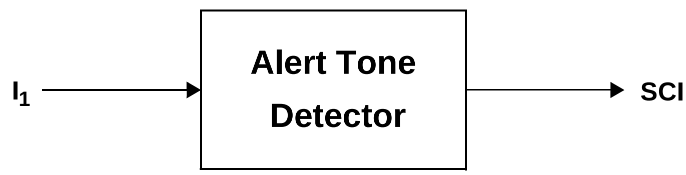


Figure 12 Alert Tone Detector - Block Diagram

Table 9 Alert Tone Detector Registers

Register	# of Bits	Name	Comment
ATDCTL0	1	EN	Alert Tone Detector Enable
ATDCTL0	5	I1	Input signal selection
ATDCTL1	1	MD	Detection of dual tones or single tones
ATDCTL1	1	DEV	Maximum deviation (0.5% or 1.1%)
ATDCTL1	8	MIN	Minimum signal level to detect alert tones

As soon as a valid alert tone is recognized, the status word of the PSB 2168 and the code for the detected combination of alert tones are updated (table **10**).

Table 10 Alert Tone Detector Results

Register	# of Bits	Name	Comment
STATUS	1	ATV	Alert tone detected
ATDCTL0	2	ATC	Alert tone code

2.1.5 CPT Detector

The selected signal is monitored continuously for a call progress tone. The CPT detector consists of a band-pass and an optional timing checker (figure **13**).

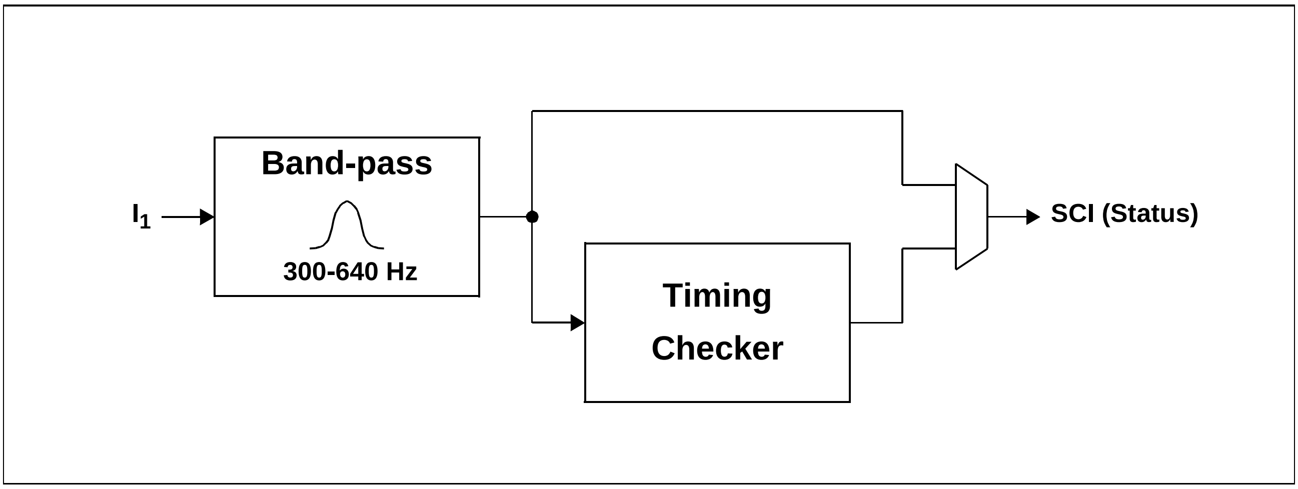


Figure 13 CPT Detector - Block Diagram

The CPT detector can be used in two modes: raw and cooked. In raw mode, the occurrence of a signal within the frequency range, time and energy limits is directly reported. The timing checker is bypassed and therefore the PSB 2168 does not interpret the length or interval of the signal.

In cooked mode, the number and duration of signal bursts are interpreted by the timing checker. A signal burst followed by a gap is called a cycle. Cooked mode requires a minimum of two cycles. The CPT flag is set with the first burst after the programmed number of cycles has been detected. The CPT flag remains set until the unit is disabled, even if the conditions are not met anymore. In this mode the CPT is modelled as a sequence of identical bursts separated by gaps with identical length. The PSB 2168 can be programmed to accept a range for both the burst and the gap. It is also possible to specify a maximum aberration of two consecutive bursts and gaps. Figure **14** shows the parameters for a single cycle (burst and gap).

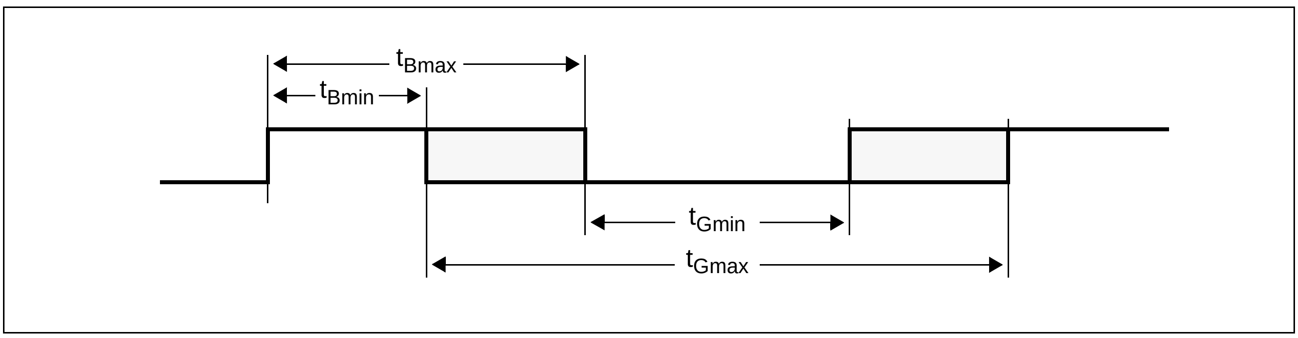


Figure 14 CPT Detector - Cooked Mode

The status bit is defined as follows:

Table 11 CPT Detector Result

Register	# of Bits	Name	Comment
STATUS	1	CPT	CP tone currently detected [340 Hz; 640 Hz]

CPT is not affected by reading the status word. It is automatically reset when the unit is disabled. Table **12** shows the control register for the CPT detector.

Table 12 CPT Detector Registers

Register	# of Bits	Name	Comment
CPTCTL	1	EN	Unit enable
CPTCTL	1	MD	Mode (cooked, raw)
CPTCTL	5	I1	Input signal selection
CPTMN	8	MINB	Minimum time of a signal burst (t_{Bmin})
CPTMN	8	MING	Minimum time of a signal gap (t_{Gmin})
CPTMX	8	MAXB	Maximum time of a signal burst (t_{Bmax})
CPTMX	8	MAXG	Maximum time of a signal gap (t_{Gmax})
CPTDT	8	DIFB	Maximum difference between consecutive bursts
CPTDT	8	DIFG	Maximum difference between consecutive gaps
CPTTR	3	NUM	Number of cycles (cooked mode), 0 (raw mode)
CPTTR	8	MIN	Minimum signal level to detect tones
CPTTR	4	SN	Minimal signal-to-noise ratio

If any condition is violated during a sequence of cycles the timing checker is reset and restarts with the next valid burst.

Note: In cooked mode CPT is set with the first burst after the programmed number of cycles has been detected.

Note: The number of cycles must be set to zero in raw mode.

2.1.6 Caller ID Decoder

The caller ID decoder is basically a 1200 baud modem (FSK, demodulation only). The bit stream is formatted by a subsequent UART and the data is available in a data register along with status information (figure **15**).

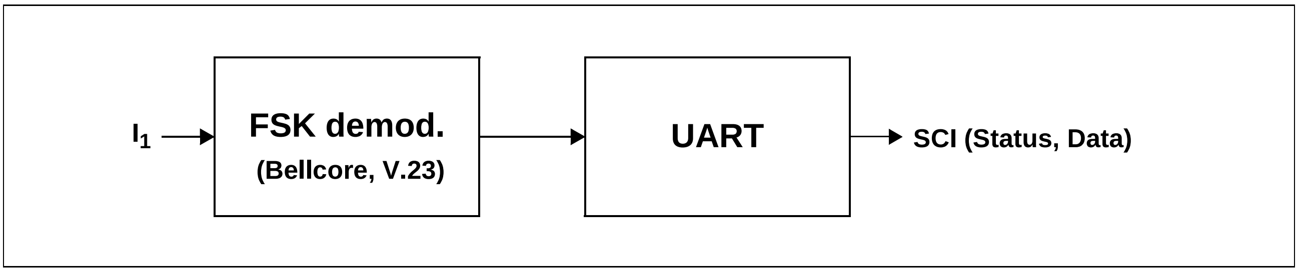


Figure 15 Caller ID Decoder - Block Diagram

The FSK demodulator supports two modes according to table **13**. The appropriate mode is detected automatically.

Table 13 Caller ID Decoder Modes

Mode	Mark (Hz)	Space (Hz)	Comment
1	1200	2200	Bellcore
2	1300	2100	V.23

The CID decoder does not interpret the data received. Each byte received is placed into the CIDCTL register (table **15**). The status byte of the PSB 2168 is updated (table **14**).

Table 14 Caller ID Decoder Status

Register	# of Bits	Name	Comment
STATUS	1	CIA	CID byte received
STATUS	1	CD	Carrier Detected

CIA and CD are cleared when the unit is disabled. In addition, CIA is cleared when CIDCTL0 is read.

Table 15 Caller ID Decoder Registers

Register	# of Bits	Name	Comment
CIDCTL0	1	EN	Unit enable
CIDCTL0	5	I1	Input signal selection
CIDCTL0	8	DATA	Last CID data byte received

Table 15 Caller ID Decoder Registers

Register	# of Bits	Name	Comment
CIDCTL1	5	NMSS	Number of mark/space sequences necessary for successful detection of carrier detect
CIDCTL1	6	NMB	Number of mark bits necessary before space of first byte after carrier detect
CIDCTL1	5	MIN	Minimum signal level for CID detection

When the CID unit is enabled, it first waits for a channel seizure signal consisting of a series of alternating space and mark signals. The number of spaces and marks that have to be received without errors before the PSB 2168 reports a carrier detect by setting status bit CD can be programmed.

Channel seizure must be followed by at least 16 continuous mark signals. The first space signal detected is then regarded as the start bit of the first message byte.

The interpretation of the data, including message type, length and checksum is completely left to the controller. The CID unit should be disabled as soon as the complete information has been received as it cannot detect the end of the transmission by itself.

Note: Some caller ID mechanism may require additional external components for DC decoupling. These tasks must be handled by the controller.

Note: The controller is responsible for selecting and storing parts of the CID as needed.

2.1.7 DTMF Generator

The DTMF generator can generate single or dual tones with programmable frequency and gain. This unit is primarily used to generate the common DTMF tones but can also be used for signalling or other user defined tones. A block diagram is shown in figure **16**.

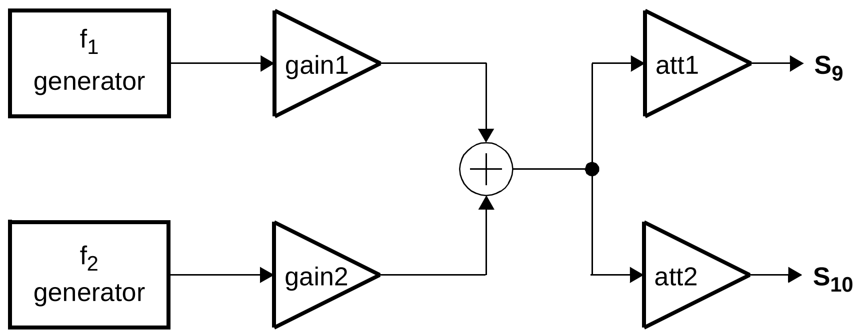


Figure 16 DTMF Generator - Block Diagram

Both generators and amplifiers are identical. There are two modes for programming the generators, cooked mode and raw mode. In cooked mode, the standard DTMF frequencies are generated by programming a single 4 bit code. In raw mode, the frequency of each generator/amplifier can be programmed individually by a separate register. The unit has two outputs which provide the same signal but with individually programmable attenuation. Table **16** shows the parameters of this unit.

Table 16 DTMF Generator Registers

Register	# of Bits	Name	Comment
DGCTL	1	EN	Enable for generators
DGCTL	1	MD	Mode (cooked/raw)
DGCTL	4	DTC	DTMF code (cooked mode)
DGF1	15	FRQ1	Frequency of generator 1
DGF2	15	FRQ2	Frequency of generator 2
DGL	7	LEV1	Level of signal for generator 1
DGL	7	LEV2	Level of signal for generator 2
DGATT	8	ATT1	Attenuation of S_9
DGATT	8	ATT2	Attenuation of S_{10}

Note: DGF1 and DGF2 are undefined when cooked mode is used and must not be written.

2.1.8 Speech Coder

The speech coder (figure **17**) has two input signals I_1 and I_2. The first signal (I_1) is fed to the coder while the second signal (I2) is used as a reference signal for voice controlled recording. The signal I_1 can be coded by either a High Quality coder or a Long Play coder.

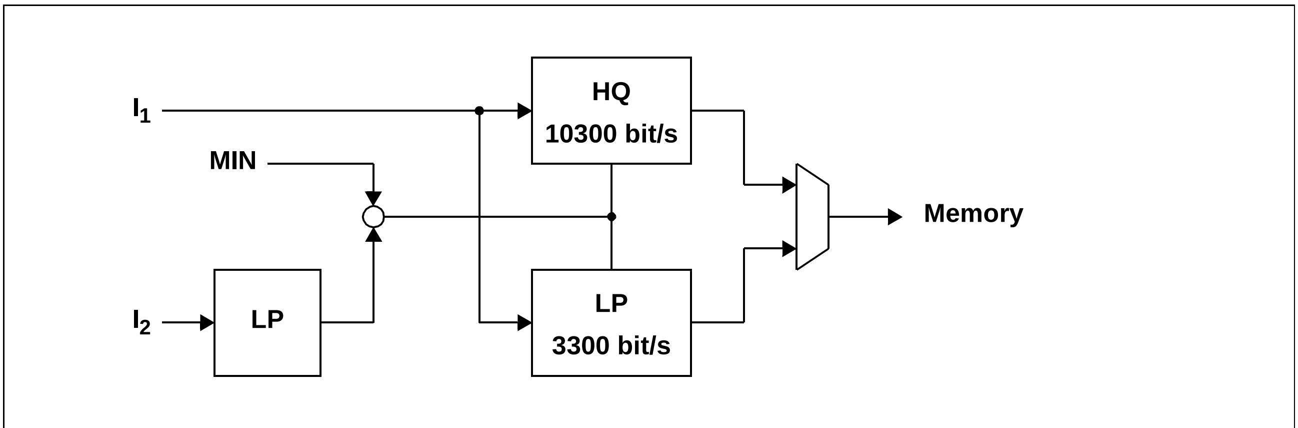


Figure 17 Speech Coder - Block Diagram

In High Quality the output data stream runs at a fixed rate of 10300 bit/s and provides excellent speech quality. In Long Play mode, the output data stream is further reduced to an average of 3300 bit/s while still maintaining good quality.

Data is written starting at the current file pointer and the file pointer is advanced as needed. In case of any memory error (e.g. memory full) a file error is indicated and the coder is disabled. The controller must subsequently close the file.

The coder can be switched on the fly. However, it may take up to 60 ms until the switch is executed. The controller must therefore wait for at least this time until issuing another command that relies on the mode switch. No audio data is lost during switching.

The signal I_2 is first filtered by a low pass LP1 with programmable time constant and then compared to a reference level MIN. If the filtered signal exceeds MIN, then the status bit SD (table **17**) is set immediately. If the filtered signal has been smaller than MIN for a programmable time TIME then the status bit SD is reset.

The coder can be enabled in permanent mode or in voice recognition mode. In permanent mode, the coder starts immediately and compresses all input data continuously. The current state of the status bit SD does not affect the coder.

In voice recognition mode, the coder is automatically started on the first transition of the status bit from 0 to 1. Once the coder has started it remains active until disabled.

Table 17 Speech Coder Status

Register	# of Bits	Name	Comment
STATUS	1	SD	Speech detected

The operation of the speech coder is defined according to table **18**.

Table 18 Speech Coder Registers

Register	# of Bits	Name	Comment
SCCTL	1	EN	Enable speech coder
SCCTL	1	HQ	High quality mode
SCCTL	1	VC	Voice controlled recording
SCCTL	5	I1	Input signal 1 selection
SCCTL	5	I2	Input signal 2 selection
SCCT2	8	MIN	Minimal signal level for speech detection
SCCT2	8	TIME	Minimum time for reset of SD
SCCT3	8	LP	Time constant for low-pass

Note: The peak data rate in LP mode is 4800 bit/s.

Note: Both HQ and LP mode will not produce identical bit streams after a coding/decoding cycle.

2.1.9 Speech Decoder

The speech decoder (figure **18**) decompresses the data previously coded by the speech coder unit and delivers a standard 128 kbit/s data stream.

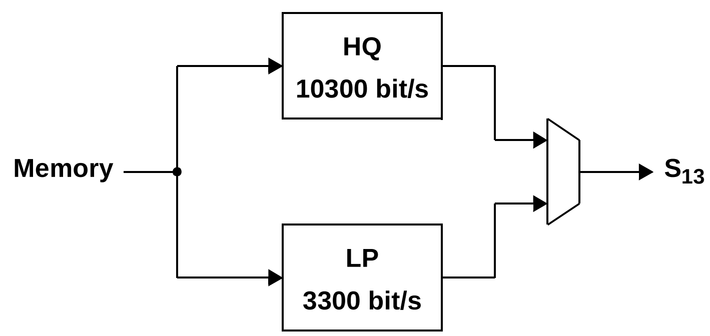


Figure 18 Speech Decoder - Block Diagram

The decoder supports fast (1.5 and 2.0 times) and slow (0.5 times) motion independent of the selected quality. The decoder requests input data as needed at a variable rate. Table **19** shows the signal and mode selection for the speech decoder.

Table 19 Speech Decoder Registers

Register	# of Bits	Name	Comment
SDCTL	1	EN	Enable speech decoder
SDCTL	2	SPEED	Selection of playback speed

Data reading starts at the location of the current file pointer. The file pointer is updated during speech decoding. If the end of the file is reached, the decoder is automatically disabled. The PSB 2168 automatically resets SDCTL:EN at this point.

2.1.10 Digital Interface

There are two almost identical interfaces at the digital side as shown in figure **19**. The only difference between these two interfaces is that only channel 1 supports the SSDI mode.

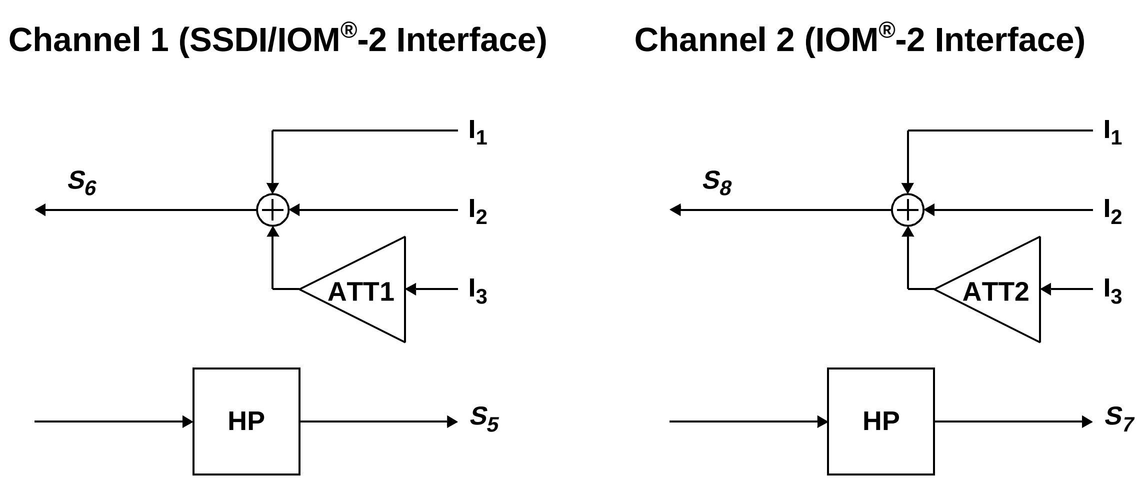


Figure 19 Digital Interface - Block Diagram

Each outgoing signal can be the sum of two signals with no attenuation and one signal with programmable attenuation (ATT). The attenuator can be used for artificial echo if there is none externally provided (e.g. ISDN application). Each input can be passed through an optional high-pass (HP). The associated registers are shown in table **20**.

Table 20 Digital Interface Registers

Register	# of Bits	Name	Comment
IFS3	5	I1	Input signal 1 for S_6
IFS3	5	I2	Input signal 2 for S_6
IFS3	5	I3	Input signal 3 for S_6
IFS3	1	HP	High-pass for S_5
IFS4	5	I1	Input signal 1 for S_8
IFS4	5	I2	Input signal 2 for S_8
IFS4	5	I3	Input signal 3 for S_8
IFS4	1	HP	High-pass for S_7

Table 20 Digital Interface Registers

Register	# of Bits	Name	Comment
IFG5	8	ATT1	Attenuation for input signal I3 (Channel 1)
IFG5	8	ATT2	Attenuation for input signal I3 (Channel 2)

2.1.11 Universal Attenuator

The PSB 2168 contains an universal attenuator that can be connected to any signal (e.g. for sidetone gain in ISDN applications).

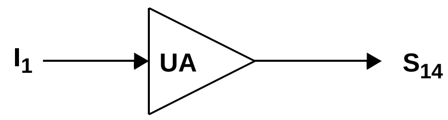


Figure 20 Universal Attenuator - Block Diagram

Table **21** shows the associated register.

Table 21 Universal Attenuator Registers

Register	# of Bits	Name	Comment
UA	8	ATT	Attenuation for UA
UA	5	I1	Input signal for UA

2.1.12 Automatic Gain Control Unit

In addition to the universal attenuator with programmable but fixed gain the PSB 2168 contains an amplifier with automatic gain control (AGC). The AGC is preceeded by a signal summation point for two input signals. One of the input signals can be attenuated.

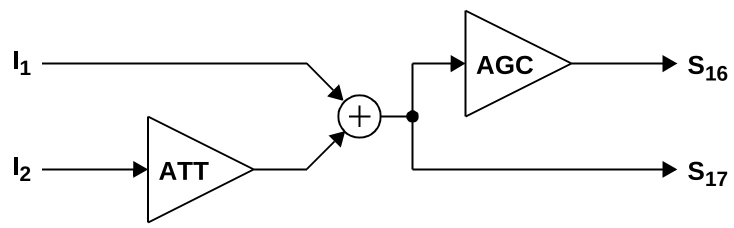


Figure 21 Automatic Gain Control Unit - Block Diagram

Furthermore the signal after the summation point is available. Besides providing a general signal summation (S_{16} not used) this signal is especially useful if the AGC unit provides the input signal for the speech coder. In this case S_{17} can be used as a reference signal for voice controlled recording.

Operation of the AGC depends on a threshold level defined by the parameter COM (value relative to the maximum PCM-value). The bold line in Figure **22** depicts the steady-state output level of the AGC as a function of the input level.

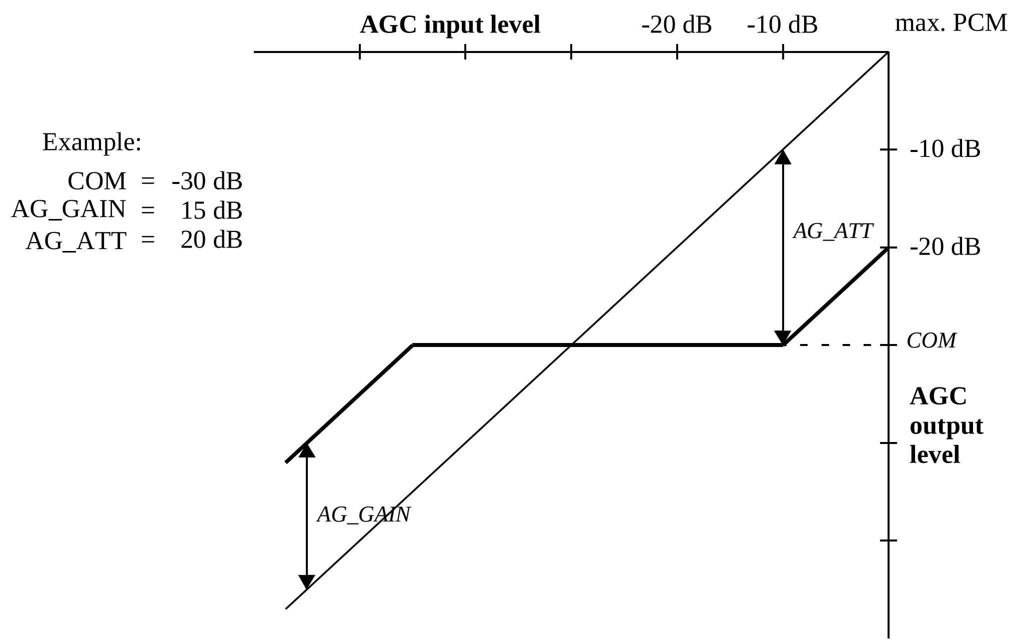


Figure 22 Automatic Gain Control Unit - Steady State Characteristic

The regulation speed is controlled by SPEEDH for signal amplitudes above the threshold and SPEEDL for amplitudes below. Usually SPEEDH will be chosen to be at least 10 times faster than SPEEDL. The AGC reacts faster for higher values of SPEEDH (SPEEDL). The current gain/attenuation of the AGC can be read at any time. An additional low pass with time constant LP is provided to avoid an immediate response of the AGC to very short signal bursts.

Furthermore the AGC contains a comparator that starts and stops the gain regulation. The signal after the summation point (S17) is filtered by a peak detector with time constant DEC for decay. Then the signal is compared to a programmable limit LIM. Regulation takes only place when the filtered signal exceeds the limit.

Table **22** shows the associated registers.

Table 22 Automatic Gain Control Registers

Register	# of Bits	Name	Comment
AGCCTL	1	EN	Enable
AGCCTL	5	I1	Input signal 1 for AGC
AGCCTL	5	I2	Input signal 2 for AGC
AGCATT	15	ATT	Attenuation for I_2
AGC1	8	AG_INIT	Initial AGC gain/attenuation
AGC1	8	COM	Compare level rel. to max. PCM-value
AGC2	8	SPEEDL	Change rate for lower levels
AGC2	8	SPEEDH	Change rate for higher level
AGC3	8	AG_ATT	Attenuation range
AGC3	7	AG_GAIN	Gain range
AGC4	7	DEC	Peak detector time constant
AGC4	8	LIM	Comparator minimal signal level
AGC5	7	LP	AGC low pass time constant

2.1.13 Equalizer

The PSB 2168 also provides an equalizer that can be inserted into any signal path. The main application for the equalizer is the adaption to the frequency characteristics of the microphone, transducer or loudspeaker.

The equalizer consists of an IIR filter followed by an FIR filter as shown in figure **23**.

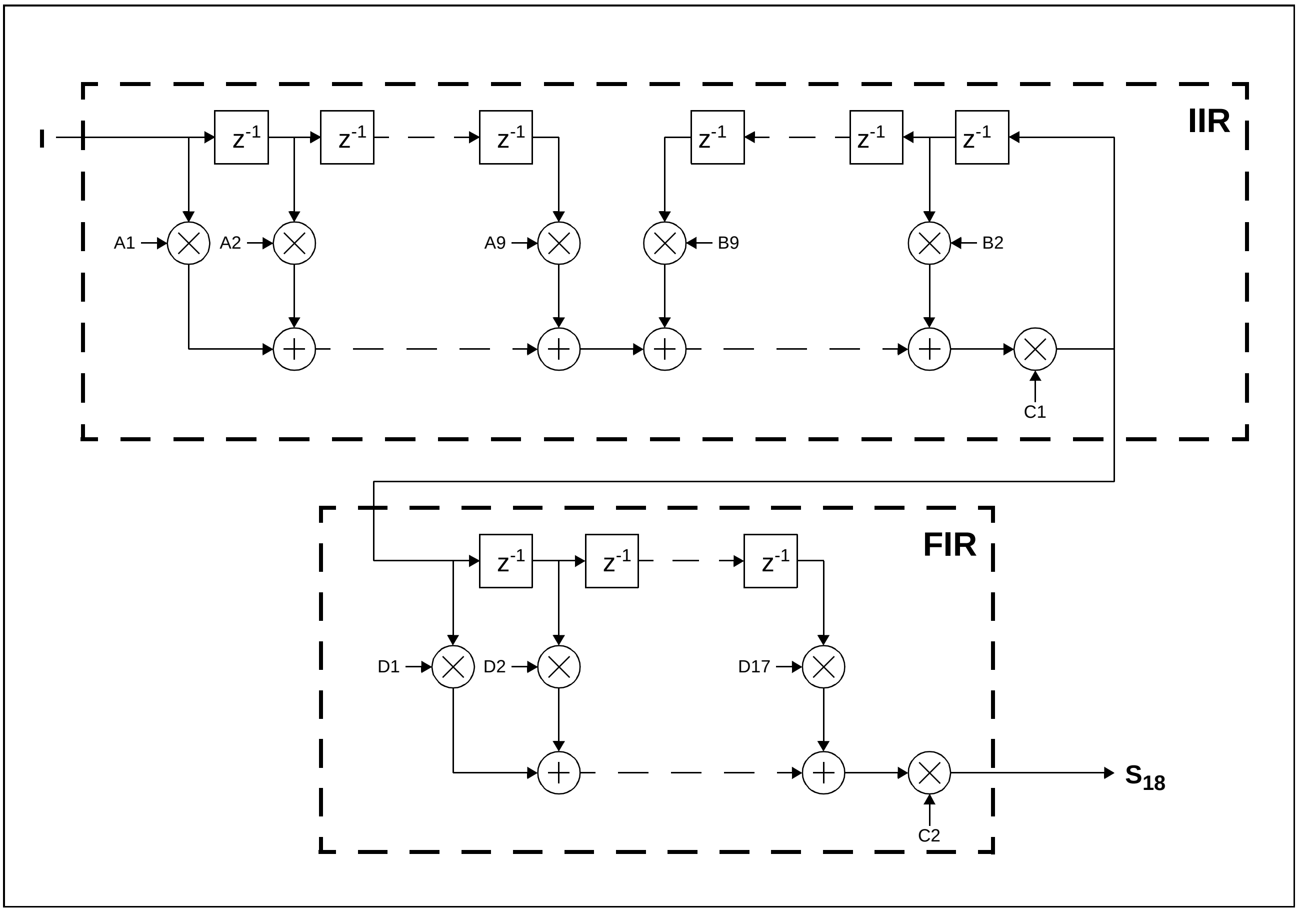


Figure 23 Equalizer - Block Diagram

The coefficients A_1-A_9, B_2-B_9 and C_1 belong to the IIR filter, the coefficients D_1-D_{17} and C_2 belong to the FIR filter. Table **23** shows the registers associated with the equalizer.

Table 23 Equalizer Registers

Register	# of Bits	Name	Comment
FCFCTL	1	EN	Enable
FCFCTL	5	I	Input signal for equalizer
FCFCTL	6	ADR	Filter coefficient address
FCFCOF	16		Filter coefficient data

Due to the multitude of coefficients the PSB 2168 uses an indirect addressing scheme for reading or writing an individual coefficient. The address of the coefficient is given by ADR and the actual value is read or written to register FCFCOF.

In order to ease programming the PSB 2168 automatically increments the address ADR after each access to FCFCOF.

Note: Any access to an out-of-range address automatically resets FCFCTL:ADR.

2.2 Memory Management

This section describes the memory management provided by the PSB 2168. As figure **24** shows, three units can access the external memory. During recording, the speech coder can write compressed speech data into the external memory. For playback, the speech decoder reads compressed speech data from external memory. In addition, the microcontroller can directly access the memory by the SCI interface.

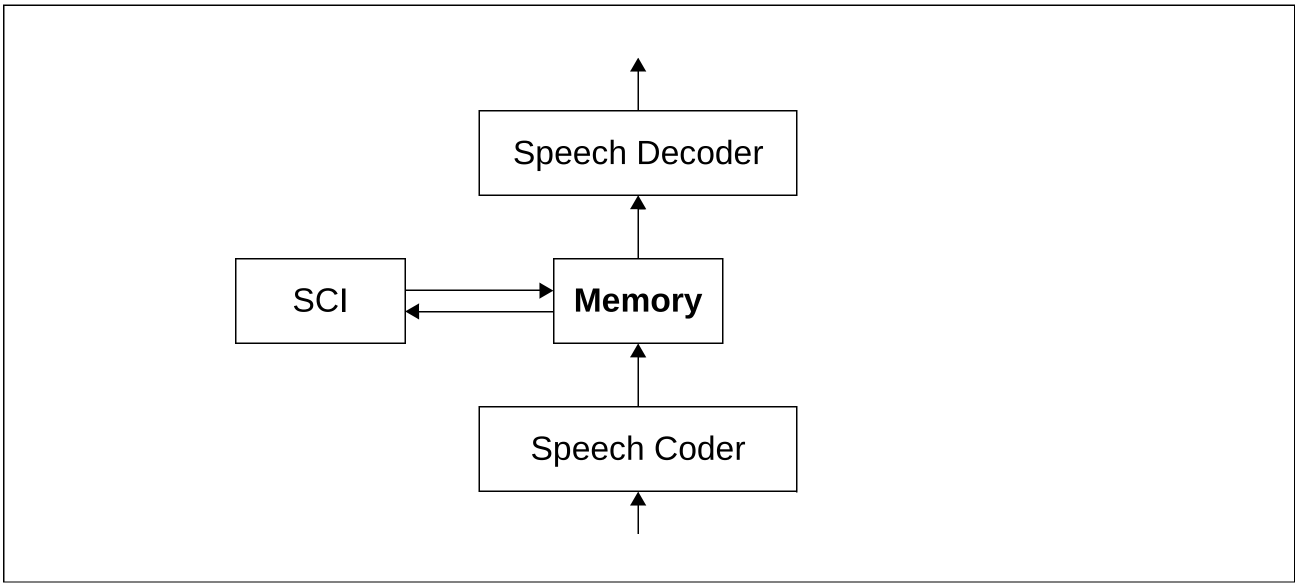


Figure 24 Memory Management - Data Flow

The memory is organized as a file system. For each memory space (R/W-memory and voice prompt memory) the PSB 2168 maintains a directory with 255 file descriptors (figure **25**).

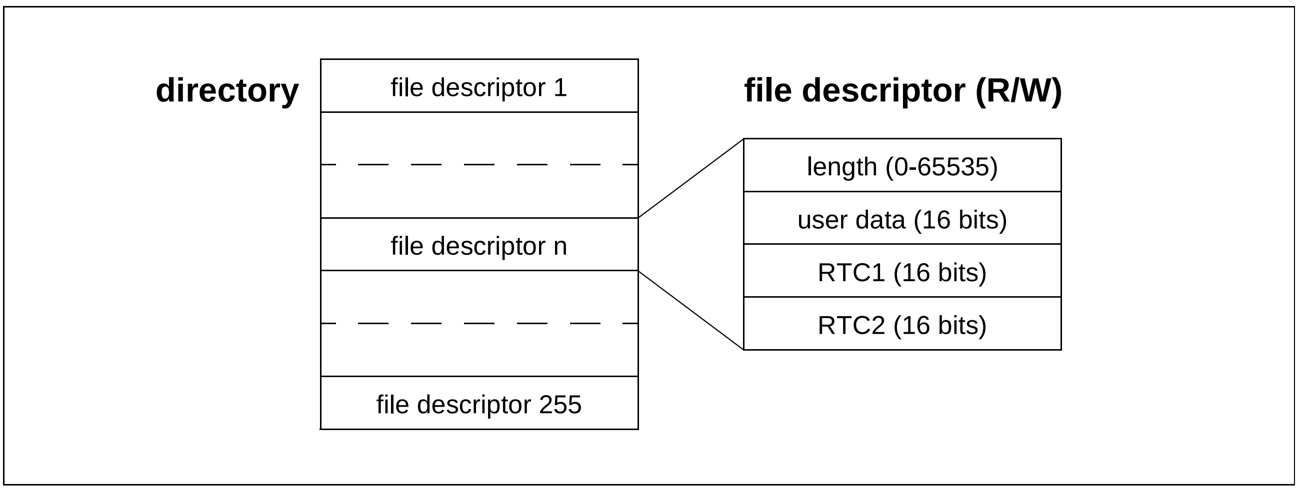


Figure 25 Memory Management - Directory Structure

The directories must be created after each power failure for volatile R/W-memory. All file descriptors are cleared (all words zero). For non-volatile memory, the directories have to be created only once. If the directories already exist, the memory has just to be activated after a reset. The file descriptors are not changed in this case.

All commands that access the other fields or involve a write access must not be used in voice prompt memory space.

2.2.1 File Definition and Access

A file is a linear sequence of units and can be accessed in two modes: binary and audio. In binary mode, a unit is a word. In audio mode, a unit is a variable number of words representing 30 ms of uncompressed speech. A file can contain at most 65535 units. Figure **26** shows an audio file containing 100 audio units. The length of the message is therefore 3 s.

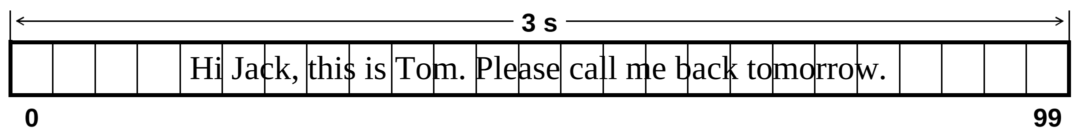


Figure 26 Audio File Organization - Example

Figure **27** shows a binary file of 11 words containing a phonebook (with only two entries).

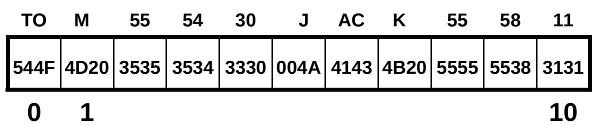


Figure 27 Binary File Organization - Example

There is one special file in the voice prompt directory (referenced by file number 255) which is intended for a large number of phrases and hence has a different organization.This file exists only in the directory for the voice prompt memory. It consists of up to 2048 phrases of arbitrary individual length. The actual number of units within an individual phrase is determined during creation and cannot be altered afterwards. Phrases can be combined in any sequence without intermediate noise or gaps.

Figure **28** shows a phrase file containing a total of five phrases.

Figure 28 Phrase File Organization - Example

Before an access to a file can take place, the file must be opened with the following information:

1. memory space (messages or voice prompts)
2. file number
3. access mode

These parameters remain effective until the next open command is given or, in case of the file pointer, until a file access. All other files are closed and cannot be accessed. The file with file number 0 is not a physical file. Opening this file closes all physical files.

The PSB 2168 provides four registers for file access and two bits within the STATUS register. Table **24** shows these registers.

Table 24 Memory Management Registers

Register	# of Bits	Comment
FCMD	16	Command to execute
FCTL	16	Access mode and file number
FDATA	16	Data transfer and additional parameters
FPTR	16 (11)	File pointer (phrase selector)
STATUS	16	Busy and Error indication

The status register contains two flags (table **25**) to indicate if currently a file command is under execution and if the last file command terminated without error. A new command must not be written to FCMD while the last one is still running (STATUS:BSY=1). The only command that can be aborted is Compress File.

Table 25 Memory Management Status

Register	# of Bits	Name	Comment
STATUS	1	BSY	File command or decoder/encoder still running
STATUS	1	ERR	File command completed/aborted with error

Writing to FCMD also resets the error bit in the status register.

Table **26** shows the parameters defining the access mode and the access location. All parameters can only be written when no file command is currently running. They become effective after the completion of an open command. If another unit (e.g. speech coder) accesses the file, the file pointer is updated automatically. Therefore the controller can monitor the progress of recording or playing by reading the file pointer.

Table 26 Memory Management Parameters

Register	# of Bits	Name	Comment
FCTL	1	MS	Memory space (R/W or voice prompt)
FCTL	1	MD	Access mode (audio or binary)
FCTL	1	TS	Write timestamp (file open only)
FCTL	8	FNO	File number (active file)
FPTR	16		File pointer or phrase selector

Commands are written to the FCMD register. The busy bit in the STATUS register is set within 125µs. The command may start execution after a delay, however (see section **2.2.5**). Some commands require additional parameters which are written prior to the command into the specified registers. Data transfer is done by the register FDATA (both reading and writing).

2.2.2 User Data Word

The user data word consists of 12 bits that can be read or written by the user, two bits (R) that are reserved for future use and two read-only bits (D,M) which indicate the status of a file.

15				0
D	M	R	R	User Definable

If D is set, the file is marked for deletion and should not be used any more. This bit is maintained by the PSB 2168 for housekeeping.

2.2.3 High Level Memory Management Commands

This section describes each of the high level memory management commands in detail. These commands are sufficient for normal operation of an answering machine. In addition, there are four low level commands (section **2.2.4**). These commands are only required for special tasks like in-system reprogramming of the voice prompt area.

2.2.3.1 Initialize

This command creates a directory, sets the external memory configuration and delivers the size of usable memory in 1 kByte blocks. Furthermore the voice prompt memory space is scanned for a valid directory. The PSB 2168 can either create an empty directory from scratch or leave the first n files of an existing directory untouched while deleting the remaining files (ARAM/DRAM only). This option is useful if due to an unexpected event (e.g. power loss during recording) some data is corrupted. In that case vital system information can still be recovered if it has been stored in the first files.

Table 27 Initialize Memory Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Initialize command code
FCMD	1	IN	Confirmation for Initialization
FCTL	8	FNO	0: delete no file 1: delete all files n: delete starting with file n
CCTL	2	MT	Type of R/W memory (DRAM, Flash)
CCTL	1	MQ	Quality of R/W memory (Audio, Normal)
CCTL	1	MV	Scan for voice prompt directory

Table 28 Initialize Memory Results

Register	# of Bits	Name	Comment
FDATA	16		Number of usable 1kByte blocks in R/W memory

Possible Errors:

- no R/W memory found
- more than 59 bad blocks (flash and ARAM)
- voice prompt directory requested, but not detected

Note: This command must be given only once for flash devices.

2.2.3.2 Activate

This command activates an existing directory, sets the external memory configuration and delivers the size of usable memory in 1 kByte blocks. Furthermore the voice prompt memory space is scanned for a valid directory. Upon activation the PSB 2168 checks (in case of ARAM/DRAM only) the consistency of the directory in R/W memory space. It returns the first file that contains corrupted data (if any). If corrupted data is detected an initialization should be performed with the same file number as an input parameter.

Table 29 Activate Memory Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Activate command code
CCTL	2	MT	Type of R/W memory (DRAM, Flash)
CCTL	1	MQ	Quality of R/W memory (Audio, Normal)
CCTL	1	MV	Voice prompt directory available

Table 30 Activate Memory Results

Register	# of Bits	Name	Comment
FDATA	16		Number of usable 1 kByte blocks in R/W memory
FCTL	8	FNO	n: number of first corrupted file

Possible error conditions:

- no memory connected
- no directory found
- device ID wrong (flash only)
- corrupted files found (see FCTL:FNO)
- directory corrupted

This command can have three types of result as shown in table **31**.

Table 31 Activate Memory Result Interpretation

Result	STATUS: ERR	FCTL: FNO	Comment
no error	0	0	Command successful, memory activated.
soft error	1	n	The first n-1 files are O.K. The memory is activated.
hard error	1	1	The memory is not activated due to a hard error.

2.2.3.3 Open File

A specific file is opened for subsequent accesses with the specified access mode. Opening a new file automatically closes the currently open file and clears the file pointer. Opening file number 0 can be used to close all physical files. If the TS flag is set, the current content of RTC1 and RTC2 is written to the appropriate fields of the file descriptor in order to provide a timestamp.

Table 32 Open File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Open command code
FCTL	1	MS	Memory space (R/W, voice prompt)
FCTL	1	MD	Access mode (audio or binary)
FCTL	1	TS	Write timestamp
FCTL	8	FNO	File number <fno>

Possible error conditions:

- selected file marked for deletion, but not yet deleted by garbage collection
- memory space invalid
- new file selected, but memory full
- <fno> exceeds number of prompts (in voice prompt space only)
- wrong access mode selected for existing file

Note: In case of flash memory existing ones in the entries RTC1/RTC2 of the file descriptor cannot be altered. Therefore TS should be set only once during the lifetime of a file.

2.2.3.4 Open Next Free File

The next free file is opened for subsequent write accesses with the specified access mode. The search starts at the specified file number. If the TS flag is set, the current content of RTC1 and RTC2 is written to the appropriate fields of the file descriptor in order to provide a timestamp. If a free file has been found, the file is opened and the file number is returned in FCTL:FNO. Otherwise an error is reported.

Table 33 Open Next Free File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Open Next Free File command code
FCTL	1	MD	Access mode (audio or binary)

Table 33 Open Next Free File Parameters

Register	# of Bits	Name	Comment
FCTL	1	TS	Write timestamp
FCTL	8	FNO	Starting point (>0)

Table 34 Open Next Free File Results

Register	# of Bits	Name	Comment
FCTL	8	FNO	File number

Possible error conditions:

- no unused file found
- memory full

Note: In case of flash memory existing ones cannot be altered. Therefore TS should be set only once during the lifetime of a file.

Note: R/W-memory must be selected (FCTL:MS). Otherwise the result is unpredictable.

2.2.3.5 Seek

The file pointer of the currently opened file is set to the specified position. If the current file is the phrase file the PSB 2168 starts the speech decoder immediately after the seek is finished. This is done by simply enabling the decoder. All other settings of the decoder remain unaffected. The BSY bit is first set during the file command. It is then reset for a short period until the speech decoder is enabled internally. It is then set again while the decoder is running and finally reset when the phrase is finished.

Table 35 Seek Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Seek command code
FPTR	16 (11)		File pointer (phrase selector)

Possible error conditions:

- file pointer out of range
- phrase number out of range

2.2.3.6 Cut File

All units starting with the unit addressed by the file pointer are removed from the file. If all units are deleted the file is marked for deletion (see user data word). However, the associated file descriptor and memory space are released only after a subsequent garbage collection.

Table 36 Cut File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Cut command code
FPTR	16		Position of first unit to delete

Possible error conditions:

- file pointer out of range
- voice prompt memory selected

2.2.3.7 Compress File

An audio file that has been recorded in HQ mode can be recoded using LP mode. This reduces the file size to approximately one third of the original size. The speech quality, however, is somewhat lower compared to a signal that has been recorded in LP mode in the first place. This command can be aborted at any time and resumed later without loss of information. Prior to this command all files must be closed. Table **37** shows the parameters for this command.

Table 37 Compress File Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Compress command code
FCTL	8	FNO	File number <fno>

Possible error conditions:

- <fno> invalid
- another file currently open
- binary file selected

2.2.3.8 Memory Status

This command returns the number of available 1 kB blocks in R/W memory space.

Table 38 Memory Status Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Memory status code

Table 39 Memory Status Results

Register	# of Bits	Name	Comment
FDATA	16	FREE	Number of free blocks

Possible error conditions:

- file open

2.2.3.9 Garbage Collection

This command initiates a garbage collection. Until a garbage collection files that are marked for deletion still occupy the associated file descriptor and memory space. After the garbage collection these file descriptors and the associated memory space are available again. This command can optionally remap the directory. In this mode the remaining file descriptors are remapped to form a contiguous block starting with file number 1. The original order is preserved. This command requires that all files are closed, i.e. file 0 is opened. Independently of the selected directory only the read/write directory is used.

Table 40 Garbage Collection Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Garbage Collection Command Code
FCMD	1	RD	Remap Directory

Possible error conditions:

- file open

2.2.3.10 Access File Descriptor

By this command the length, user data word and RTC1/RTC2 of a file descriptor can be read. The user data word can also be written. The file or the other entries of the file descriptor are not affected by this command.

Table 41 Access File Descriptor Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Read Access or Write Access command code
FDATA	16		User data (write access only)

Table 42 Access File Descriptor Results

Register	# of Bits	Name	Comment
FDATA	16		Content of selected entry (read access only)

Possible error conditions:

- none

Note: In case of flash memory bits already set to 1 cannot be altered.

Note: Do not use this command with the phrase file (fno = 255).

2.2.3.11 Read Data

This command can be used in binary access mode only. A single word is read at the position given by the file pointer. The file pointer can be set by the Seek command. The file pointer is advanced by one word automatically.

Table 43 Read Data Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Read Data Command Code

Table 44 Read Data Results

Register	# of Bits	Name	Comment
FDATA	16		Data word

Possible error conditions:

- file pointer out of range
- phrase file selected
- audio file selected

2.2.3.12 Write Data

This commands can be used in binary access mode only. A single word is written at the position of the file pointer. The file pointer is advanced by one word automatically. Note, that for FLASH memory only zeroes can be overwritten by ones. This restriction occurs only if an already used value within an existing file is to be overwritten.

Table 45 Write Data Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Access Mode Command Code (including mode)
FDATA	16		Data word

Possible error conditions:

- file pointer out of range (for existing files only)
- voice prompt memory selected
- memory full
- audio file selected

2.2.4 Low Level Memory Management Commands

These commands allow the direct access of any location (single word) of the external memory. Additionally it is possible to erase any block in case of a flash device. These commands should not be used during normal operation as they may interfere with the file system. No file must be open when one of these commands is given.

The primary use of these commands is the in-system programming of a flash device with voice prompts. Please refer to the appropriate Application Notes.

2.2.4.1 Set Address

This command sets the 24 bit address pointer APTR. Only the address bits A_8-A_{23} are set, the address bits A_0-A_7 are automatically cleared.

Table 46 Set Address Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Set Address command code
FDATA	16	ADR	Address bits A_8-A_{23} of address pointer APTR

Possible error conditions:

- file open

2.2.4.2 DMA Read

This command reads a single word addressed by APTR. After the read access APTR is automatically incremented by one. Table **47** shows the parameters for this command.

Table 47 DMA Read Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	DMA Read command code

Table 48 DMA Read Results

Register	# of Bits	Name	Comment
FDATA	16	DATA	Data read from address APTR.

Possible error conditions:

- file open

2.2.4.3 DMA Write

This command writes a single word to the location addressed by APTR. After the write access APTR is automatically incremented by one. Table **49** shows the parameters for this command.

Table 49 DMA Write Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	DMA Write command code
FDATA	16	DATA	Data to be written to APTR

Possible error conditions:

- file open

Note: If flash memory is connected the actual write is only performed when the last word within a page is written. Until then the data is merely buffered in the flash device. Please check the flash memory data sheets on page size.

2.2.4.4 Block Erase

This command erases the physical block which includes the address given by APTR. The actual amount of memory erased by this command depends on the block size of the flash device. Table **50** shows the parameters for this command.

Table 50 Block Erase Parameters

Register	# of Bits	Name	Comment
FCMD	5	CMD	Block Erase command code

Possible error conditions:

- file open
- ARAM/DRAM configured

2.2.5 Execution Time

The execution time of the file commands is determined by four factors:

1. Internal state of the PSB 2168
2. Memory configuration
3. Memory state
4. Individual characteristics of the memory devices

Therefore there is no general formula for an exact calculation of the execution time for file commands. For ARAM/DRAM items three and four are not significant as the memory access timing is always fixed and no additional delay is incurred for erasing memory blocks. However, the amount of memory has significant impact on the initialization in case of ARAM and flash.

For flash devices the particular location of a write access in combination with the internal organization of the memory device may result in a block erase and subsequent write accesses in order to copy data. In this case the individual erase and write timing of the attached devices also prolongs the execution time.

The first factor, the internal state of the PSB 2168, can influence all file commands regardless of the memory type attached. In general the PSB 2168 may delay any file command by up to 30 ms. However, it is possible to skip this delay if the following conditions hold:

1. The command is not *initialize/activate*
2. Neither the DTMF detector nor the speech coder nor the speech decoder are running

If neither condition is violated then the PSB 2168 can be forced to start command execution immediately. This is done by setting the EIE bit in the FCMD register along with the command code.

Table **51** gives an indication of the execution time for two typical memory configurations.

Table 51 Execution Times

Command	ARAM (4 MBit)	KM29LV040
Initialize	40 s[1)]	<11 s
Activate	< 10 ms	3 s
Open File /Open Next Free File	<10 ms	<26 ms
Seek (within 4 MBit File)	<0.5 s	<0.5 s
Seek (within phrase file)	<1 ms	<1 ms
Cut File	<5 ms	<5 ms
Compress File	#units * 30 ms	#units * 30 ms
Access File Descriptor	<10 ms	<10 ms

Table 51 Execution Times

Command	ARAM (4 MBit)	KM29LV040
Memory Status	<10 ms	<10 ms
Read/Write Data	<10 ms	<10 ms
Garbage Collection	<20 ms	3 s

[1] less than 20 ms for DRAM

2.2.6 Special Notes on File Commands

1. No MMU commands must be inserted between opening a file and writing data to it, either by writing data to a binary file or by enabling the coder for audio files.
   Therefore reading or writing the file descriptor (e.g. user data word) is only allowed after all data writing has happened.

2. If an audio file has been opened for replay, a Write File Descriptor Command must be followed by a Seek command before the decoder can be enabled.

2.3 Miscellaneous

2.3.1 Real Time Clock

The PSB 2168 supplies a real time clock which maintains time with a resolution of a second and a range of up to a year. There are two registers which contain the current time and date (table **52**).

Table 52 Real Time Clock Registers

Register	# of Bits	Name	Comment
RTC1	6	SEC	Seconds elapsed
RTC1	6	MIN	Minutes elapsed
RTC2	5	HR	Hours elapsed
RTC2	11	DAY	Days elapsed

The real time clock maintains time during normal mode and power down mode only if the auxiliary oscillator OSC is running and the RTC is enabled.

Note: Writing out-of-range values to RTC1 and RTC2 results in undefined operation of the RTC

2.3.2 SPS Control Register

The two SPS outputs (SPS_0, SPS_1) can be used as either general purpose outputs, extended address outputs for Voice Prompt EPROM or as status register outputs. Table **53** shows the associated register.

Table 53 SPS Registers

SPSCTL	1	SP0	Output Value of SPS_0
SPSCTL	1	SP1	Output Value of SPS_1
SPSCTL	3	MODE	Mode of Operation
SPSCTL	4	POS	Position for status register window

When used as status register outputs, the status register bit at position POS appears at SPS_0 and the bit at position POS+1 appears at SPS_1. This mode of operation can be used for debugging purposes or direct polling of status register bits.

2.3.3 Reset and Power Down Mode

The PSB 2168 can be in either reset mode, power down mode or active mode. During reset the PSB 2168 clears the hardware configuration registers and stops both internal and external activity. The address lines MA_0-MA_{15} provide a weak low until they are actually used as address lines (strong outputs) or auxiliary port pins (I/O). In reset mode the hardware configuration registers can be read and written. With the first access to a read/write register the PSB 2168 enters active mode. In this mode the main oscillator is running and normal operation takes place. By setting the power down bit (PD) the PSB 2168 can be brought to power down mode.

Table 54 Power Down Bit

Register	# of Bits	Name	Comment
CCTL	1	PD	power down mode

In power down mode the main oscillator is stopped and, depending on HWCONFIG2:PPM), the memory control lines are released (weak high). Depending on the configuration (ARAM/DRAM, APP) the PSB 2168 may still generate external activity (e.g. refresh cycles). The PSB 2168 enters active mode again upon an access to a read/ write register. Figure **29** shows a state chart of the modes of the PSB 2168.

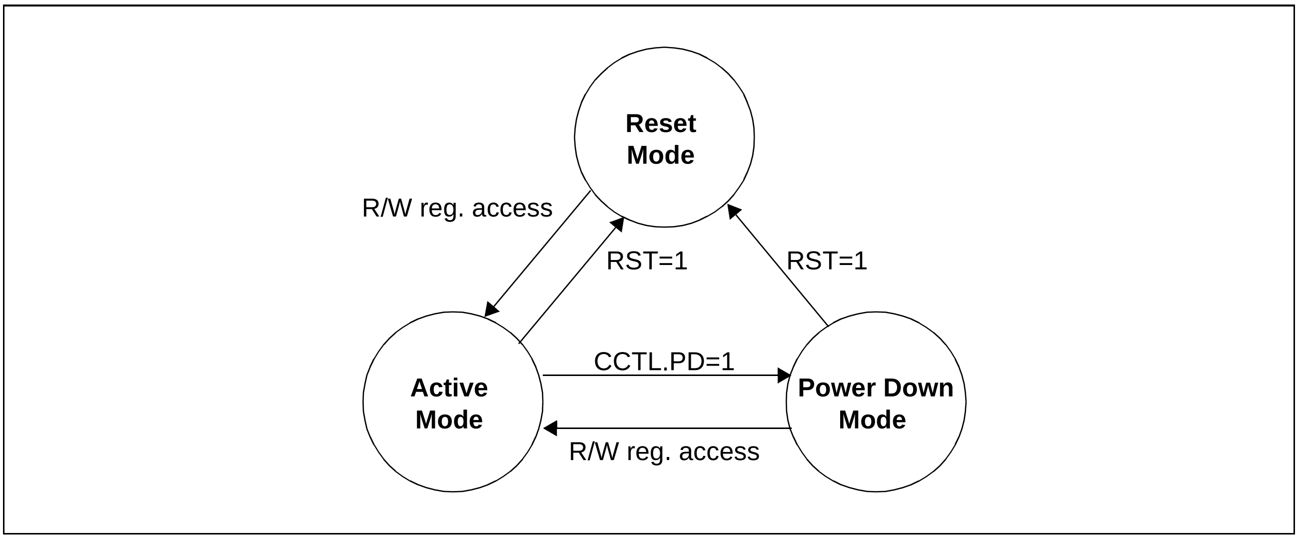


Figure 29 Operation Modes - State Chart

2.3.4 Interrupt

The PSB 2168 can generate an interrupt to inform the host of an update of the STATUS register according to table **55**. An interrupt mask register (INTM) can be used to disable or enable the interrupting capability of each bit of the STATUS register except ABT individually.

Table 55 Interrupt Source Summary

STATUS (old)	STATUS (new)	Set by	Reset by
RDY=0	RDY=1	Command completed	Command issued
CIA=0	CIA=1	New Caller ID byte available	CIDCTL0 read
CD=0	CD=1	Carrier detected	Carrier lost
CD=1	CD=0	Carrier lost	Carrier detected
CPT=0	CPT=1	Call progress tone detected	CPT lost
CPT=1	CPT=0	Call progress tone lost	CPT detected
CNG=0	CNG=1	Fax calling tone detected	CNG lost
DTV=0	DTV=1	DTMF tone detected	DTMF tone lost
DTV=1	DTV=0	DTMF tone lost	DTMF tone detected
ATV=0	ATV=1	Alert tone detected	Alert tone lost
ATV=1	ATV=0	Alert tone lost	Alert tone detected
BSY=1	BSY=0	File command completed	New command issued
SD=0	SD=1	Speech activity detected	Speech activity lost
SD=1	SD=0	Speech activity lost	Speech activity detected

An interrupt is internally generated if any combination of these events occurs and the interrupt is not masked. The interrupt is cleared when the host reads the STATUS register. If a new event occurs while the host reads the status register, the status register is updated *after* the current access is terminated and a new interrupt is generated immediately after the access has ended.

Note: If the internal interrupt occurs after the controller has already selected the device but not yet read the STATUS word, then the STATUS word is updated and the internal interrupt is cleared. Therefore the controller should always evaluate the STATUS word when read.

2.3.5 Abort

If the PSB 2168 cannot continue the current operations in progress (e.g. due to a transient loss of power) it stops operation and initializes all read/write registers to their reset state. After that it sets the ABT bit of the STATUS register and generates an interrupt. The PSB 2168 discards all commands with the exception of a write command to the revision register while ABT is set. Only after the write command to the revision register (with any value) the ABT bit is reset and a reinitialization can take place.

2.3.6 Revision Register

The PSB 2168 contains a revision register. This register is read only and does not influence operation in any way. A write to the revision register clears the ABT bit of the STATUS register but does not alter the content of the revision register.

2.3.7 Hardware Configuration

The PSB 2168 can be adapted to various external hardware configurations by four special registers: HWCONFIG0 to HWCONFIG3. These registers are usually only written once during initialization and must not be changed while the PSB 2168 is in active mode. It is mandatory that the programmed configuration reflects the external hardware for proper operation. Special care must be taken to avoid I/O conflicts or excess current by enabling inputs without an external driving source. Table **56** can be used as a checklist.

Table 56 Hardware Configuration Checklist

Register	Name	Value	Check
HWCONFIG0	$\overline{\text{PFRDY}}$	1	FRDY must not float
HWCONFIG0	OSC	1	OSC1/2 must be connected to a crystal

2.3.8 Auxiliary Clock Generation

The PSB 2168 can generate a data clock (at AFECLK) and a frame synchronization signal (at AFEFS) for typical single channel codecs. The PSB 2168 provides two pairs of frequencies according to table **57**.

Table 57 Auxiliary Clock Generation

CM1	CM0	AFECLK	AFEFS	Comment
0	0	L	L	auxiliary clock generation disabled
0	1	undefined	undefined	reserved
1	0	512 kHz	8 kHz	e.g. MC145480
1	1	1.536 MHz	8 kHz	e.g. TP3054

Note: These frequencies are derived from the main oscillator. Therefore the values listed in the table are only valid for the specified oscillator frequencies (see HWCONFIG1)

2.3.9 Dependencies of Modules

There are some restrictions concerning the modules that can be enabled at the same time (table **58**). A checked cell indicates that the two modules (defined by the row and the column of the cell) must not be enabled at the same time.

Table 58 Dependencies of Modules

	Speech Encoder	Speech Decoder	Line EC (24 ms)	DTMF Detector	File Command
Speech Encoder		X	X		B,O,I
Speech Decoder	X		X[1)]		B,O,I
Line EC (24 ms)	X	X[1)]			B,O
DTMF Detector					B,I
File Command	B,O,I	B,O,I	B,O	B,I	

1) if Speech Decoder is running at slow speed

There are three classes of file commands denoted by the letters B, O and I. Table **59** shows the definition of these classes:

Table 59 File Command Classes

Class	Description
B	Background commands (Activate, Recompress, Garbage Collection, Initialize)
O	Open Commands (Open, Open Next Free File)
I	Any command executed with EIE=1 (i.e. immediate execution)

Examples:

- The line echo canceller (in 24 ms mode) cannot be enabled when the speech decoder is running at slow speed.
- If the DTMF detector is running, none of the background file commands (B) must be executed. In addition, no file command must be executed with immediate execution enabled (I). However, files my be opened and other commands (like read or write) may be executed without immediate execution enabled.

2.4 Interfaces

This section describes the interfaces of the PSB 2168. The PSB 2168 supports both an IOM®-2 interface with single and double clock mode and a strobed serial data interface (SSDI). However, these two interfaces cannot be used simultaneously as they share some pins. Both interfaces are for data transfer only and cannot be used for programming the PSB 2168. Table **60** lists the features of the two alternative interfaces.

Table 60 SSDI vs. IOM®-2 Interface

	IOM®-2	SSDI
Signals	4	6
Channels (bidirectional)	2	1
Code	linear PCM, A-law, μ-law	linear PCM
Synchronization within frame	by timeslot (programmable)	by signal (DXST, DRST)

2.4.1 IOM®-2 Interface

The data stream is partitioned into packets called frames. Each frame is divided into a fixed number of timeslots. Each timeslot is used to transfer 8 bits. Figure **30** shows a commonly used terminal mode (three channels ch_0, ch_1 and ch_2 with four timeslots each). The first timeslot (in figure **30**: B1) is denoted by number 0, the second one (B2) by 1 and so on.

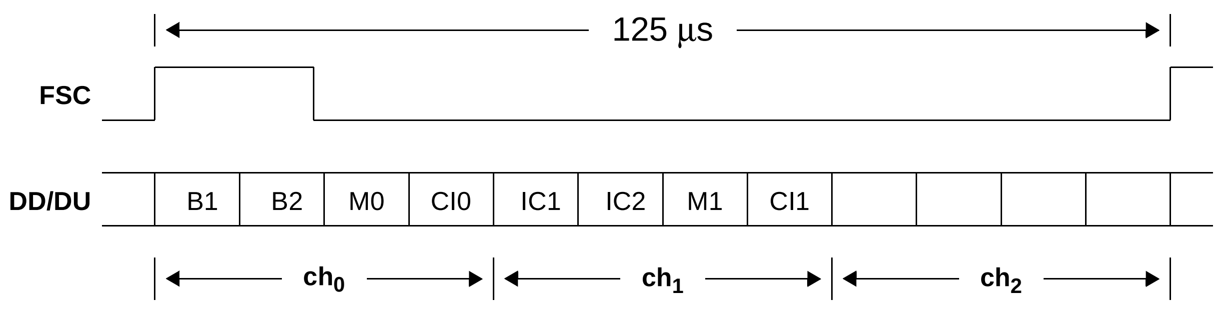


Figure 30 IOM®-2 Interface - Frame Structure

The signal FSC is used to indicate the start of a frame. Figure **31** shows as an example two valid FSC-signals (FSC, FSC*) which both indicate the same clock cycle as the first clock cycle of a new frame (T_1).

Note: Any timeslot (including M0, CI0, ...) can be used for data transfer. However, programming is not supported via the monitor channels.

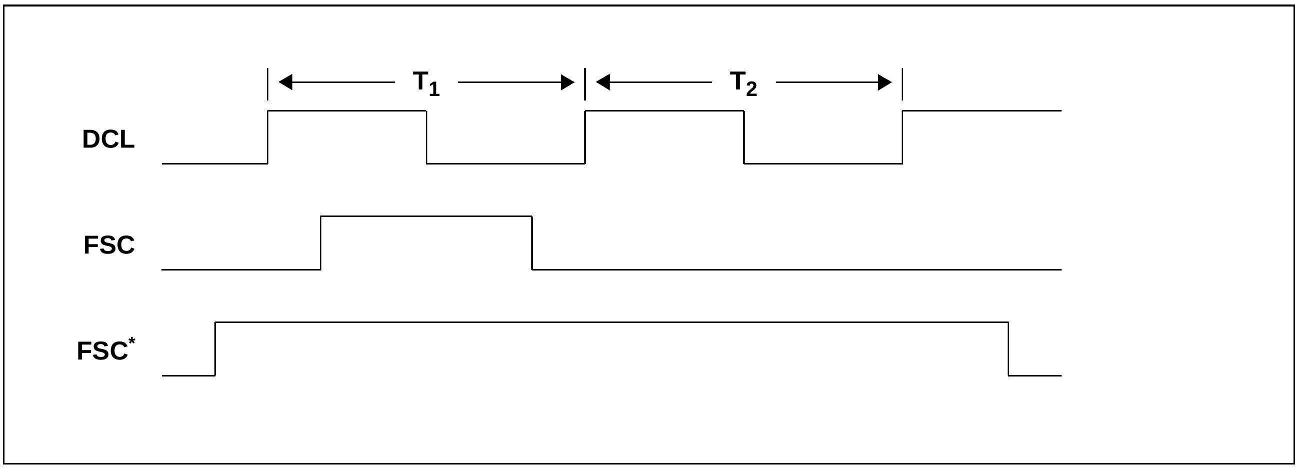


Figure 31 IOM®-2 Interface - Frame Start

The PSB 2168 supports both single clock mode and double clock mode. In single clock mode, the bit rate is equal to the clock rate. Bits are shifted out with the rising edge of DCL and sampled at the falling edge. In double clock mode, the clock runs at twice the bit rate. Therefore for each bit there are two clock cycles. Bits are shifted out with the rising edge of the first clock cycle and sampled with the falling edge of the second clock cycle. Figure **32** shows the timing for single clock mode and figure **33** shows the timing for double clock mode.

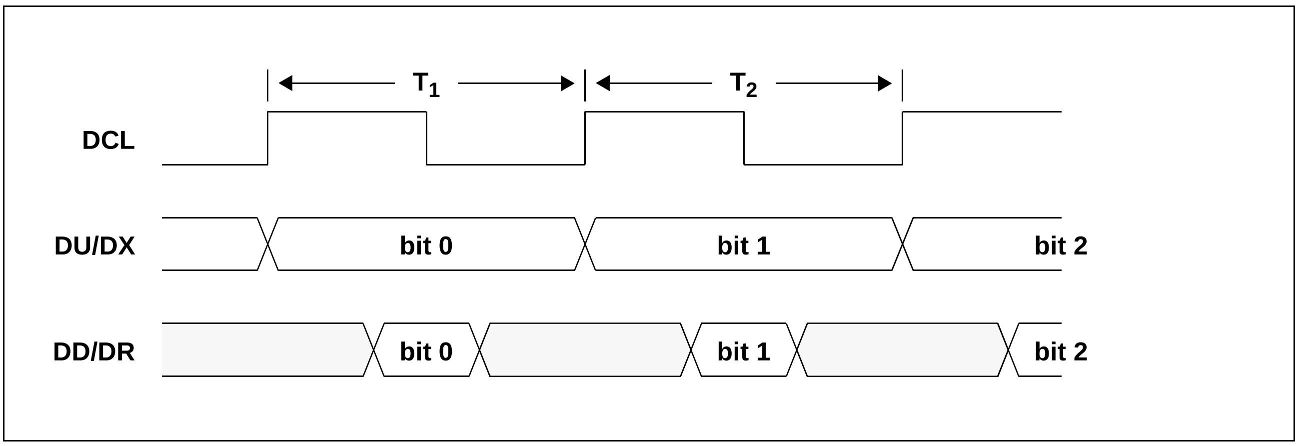


Figure 32 IOM®-2 Interface - Single Clock Mode

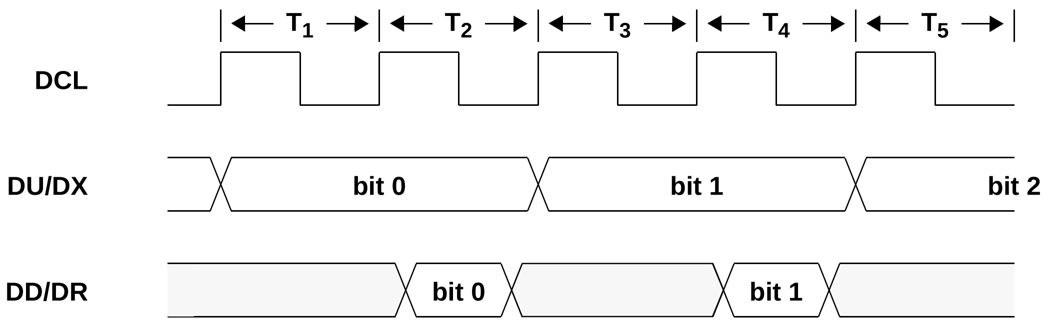


Figure 33 IOM®-2 Interface - Double Clock Mode

The PSB 2168 supports up to two channels simultaneously for data transfer. Both the coding (PCM or linear) and the data direction (DD/DU assignment for transmit/receive) can be programmed individually for each channel. Table **61** shows the registers used for configuration of the IOM®-2 interface.

Table 61 IOM®-2 Interface Registers

Register	# of Bits	Name	Comment
SDCONF	1	EN	Interface enable
SDCONF	1	DCL	Selection of clock mode
SDCONF	6	NTS	Number of timeslots within frame
SDCHN1	1	EN	Channel 1 enable
SDCHN1	6	TS	First timeslot (channel 1)
SDCHN1	1	DD	Data Direction (channel 1)
SDCHN1	1	PCM	8 bit code or 16 bit linear PCM (channel 1)
SDCHN1	1	PCD	8 bit code (A-law or μ-law, channel 1)
SDCHN2	1	EN	Channel 2 enable
SDCHN2	6	TS	First timeslot (channel 2)
SDCHN2	1	DD	Data Direction (channel 2)
SDCHN2	1	PCM	8 bit code or 16 bit linear PCM (channel 2)
SDCHN2	1	PCD	8 bit code (A-law or μ-law, channel 2)

In A-law or μ-law mode, only 8 bits are transferred and therefore only one timeslot is needed for a channel. In linear mode, 16 bits are needed for a single channel. In this mode, two consecutive timeslots are used for data transfer. Bits 8 to 15 are transferred within the first timeslot and bits 0 to 7 are transferred within the next timeslot. The first timeslot must have an even number. The most significant bit is always transmitted first.

2.4.2 SSDI Interface

The SSDI interface is intended for seamless connection to low-cost burst mode controllers (e.g. PMB 27251) and supports a single channel in each direction. The data stream is partitioned into frames. Within each frame one 16 bit value can be sent and received by the PSB 2168. The start of a frame is indicated by the rising edge of FSC. Data is always sampled at the falling edge of DCL and shifted out with the rising edge of DCL.

The SSDI transmitter and receiver are operating independently of each other except that both use the same FSC and DCL signal.

2.4.2.1 SSDI Interface - Transmitter

The PSB 2168 indicates outgoing data (on signal DX) by activating DXST for 16 clocks. The signal DXST is activated with the same rising edge of DCL that is used to send the first bit (Bit 15) of the data. DXST is deactivated with the first rising edge of DCL after the last bit has been transferred. The PSB 2168 drives the signal DX only when DXST is activated. Figure **34** shows the timing for the transmitter.

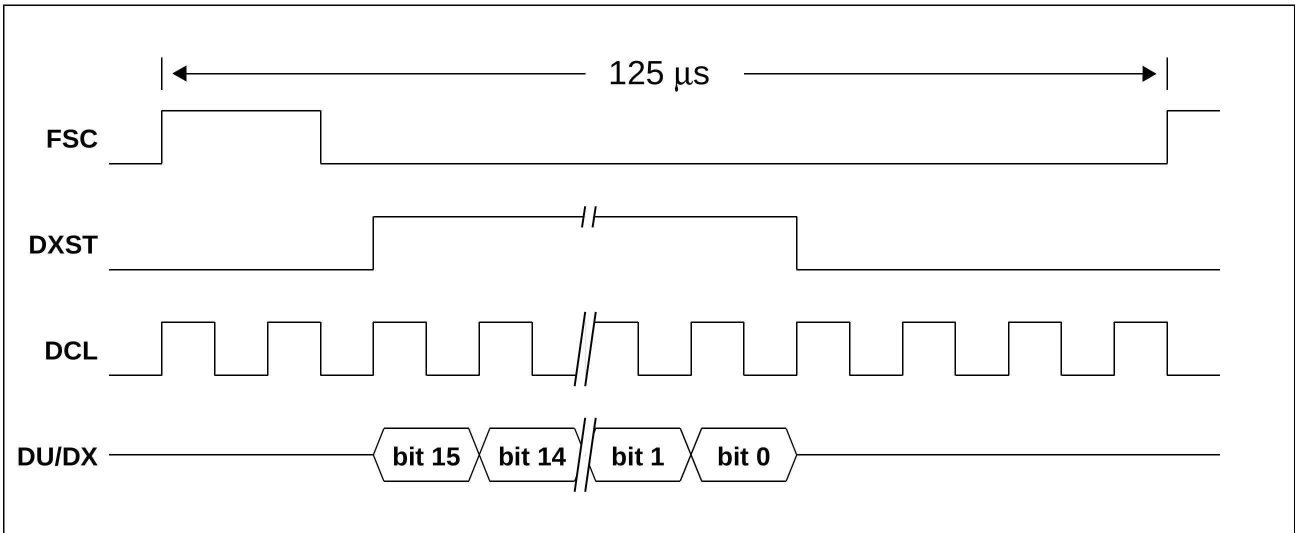


Figure 34 SSDI Interface - Transmitter Timing

2.4.2.2 SSDI Interface - Receiver

Valid data is indicated by an active DRST pulse. Each DRST pulse must last for exactly 16 DCL clocks. As there may be more than one DRST pulses within a single frame the PSB 2168 can be programmed to listen to the n-th pulse with n ranging from 1 to 16. In order to detect the first pulse properly, DRST must not be active at the rising edge of FSC. In figure **35** the PSB 2168 is listening to the third DRST pulse (n=3).

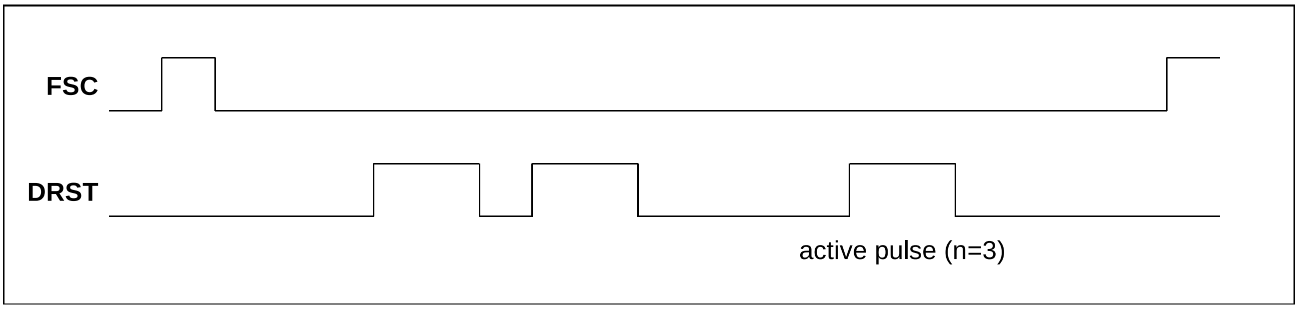


Figure 35 SSDI Interface - Active Pulse Selection

Figure **36** shows the timing for the SSDI receiver.

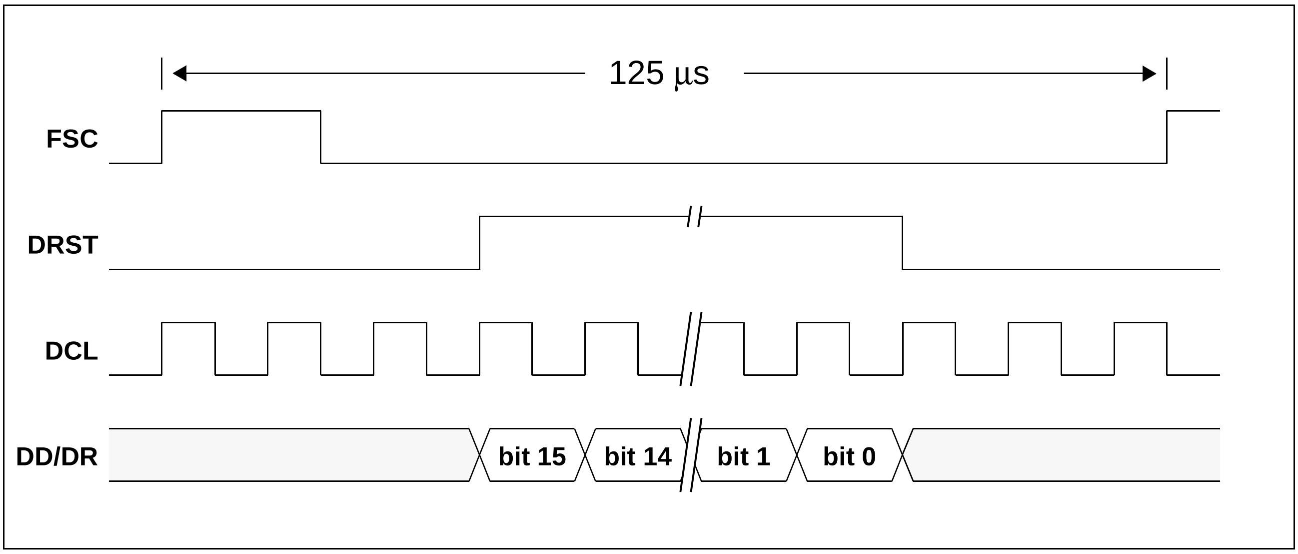


Figure 36 SSDI Interface - Receiver Timing

Table **62** shows the registers used for configuration of the SSDI interface.

Table 62 SSDI Interface Register

Register	# of Bits	Name	Comment
SDCHN1	4	NAS	Number of active DRST strobe

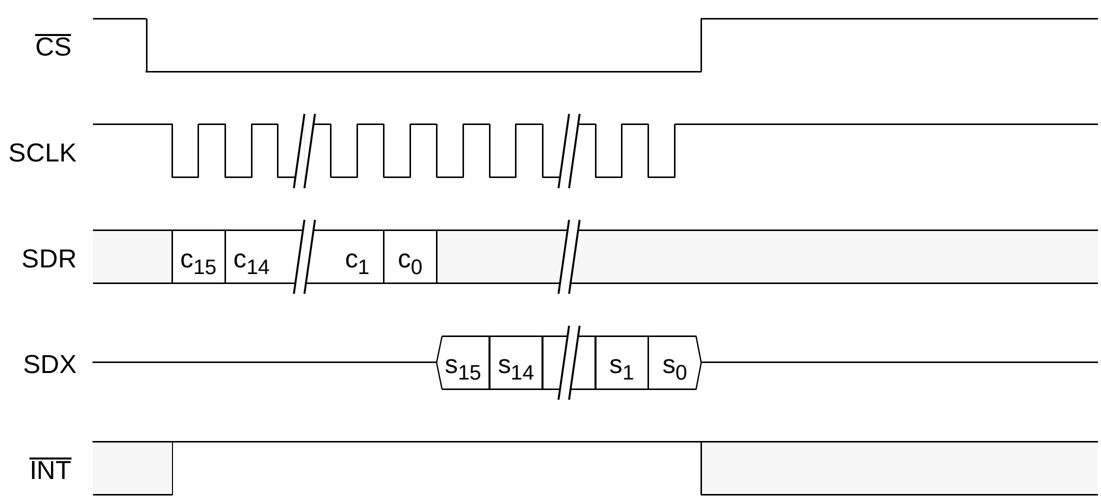
2.4.3 Serial Control Interface

The serial control interface (SCI) uses four lines: SDR, SDX, SCLK and $\overline{CS}$. Data is transferred by the lines SDR and SDX at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of an access. Data is sampled by the PSB 2168 at the rising edge of SCLK and shifted out at the falling edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. The accesses to the PSB 2168 can be divided into three classes:

1. Configuration Read/Write
2. Status/Data Read
3. Register Read/Write

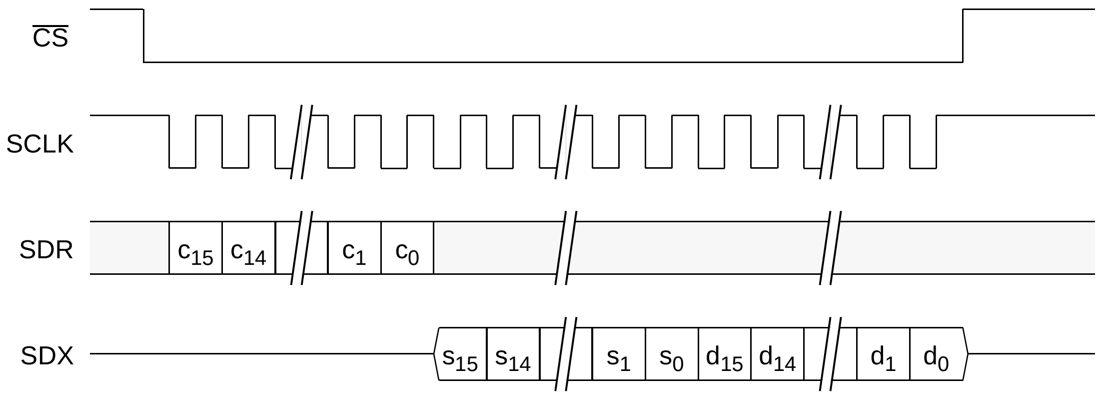
If the PSB 2168 is in power down mode, a read access to the status register does not deliver valid data with the exception of the RDY bit. After the status has been read the access can be either terminated or extended to read data from the PSB 2168. A register read/write access can only be performed when the PSB 2168 is ready. The RDY bit in the status register provides this information.

Any access to the PSB 2168 starts with the transfer of 16 bits to the PSB 2168 over line SDR. This first word specifies the access class, access type (read or write) and, if necessary, the register accessed. If a configuration register is written, the first word also includes the data and the access is terminated. Likewise, if a register read is issued, the access is terminated after the first word. All other accesses continue by the transfer of the status register from the PSB 2168 over line SDX. If a register (excluding configuration) is to be written, the next 16 bits containing the data are transferred over line SDR and the access is terminated. Figures **37** to **40** show the timing diagrams for the different access classes and types to the PSB 2168.



c_{15},..,c_0: command word for status register read
s_{15},..,s_0: status register

Figure 37 Status Register Read Access

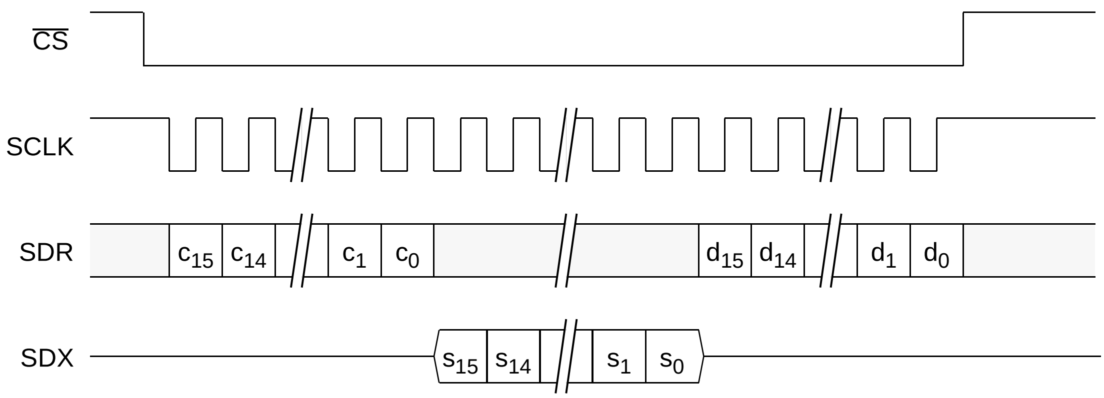


$c_{15},..,c_0$: command word for data read

$s_{15},..,s_0$: status register

$d_{15},..,d_0$: data to be read

Figure 38 Data Read Access



$c_{15},..,c_0$: command word for register write

$s_{15},..,s_0$: status register

$d_{15},..,d_0$: data to be written

Figure 39 Register Write Access

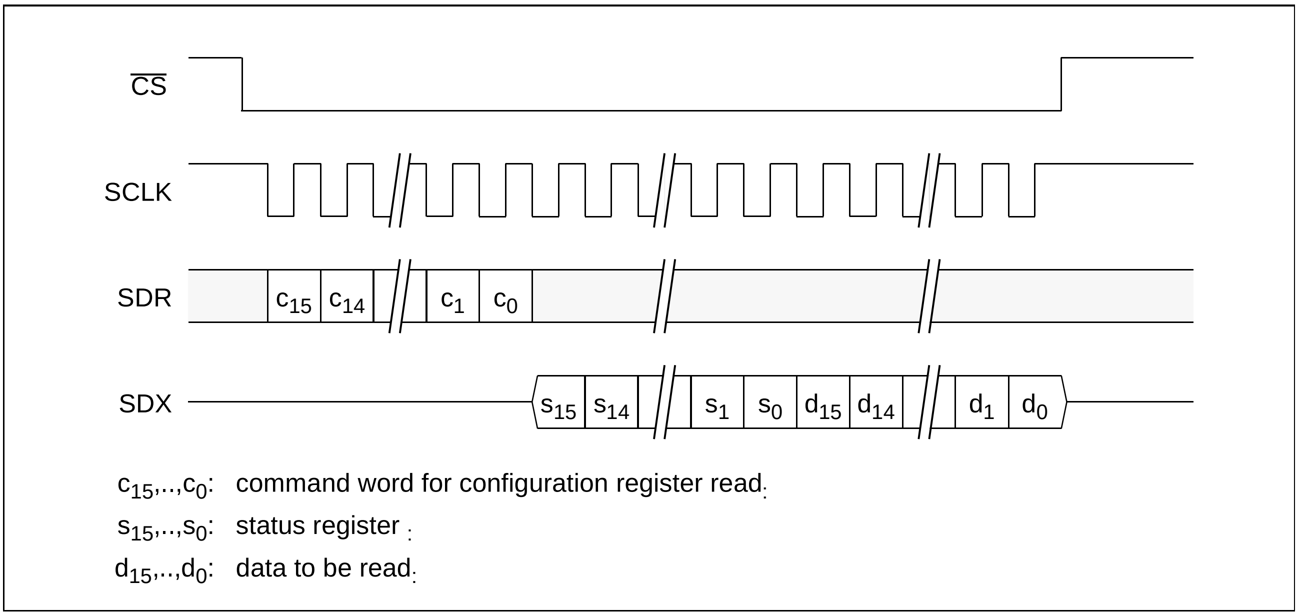


Figure 40 Configuration Register Read Access

Configuration registers at even adresses use bit positions d_7-d_0 while configuration registers at odd adresses use bit positions d_{15}-d_8.

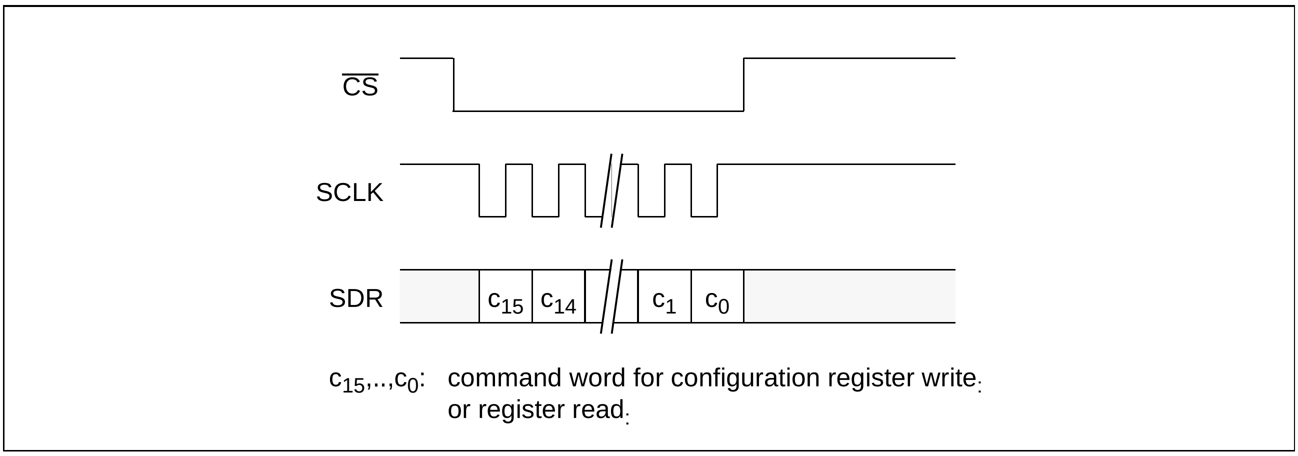


Figure 41 Configuration Register Write Access or Register Read Command

The internal interrupt signal is cleared when the first bit of the status register is put on SDX. However, externally the signal $\overline{\text{INT}}$ is deactivated as long as $\overline{\text{CS}}$ stays low. If the internal interrupt signal is not cleared or another event causing an interrupt occurs while the microcontroller is already reading the status belonging to the first event then INT goes low again immediately after $\overline{\text{CS}}$ is removed. The timing is shown in figure **37**. Table **63** shows the formats of the different command words. All other command words are reserved.

Table 63 Command Words for Register Access

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Status Register or Data Read Access	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Read Register	0	1	0	1	REG											
Write Register	0	1	0	0	REG											
Read Configuration Reg.	0	1	1	1	0	0	R	0	0	0	0	0	0	0	0	0
Write Configuration Reg.	0	1	1	0	0	0	W		DATA							

In case of a configuration register write, W determines which configuration register is to be written (table **64**):

Table 64 Address Field W for Configuration Register Write

9	8	Register
0	0	HWCONFIG 0
0	1	HWCONFIG 1
1	0	HWCONFIG 2
1	1	HWCONFIG 3

In case of a configuration register read, R determines which pair of configuration registers is to be read (table **65**):

Table 65 Address Field R for Configuration Register Read

9	Register pair
0	HWCONFIG 0 / HWCONFIG 1
1	HWCONFIG 2 / HWCONFIG 3

Note: Reading any register except the status register or a hardware configuration register requires at least two accesses. The first access is a register read command (figure ***41****). With this access the register address is transferred to the. After that access data read accesses (figure* ***38****) must be executed. The first data read access with STATUS:RDY=1 delivers the value of the register.*

2.4.4 Memory Interface

The PSB 2168 supports either Flash Memory or ARAM/DRAM as external memory for storing messages. If ARAM/DRAM is used, an EPROM can be added optionally to support read-only messages (e.g. voice prompts). Table **66** summarizes the different configurations supported.

Table 66 Supported Memory Configurations

Mbit	Type	Bank 0 (D_0-D_3)	Bank 1 (D_4-D_7)	Comment
1	ARAM/DRAM	256kx4	-	
2	ARAM/DRAM	256kx4	256kx4	
4	ARAM/DRAM	1Mx4	-	
4	ARAM/DRAM	512kx8		
8	ARAM/DRAM	1Mx4	1Mx4	
16	ARAM/DRAM	4Mx4	-	2k or 4k refresh
16	ARAM/DRAM	2Mx8		2k refresh
32	ARAM/DRAM	4Mx4	4Mx4	2k or 4k refresh
32	ARAM/DRAM	2x2Mx8		2k refresh
64	ARAM/DRAM	16Mx4	-	4k or 8k refresh
64	ARAM/DRAM	8Mx8		4k or 8k refresh
128	ARAM/DRAM	16Mx4	16Mx4	4k or 8k refresh
4-128	FLASH	512kx8 devices		KM29N040
16-128	FLASH	2Mx8 devices		KM29N16000

If ARAM/DRAM is used, the total amount of memory must be a power of two and all devices must be of the same type. The pin FRDY must be tied high.

For flash devices, the PSB 2168 supports in-circuit programming of voice prompts by releasing the control lines during reset and (optionally) power down. Instead of actively driving the lines $\overline{FCS}$, $\overline{FOE}$, $\overline{FWE}$, FCLE and ALE these lines are pulled high by a weak pullup during reset and (optionally) power down.

2.4.4.1 ARAM/DRAM Interface

The PSB 2168 supports up to two banks of memory which may be 4 bit or 8 bit wide (Figure **42**). If both banks are used they must be populated identically.

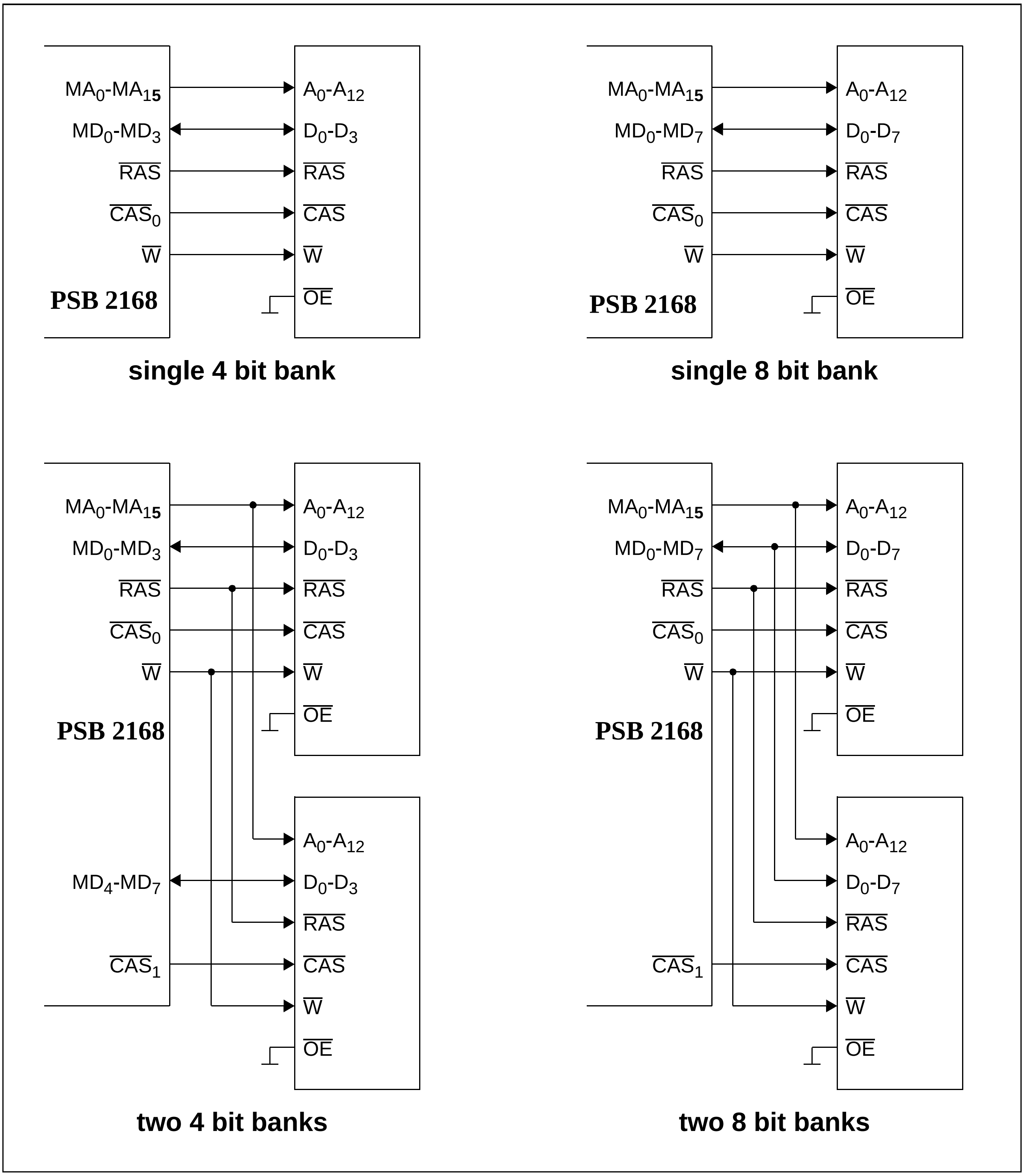


Figure 42 ARAM/DRAM Interface - Connection Diagram

The PSB 2168 also supports different internal organizations of ARAM/DRAM chips. Table **67** shows the necessary connections on the address bus.

Table 67 Address Line Usage (ARAM/DRAM Mode)

ARAM/DRAM	CS9[1)]	MA_0-MA_8	MA_9	MA_{10}	MA_{11}	MA_{12}	MA_{13}
256k x4	1	A_0-A_8					
512k x8	1	A_0-A_8	A_9				
1M x4	0	A_0-A_8	A_9				
4M x4 (2k refresh)	0	A_0-A_8	A_9	A_{10}			
4M x4 (4k refresh)	0	A_0-A_8	A_9	A_{10}	A_{11}		
2M x8	0	A_0-A_8	A_9	A_{10}			
16M x4 (4k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	
16M x4 (8k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	A_{12}
8M x8 (4k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	
8M x8 (8k refresh)	0	A_0-A_8	A_9	A_{10}		A_{11}	A_{12}

1) see chip control register CCTL

The timing of the ARAM/DRAM interface is shown in figures **43** to **45**. The timing is derived form the internal memory clock MCLK* which runs at a quarter of the system clock.

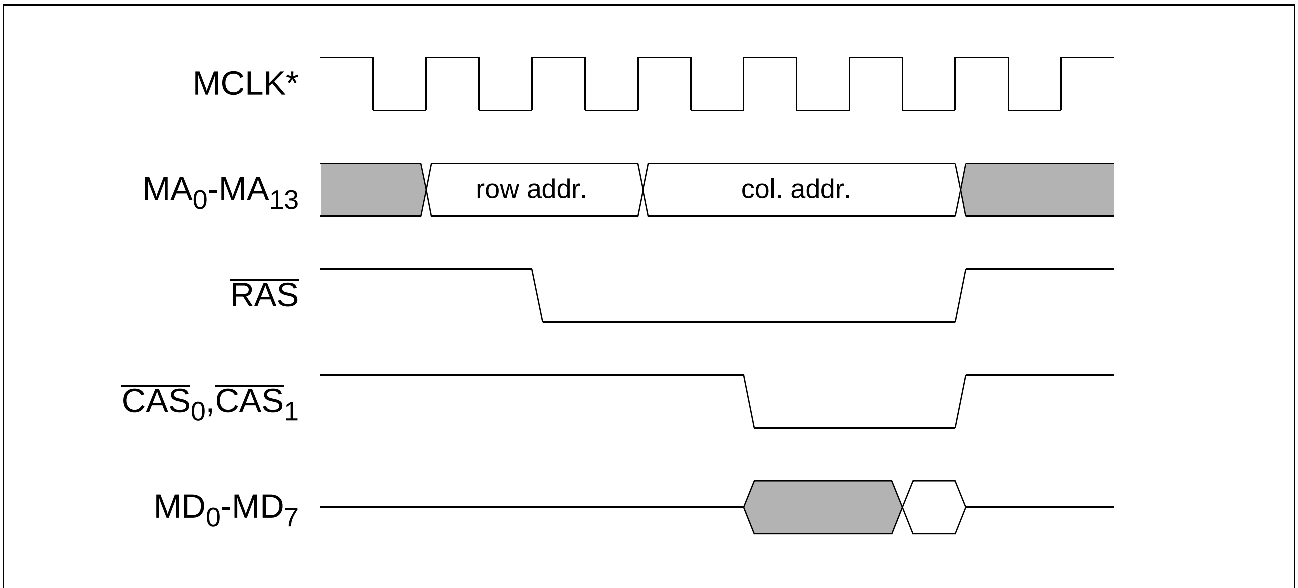


Figure 43 ARAM/DRAM Interface - Read Cycle Timing

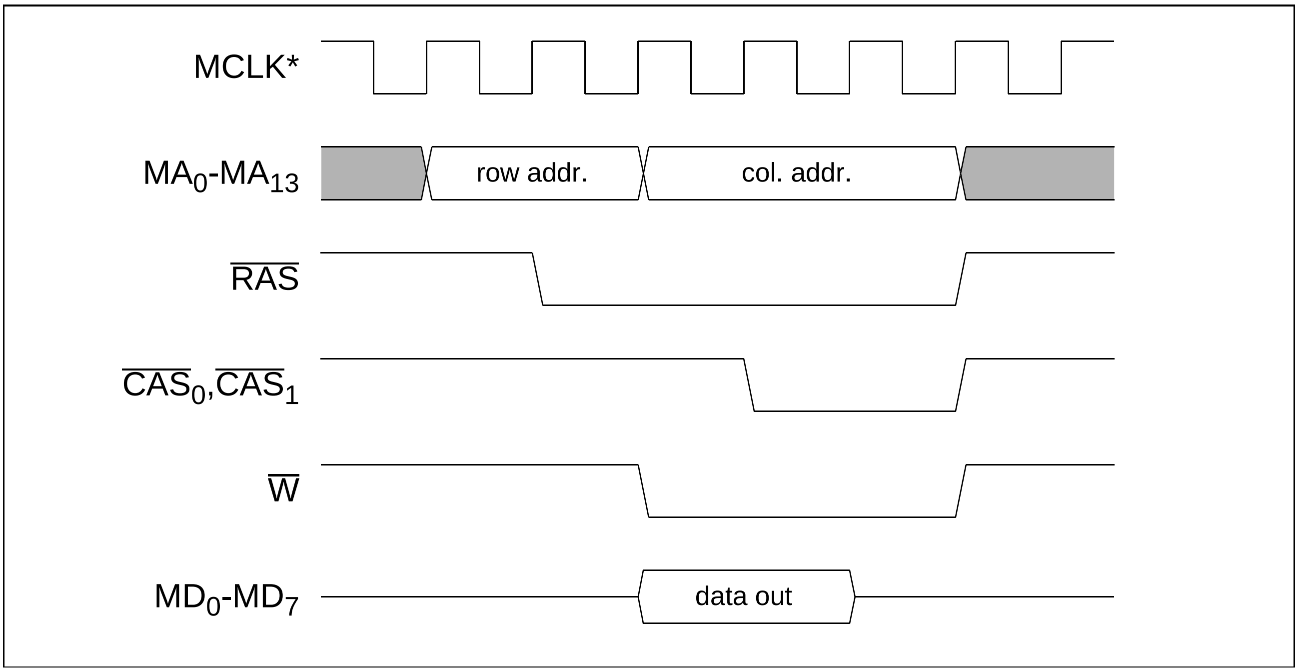


Figure 44 ARAM/DRAM Interface - Write Cycle Timing

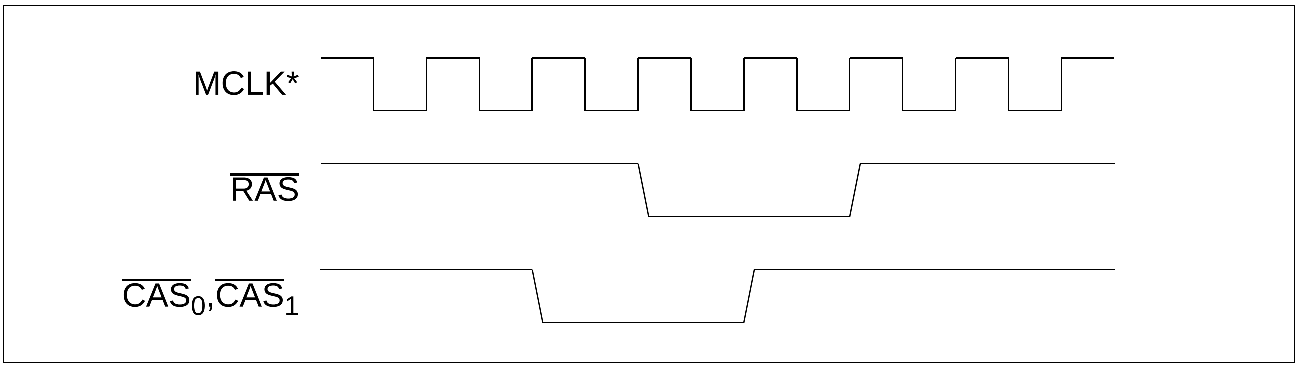


Figure 45 ARAM/DRAM Interface - Refresh Cycle Timing

The PSB 2168 ensures that $\overline{RAS}$ remains inactive for at least one MCLK*-cycle between successive accesses.

The frequency at which refresh cycles are performed is shown in table **68**.

Table 68 Refresh Frequency Selection

Refresh frequency	Comment
64 kHz	Memory access (e.g. recording) in progress
8, 16, 32 or 64 kHz[1)]	No memory access in progress or power-down

1) as programmed by HWCONFIG2:RSEL

2.4.4.2 EPROM Interface

The PSB 2168 supports an EPROM in parallel with ARAM/DRAM. This interface is always 8 Bits wide and supports a maximum of 256 kB. Figure **46** shows a connection diagram and figure **47** the timing. This interface supports read cycles only.

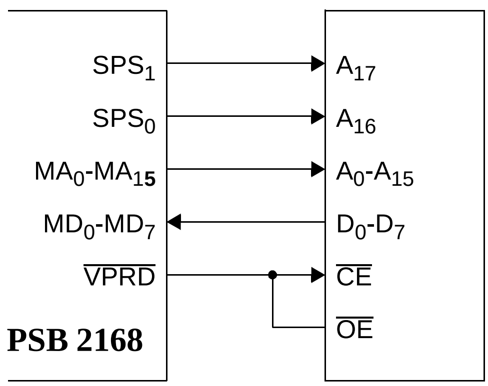


Figure 46 EPROM Interface - Connection Diagram

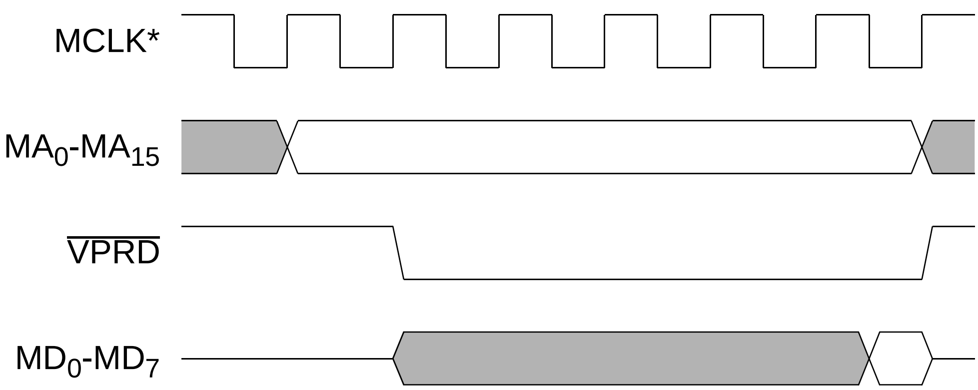


Figure 47 EPROM Interface - Read Cycle Timing

Note: *In order to access more than 64 kB the pins SPS_0 and SPS_1 can be programmed to provide the address lines A_{16} and A_{17}. In this mode A_{16} and A_{17} remain stable during the whole read cycle. See the register SPSCTL for programming information.*

2.4.4.3 Flash Memory Interface

The PSB 2168 has special support for the KM29N040 and KM29N16000 or equivalent devices. No external components are required for up to four KM29N040. Figure **48** shows the connection diagram for a single device.

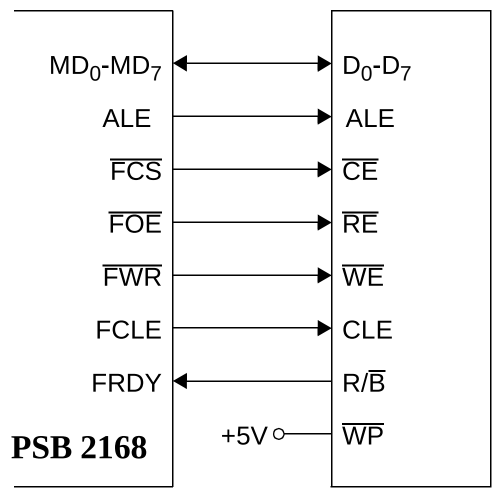


Figure 48 Flash Memory Interface - Connection Diagram

Table **69** shows the signals output during a device access on the MA-lines. The address bits can used by an external decoder. Up to four KM29N040 are supported directly by the decoded select signals $\overline{FCS}_0$-$\overline{FCS}_3$.

Table 69 Address Line Usage (Samsung Mode)

MA_{11}	MA_{10}	MA_9	MA_8	MA_7	MA_6	MA_5	MA_4	MA_3	MA_2	MA_1	MA_0
$\overline{FCS}_3$	$\overline{FCS}_2$	$\overline{FCS}_1$	$\overline{FCS}_0$	A_{23}	A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}

Figure **49** shows an application with three KM29N040 devices.

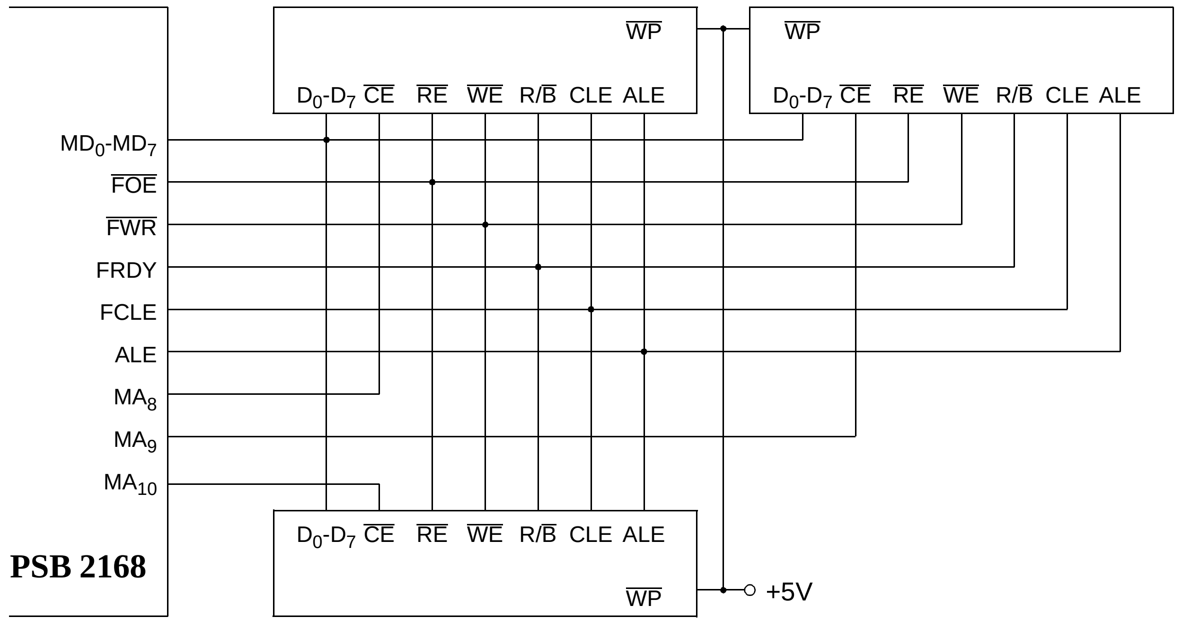


Figure 49 Flash Memory Interface - Multiple Devices

An access to the Flash Memory can consist of several partial access cycles where only the timing of the partial access cycles is defined but not the time between two adjacent partial access cycles. The PSB 2168 performs three types of partial access cycles:

1. Command write
2. Address write
3. Data read/write

Table **70** shows the supported accesses and the corresponding partial access cycles.

Table 70 Flash Memory Command Summary

Access	Command write	Address write 1	Address write 2	Address write 3	# of Data read/write	Command write
RESET	FF	-	-	-	-	-
STATUS READ	70	-	-	-	1	-
BLOCK ERASE	60	A_8-A_{15}	A_{16}-A_{23}	-	-	D0
READ	00	A_0-A_7	A_8-A_{15}	A_{16}-A_{23}	1-32	-
WRITE	80	A_0-A7	A_8-A_{15}	A_{16}-A_{23}	1-32	10

The timing for the partial access cycles is shown in figures **50** to **51**. Note that both $\overline{FCS}$ and MA_0-MA_{15} remain stable between the first and the last partial access of a device access.

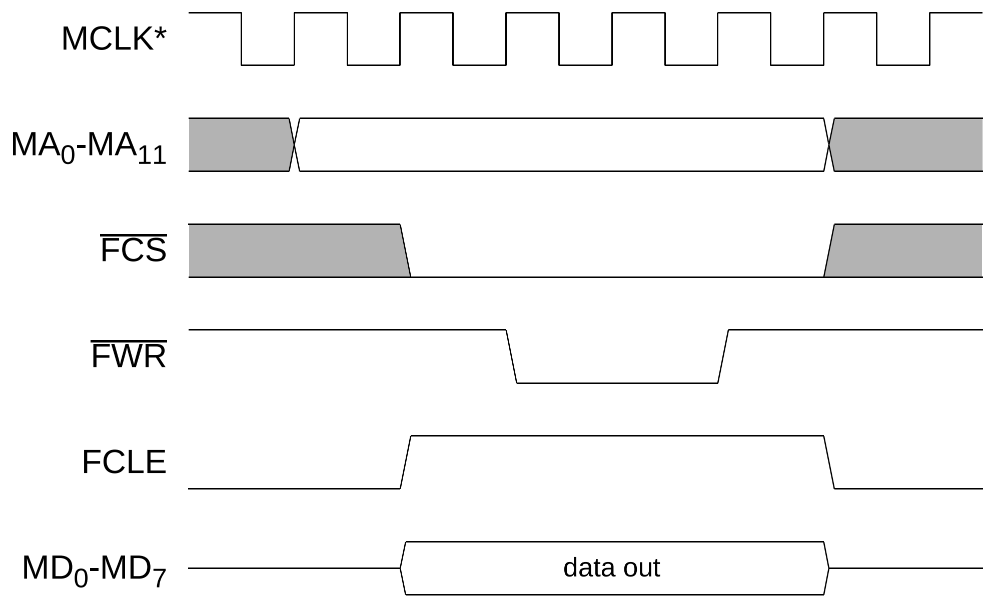


Figure 50 Flash Memory Interface - Command Write

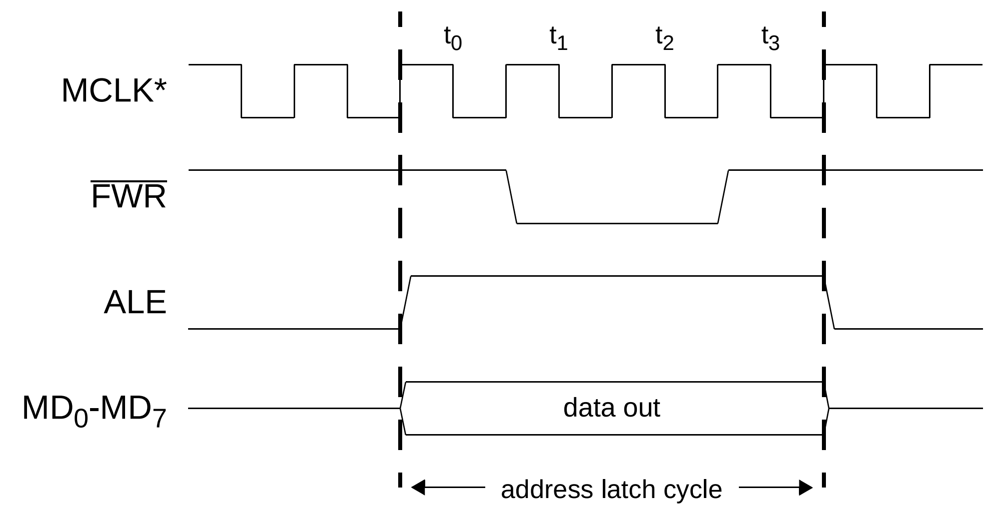


Figure 51 Flash Memory Interface - Address Write

As there is no access that starts or stops with an address write cycle (figure **51**) $\overline{FCS}$ is already low at the start of this cycle and also remains low.

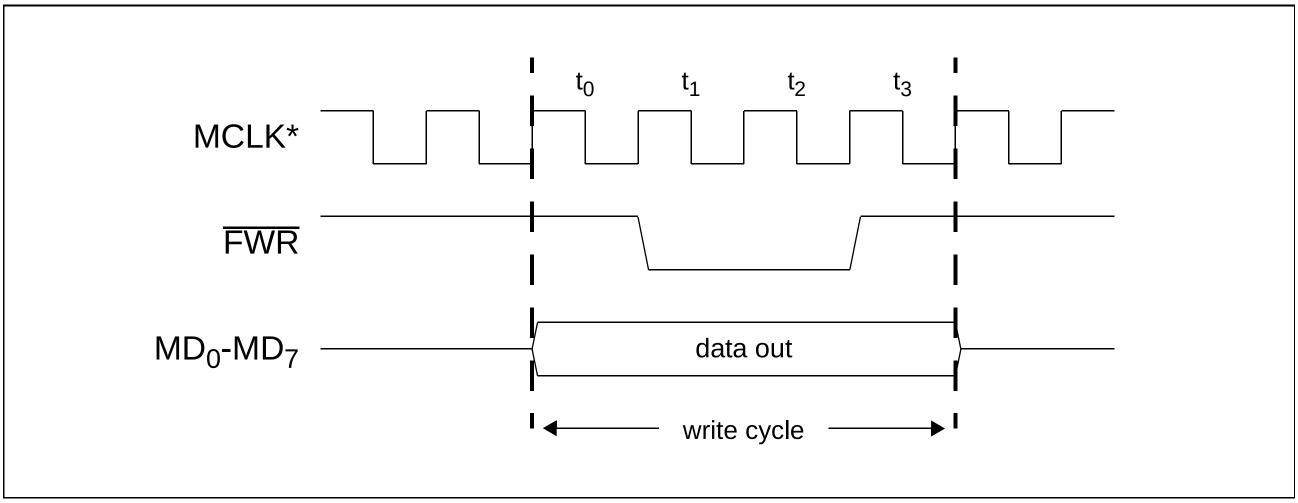


Figure 52 Flash Memory Interface - Data Write

As there is no access that starts or stops with a data write cycle (figure **52**) $\overline{FCS}$ is already low at the start of this cycle and also remains low.

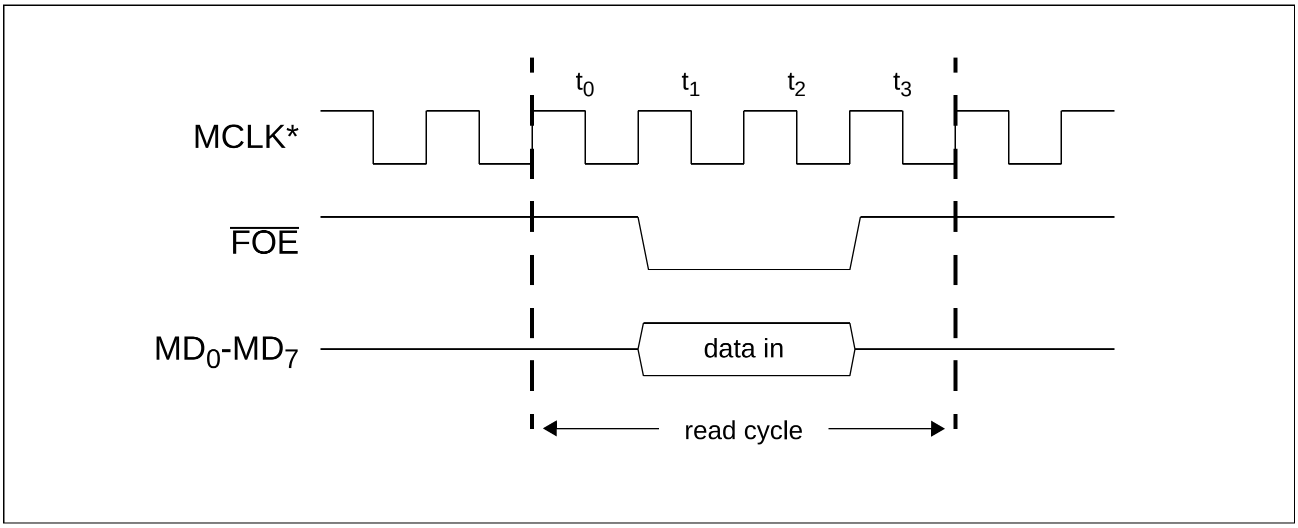


Figure 53 Flash Memory Interface - Data Read

If the device access ends with a read cycle, the $\overline{FCS}$-signals go inactive after t_3 of the last read cycle. The data is latched at the rising edge of $\overline{FOE}$.

2.4.5 Auxiliary Parallel Port

The PSB 2168 provides an auxiliary parallel port if the memory interface is in Samsung mode and only one device is used. In this case the lines MA_0 to MA_{15} are not needed for the memory interface and can therefore be used for an auxiliary parallel port. This port has two modes: static mode and multiplex mode.

2.4.5.1 Static Mode

In static mode all pins of the auxiliary parallel port interface have identical functionality. Any pin can be configured as an output or an input. Pins configured as outputs provide a static signal as programmed by the controller. Pins configured as inputs are monitoring the signal continuously without latching. The controller always reads the current value. Table **71** shows the registers used for static mode.

Table 71 Static Mode Registers

Register	# of bits	Comment
DOUT3	16	Output signals (for pins configured as outputs)
DIN	16	Input signals (for pins configured as inputs)
DDIR	16	Pin direction

2.4.5.2 Multiplex Mode

In multiplex mode, the PSB 2168 uses MA_{12}-MA_{15} to distinguish four timeslots. Each timeslot has a duration of approximately 2 ms. The timeslots are separated by a gap of approximately 125 µs in which none of the signals at MA_{12}-MA_{15} are active. The PSB 2168 multiplexes three more output registers to MA_0-MA_{11} in timeslots 0, 1 and 2. In timeslot 3 the direction of the pins can be programmed. For input pins, the signal is latched at the falling edge of MA_{15}. Table **72** shows the registers used for multiplex mode.

This mode is useful for scanning keys or controlling seven segment LED displays.

Table 72 Multiplex Mode Registers

Register	# of bits	Comment
DOUT0	12	Output signals on MA_0-MA_{11} while MA_{15}=1
DOUT1	12	Output signals on MA_0-MA_{11} while MA_{14}=1
DOUT2	12	Output signals on MA_0-MA_{11} while MA_{13}=1
DOUT3	12	Output signals (for pins configured as outputs) while MA_{12}=1
DIN	12	Input signals (for pins configured as inputs) at falling edge of MA_{12}
DDIR	12	Pin direction during MA_{12}=1

Figure **54** shows the timing diagram for multiplex mode.

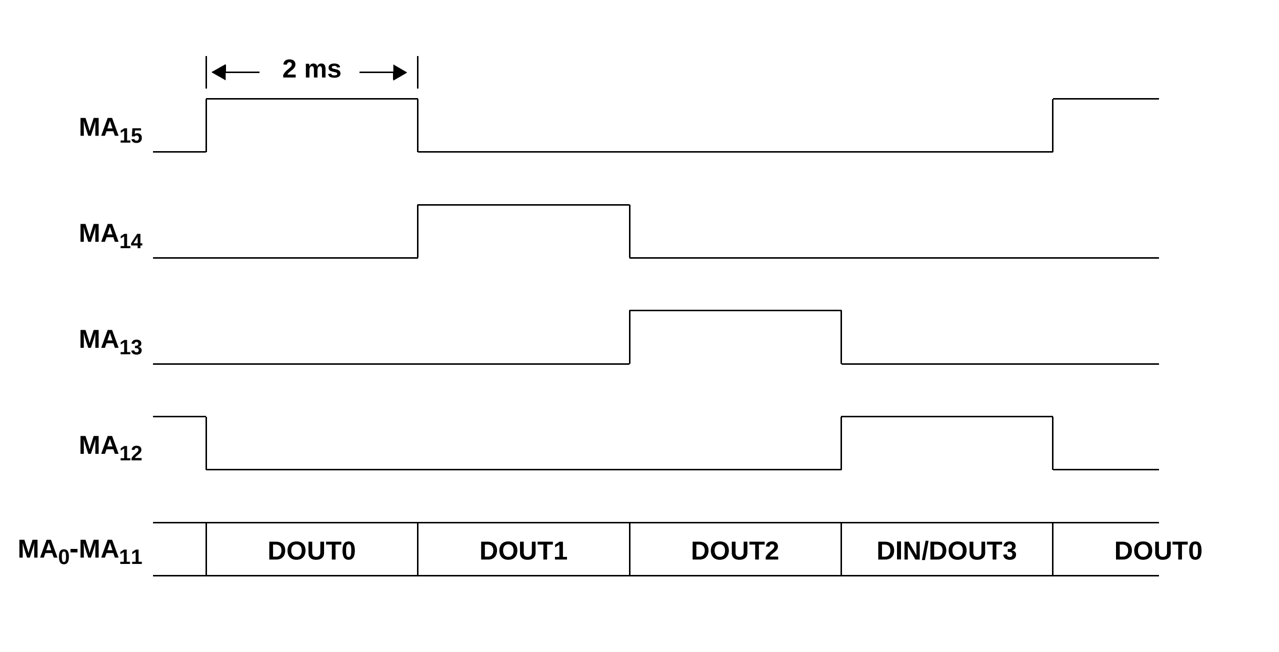


Figure 54 Auxiliary Parallel Port - Multiplex Mode

Note: In either mode the voltage at any pin (MA_0 to MA_{15}) must not exceed V_{DD}.

3 Detailed Register Description

The PSB 2168 has a single status register (read only) and an array of data registers (read/write). The purpose of the status register is to inform the external microcontroller of important status changes of the PSB 2168 and to provide a handshake mechanism for data register reading or writing. If the PSB 2168 generates an interrupt, the status register contains the reason of the interrupt.

3.1 Status Register

15															0
RDY	ABT	0	0	CIA	CD	CPT	CNG	SD	ERR	BSY	DTV	ATV	-[1)]	-[1)]	-[1)]

1) undefined

RDY Ready

0: The last command (if any) is still in progress.

1: The last command has been executed.

ABT Abort

0: No exception during operation

1: Some exception other than reset caused the PSB 2168 to abort any operation currently in progress. The external microcontroller should reinitialize the PSB 2168 to ensure proper operation. The ABT bit is cleared by writing any value to register REV. No other command is accepted by the PSB 2168 while ABT is set.

CIA Caller ID Available

0: No new data for caller ID

1: New caller ID byte available

CD Carrier Detect

0: No carrier detected

1: Carrier detected

CPT **Call Progress Tone**

0: Currently no call progress tone detected or pause detected (raw mode)

1: Currently a call progress is detected

CNG **Fax Calling Tone**

0: Currently no fax calling tone detected

1: Currently a fax calling tone is detected

SD **Speech Detected**

0: No speech detected

1: Speech signal at input of coder

ERR **Error (File Command)**

0: No error

1: Last file command resulted in an error

BSY **Busy (File Command)**

0: File system idle

1: File system still busy (also set during encoding/decoding)

DTV **DTMF Tone Valid**

0: No new DTMF code available

1: New DTMF code available in DDCTL

ATV **Alert Tone Valid**

0: No new alert tone code available

1: New alert tone code available in ADCTL0

3.2 Hardware Configuration Registers

HWCONFIG 0 - Hardware Configuration Register 0

7							0
PD	0	RTC	OSC	PPSDI	$\overline{\text{PFRDY}}$	PPINT	PPSDX

PPSDX Push/Pull for SDX

0: The SDX pin has open-drain characteristic

1: The SDX pin has push/pull characteristic

PPINT Push/Pull for $\overline{\text{INT}}$

0: The $\overline{\text{INT}}$ pin has open-drain characteristic

1: The $\overline{\text{INT}}$ pin has push/pull characteristic

$\overline{\text{PFRDY}}$ Pullup for FRDY

0: The internal pullup resistor of pin $\overline{\text{FRDY}}$ is enabled

1: The internal pullup resistor of $\overline{\text{FRDY}}$ is disabled

PPSDI Push/Pull for SDI interface

0: The DU and DD pins have open-drain characteristic

1: The DU and DD pins have push/pull characteristic

OSC Enable Auxiliary Oscillator

0: The auxiliary oscillator (OSC_1, OSC_2) is disabled

1: The auxiliary oscillator (OSC_1, OSC_2) is enabled

RTC Enable Real Time Clock

0: The real time clock is disabled

1: The real time clock (RTC) is enabled.

PD Power Down (read only)

0: The PSB 2168 is in active mode

1: The PSB 2168 is in power down mode

HWCONFIG 1 - Hardware Configuration Register 1

7					0
APP	0	0	1	XTAL	SSDI

APP Auxiliary Parallel Port

7	6	Description
0	0	normal (ARAM/DRAM, Intel type flash, voice prompt EPROM)
0	1	APP static mode
1	0	APP multiplex mode
1	1	reserved

XTAL XTAL Frequency

2	1	Factor p[1)]	Description
0	0	reserved	reserved
0	1	4.5	31.104 MHz
1	0	4	27.648 MHz
1	1	reserved	reserved

1) The factor p is needed to calculate the clock frequency at AFECLK.

SSDI SSDI Interface Selection

0: IOM®-2 Interface

1: SSDI Interface

HWCONFIG 2 - Hardware Configuration Register 2

7					0
PPM	ESDX	ESDR	0	0	RSEL

PPM **Push/Pull for Memory Interface (reset, power down)**

0: The signals for the memory interface have push/pull characteristic

1: The signals for the memory interface have pullup/pulldown characteristic

ESDX **Edge Select for DX**

0: DX is transmitted with the rising edge of DCL

1: DX is transmitted with the falling edge of DCL

ESDR **Edge Select for DR**

0: DR is latched with the falling edge of DCL

1: DR is latched with the rising edge of DCL

RSEL **Refresh Select**

1	0	Description
0	0	64 kHz refresh frequency
0	1	32 kHz refresh frequency
1	0	16 kHz refresh frequency
1	1	8 kHz refresh frequency

HWCONFIG 3 - Hardware Configuration Register 3

7							0
0	0	0	0	0	0	CM1	CM0

CM1 Clock Master 1

0: Clock generation at AFEFS and AFECLK disabled

1: Clock generation at AFEFS and AFECLK enabled

CM0 Clock Master 0

0: 512 kHz (AFECLK)

1: 1.536 MHz (AFECLK)

3.3 Read/Write Registers

The following sections contains all read/write registers of the PSB 2168. The register addresses are given as hexadecimal values. Registers marked with an R are affected by reset or a wake up after power down. All other registers retain their previous value. No access must be made to addresses other than those associated with a read/write register.

Furthermore parameters of a functional unit must not be altered while the unit is enabled. Parameters that can be changed on the fly (taking effect while the functional unit is enabled) are marked individually.

3.3.1 Register Table

Address.	Name	Long Name	Page
00h	REV	Revision	96
01h R	CCTL	Chip Control	97
02h R	INTM	Interrupt Mask Register	98
0Ah R	SDCONF	Serial Data Interface Configuration	99
0Bh R	SDCHN1	Serial Data Interface Channel 1	100
0Ch R	IFS3	Interface Select 3	102
0Dh R	SDCHN2	Serial Data Interface Channel 2	103
0Eh R	IFS4	Interface Select 4	104
0Fh R	IFG5	Interface Gain 5	105
10h R	UA	Universal Attenuator	106
11h R	DGCTL	DTMF Generator Control	107
12h	DGF1	DTMF Generator Frequency 1	108
13h	DGF2	DTMF Generator Frequency 2	109
14h	DGL	DTMF Generator Level	110
15h	DGATT	DTMF Generator Attenuation	111
16h R	CNGCTL	Calling Tone Control	112
17h	CNGBT	CNG Burst Time	113
18h	CNGLEV	CNG Minimal Signal Level	114
19h	CNGRES	CNG Signal Resolution	115
1Ah R	ATDCTL0	Alert Tone Detection 0	116
1Bh	ATDCTL1	Alert Tone Detection 1	117
1Ch R	CIDCTL0	Caller ID Control 0	118
1Dh	CIDCTL1	Caller ID Control 1	119
20h R	CPTCTL	Call Progress Tone Control	120
21h	CPTTR	Call Progress Tone Thresholds	121
22h	CPTMN	CPT Minimum Times	122
23h	CPTMX	CPT Maximum Times	123
24h	CPTDT	CPT Delta Times	124
25h R	LECCTL	Line Echo Cancellation Control	125

26h	LECLEV	Minimal Signal Level for Line Echo Cancellation	126
27h	LECATT	Externally Provided Attenuation	127
28h	LECMGN	Margin for Double Talk Detection	128
29h R	DDCTL	DTMF Detector Control	129
2Ah	DDTW	DTMF Detector Signal Twist	130
2Bh	DDLEV	DTMF Detector Minimum Signal Level	131
2Eh R	FCFCTL	Equalizer Control	132
2Fh	FCFCOF	Equalizer Coefficient Data	134
30h R	SCCTL	Speech Coder Control	135
31h	SCCT2	Speech Coder Control 2	136
32h	SCCT3	Speech Coder Control 3	137
34h R	SDCTL	Speech Decoder Control	138
38h R	AGCCTL	AGC Control	139
39h R	AGCATT	Automatic Gain Control Attenuation	140
3Ah	AGC1	Automatic Gain Control 1	141
3Bh	AGC2	Automatic Gain Control 2	142
3Ch	AGC3	Automatic Gain Control 3	143
3Dh	AGC4	Automatic Gain Control 4	144
3Eh	AGC5	Automatic Gain Control 5	145
40h R	FCTL	File Control	146
41h R	FCMD	File Command	147
42h R	FDATA	File Data	149
43h R	FPTR	File Pointer	150
47h R	SPSCTL	SPS Control	151
48h R	RTC1	Real Time Clock 1	152
49h R	RTC2	Real Time Clock 2	153
4Ah R	DOUT0	Data Out (Timeslot 0)	154
4Bh R	DOUT1	Data Out (Timeslot 1)	155
4Ch R	DOUT2	Data Out (Timeslot 2)	156
4Dh R	DOUT3	Data Out (Timeslot 3 or Static Mode)	157
4Eh	DIN	Data In (Timeslot 3 or Static Mode)	158
4Fh R	DDIR	Data Direction (Timeslot 3 or Static Mode)	159

Note: Registers CCTL, FCTL, FCMD, FDATA, FPTR, RTC1, RTC2, DOUT0, DOUT1, DOUT2, DOUT3 and DDIR are only affected by reset, not by wakeup. For register SPSCTL see the register description for the exact behaviour.

3.3.2 Register Naming Conventions

Several registers contain one or more fields for input signal selection. All fields labelled I_1 (I_2, I_3) are five bits wide and use the same coding as shown in table 73.

Table 73 Signal Encoding

4	3	2	1	0	Signal	Description
0	0	0	0	0	S_0	Silence
0	0	0	0	1	S_1	Reserved
0	0	0	1	0	S_2	Reserved
0	0	0	1	1	S_3	Reserved
0	0	1	0	0	S_4	Reserved
0	0	1	0	1	S_5	Serial interface input, channel 1
0	0	1	1	0	S_6	Serial interface output, channel 1
0	0	1	1	1	S_7	Serial interface input, channel 2
0	1	0	0	0	S_8	Serial interface output, channel 2
0	1	0	0	1	S_9	DTMF generator output
0	1	0	1	0	S_{10}	DTMF generator auxiliary output
0	1	0	1	1	S_{11}	Reserved
0	1	1	0	0	S_{12}	Reserved
0	1	1	0	1	S_{13}	Speech decoder output
0	1	1	1	0	S_{14}	Universal attenuator output
0	1	1	1	1	S_{15}	Line echo canceller output
1	0	0	0	0	S_{16}	AGC unit output (after AGC)
1	0	0	0	1	S_{17}	AGC unit output (before AGC)
1	0	0	1	0	S_{18}	Equalizer output
1	0	0	1	1		reserved
1	0	1	-	-		reserved
1	1	-	-	-		reserved

00_h REV Revision

15															0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

The revision register can only be read. For the PSB 2168, V2.1, all bits except bit 13 are zero.

Note: A write access to the revision register does not alter its content. It does, however, reset the ABT bit of the STATUS register.

01_h CCTL Chip Control

15															0
0	0	0	0	MV	0	0	PD	0	0	0	MQ	MT		CS9	SAS

Reset Value

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MV **Voice Prompt Directory**

0: not available

1: available (within EPROM or Flash)

PD **Power Down**

0: PSB 2168 is in active mode

1: enter power-down mode

MQ **Memory Quality**

0: ARAM

1: DRAM

MT **Memory Type**

3	2	Description
0	0	ARAM/DRAM
1	1	Samsung flash memory

CS9 **CAS selection**

0: other memory

1: 256kx4 or 512kx8 memory

SAS **Split Address Space**

0: other ARAM/DRAM

1: two 2Mx8 devices

02_h INTM Interrupt Mask Register

15															0
RDY	1	0	0	CIA	CD	CPT	CNG	SD	0	BSY	DTV	ATV	0	0	0

Reset Value

0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

If a bit of this register is reset (set to 0), the corresponding bit of the status register does not generate an interrupt.

If a bit is set (set to 1), an external interrupt can be generated by the corresponding bit of the status register.

l

$0A_h$ SDCONF Serial Data Interface Configuration

15										0
0	0	NTS	0	0	0	0	0	DCL	0	EN

Reset Value

0	0	0	0	0	0	0	0	0	0	0

NTS Number of Timeslots

13	12	11	10	9	8	Description
0	0	0	0	0	0	1
0	0	0	0	0	1	2
...	...	...	...	...	...	...
1	1	1	1	1	1	64

DCL Double Clock Mode

0: Single Clock Mode

1: Double Clock Mode

EN Enable Interface

0: Interface is disabled (both channels)

1: Interface is enabled (depending on separate channel enable bits)

$0B_h$ SDCHN1 Serial Data Interface Channel 1

15							0
NAS	0	0	PCD	EN	PCM	DD	TS

Reset Value

0	0	0	0	0	0	0	0

NAS Number of active DRST strobe (SSDI interface mode)

15	14	13	12	Description
0	0	0	0	1
...	...	...	...	...
1	1	1	1	16

PCD PCM Code

0: A-law

1: µ-law

EN Enable Interface

0: Interface is disabled

1: Interface is enabled if SDCONF:EN=1

PCM PCM Mode

0: 16 Bit Linear Coding (two timeslots)

1: 8 Bit PCM Coding (one timeslot)

DD Data Direction

0: DD: Data Downstream, DU: Data Upstream

1: DD: Data Upstream, DU: Data Downstream

TS Timeslot for Channel 1

5	4	3	2	1	0	Description
0	0	0	0	0	0	0
...	...	...	...	...	...	...
1	1	1	1	1	1	63

Note: If PCM=0 then TS denotes the first timeslot of the two consecutive timeslots used. Only even timeslots are allowed in this case.

$0C_h$ IFS3 Interface Select 3

15			0
HP	I1	I2	I3

Reset Value

0	0	0	0

HP **High-Pass for S_5**

0: Disabled

1: Enabled

I1 **Input signal 1 for S_6**

I2 **Input signal 2 for S_6**

I3 **Input signal 3 for S_6**

Note: As all sources are always active, unused sources must be set to 0 (S_0).

$0D_h$ SDCHN2 Serial Data Interface Channel 2

15										0
0	0	0	0	0	0	PCD	EN	PCM	DD	TS

Reset Value

0	0	0	0	0	0	0	0	0	0	0

PCD **PCM Code**

0: A-law

1: µ-law

EN **Enable Interface**

0: Interface is disabled

1: Interface is enabled if SDCONF:EN=1

PCM **PCM Mode**

0: 16 Bit Linear Coding (two timeslots)

1: 8 Bit PCM Coding (one timeslot)

DD **Data Direction**

0: DD: Data Downstream, DU: Data Upstream

1: DD: Data Upstream, DD: Data Downstream

TS **Timeslot for Channel 2**

5	4	3	2	1	0	Description
0	0	0	0	0	0	0
0	0	0	0	0	1	1
...	...	...	...	...	...	...
1	1	1	1	1	1	63

Note: If PCM=0 then TS denotes the first timeslot of the two consecutive timeslots used. Only even timeslots are allowed in this case.

0E$_h$ IFS4 Interface Select 4

15			0
HP	I1	I2	I3

Reset Value

0	0	0	0

HP **High-Pass for S_7**

0: Disabled

1: Enabled

I1 **Input signal 1 for S_8**

I2 **Input signal 2 for S_8**

I3 **Input signal 3 for S_8**

As all sources are always active, unused sources must be set to 0 (S_0).

$0F_h$ IFG5 Interface Gain 5

15	0
ATT1[1)]	ATT2[1)]
Reset Value	
255 (0 dB)	255 (0 dB)

[1)] Can be changed on the fly.

ATT1 Attenuation for I3 (Channel 1)

In order to obtain an attenuation *A* the parameter ATT1 can be calculated by the following formula:

$$\text{ATT1} = 256 \times 10^{A/20\ \text{dB}}$$

ATT2 Attenuation for I3 (Channel 2)

In order to obtain an attenuation *A* the parameter ATT2 can be calculated by the following formula:

$$\text{ATT2} = 256 \times 10^{A/20\ \text{dB}}$$

10_h UA Universal Attenuator

15				0
ATT[1)]	0	0	0	I1

Reset Value

0 (-100 dB)	0	0	0	0

1) Can be changed on the fly.

ATT Attenuation for UA

For a given attenuation *A* [dB] the parameter ATT can be calculated by the following formula:

$$\mathrm{ATT} = 256 \times 10^{A/20\,\mathrm{dB}}$$

I1 Input Selection for UA

11_h DGCTL DTMF Generator Control

15												0
EN	MD	0	0	0	0	0	0	0	0	0	0	DTC

Reset Value

0	0	0	0	0	0	0	0	0	0	0	0	0

EN **Generator Enable**

0: Disabled

1: Enabled

MD **Mode**

0: raw

1: cooked

DTC **Dial Tone Code (cooked mode)**

3	2	1	0	Digit	Frequency
0	0	0	0	1	697/1209
0	0	0	1	2	697/1336
0	0	1	0	3	697/1477
0	0	1	1	A	697/1633
0	1	0	0	4	770/1209
0	1	0	1	5	770/1336
0	1	1	0	6	770/1477
0	1	1	1	B	770/1633
1	0	0	0	7	852/1209
1	0	0	1	8	852/1336
1	0	1	0	9	852/1477
1	0	1	1	C	852/1633
1	1	0	0	*	941/1209
1	1	0	1	0	941/1336
1	1	1	0	#	941/1477
1	1	1	1	D	941/1633

12_h DGF1 DTMF Generator Frequency 1

15	0
0	FRQ

FRQ Frequency of Generator 1

The parameter FRQ for a given frequency *f* [Hz] can be calculated by the following formula:

$$FRQ = 32768 \times \frac{f}{4000Hz}$$

13_h DGF2 DTMF Generator Frequency 2

15		0
0	FRQ	

FRQ Frequency of Generator 2

he parameter FRQ for a given frequency *f* [Hz] can be calculated by the following formula:

$$FRQ = 32768 \times \frac{f}{4000Hz}$$

14_h DGL DTMF Generator Level

15			0
0	LEV2	0	LEV1

LEV2 Signal Level of Generator 2

In order to obtain a signal level *L* (relative to the PCM maximum value) for generator 2 the value of LEV2 can be calculated according to the following formula:

$$\mathrm{LEV2} = 128 \times 10^{L/20\,\mathrm{dB}}$$

LEV1 Signal Level of Generator 1

In order to obtain a signal level *L* (relative to the PCM maximum value) for generator 1 the value of LEV1 can be calculated according to the following formula:

$$\mathrm{LEV1} = 128 \times 10^{L/20\,\mathrm{dB}}$$

15_h DGATT DTMF Generator Attenuation

15	0
ATT2	ATT1

ATT2 Attenuation of Signal S_{10}

In order to obtain attenuation *A* the parameter ATT2 can be calculated by the formula:

$$\mathrm{ATT2} = \begin{cases} 128 + 1024 \times 10^{A/20\ \mathrm{dB}} & ;A > 18,1\ \mathrm{dB} \\ 128 \times 10^{A/20\ \mathrm{dB}} & ;A < 18,1\ \mathrm{dB} \end{cases}$$

ATT1 Attenuation of Signal S_9

In order to obtain attenuation *A* the parameter ATT1 can be calculated by the formula:

$$\mathrm{ATT1} = \begin{cases} 128 + 1024 \times 10^{A/20\ \mathrm{dB}} & ;A > 18,1\ \mathrm{dB} \\ 128 \times 10^{A/20\ \mathrm{dB}} & ;A < 18,1\ \mathrm{dB} \end{cases}$$

16_h CNGCTL Calling Tone Control

15											0
EN	0	0	0	0	0	0	0	0	0	0	I1

Reset Value

0	0	0	0	0	0	0	0	0	0	0	0

EN **Enable**

0: CNG unit disabled

1: CNG unit enabled

I1 **Input Selection for Calling Tone Detector**

17_h CNGBT CNG Burst Time

15	0
0	TIME

TIME Minimum Time for Calling Tone

In order to obtain the parameter TIME for a minimum time *t* the following formula can be used:

$$\mathrm{TIME} = t / 0.125\ \mathrm{ms}$$

18_h CNGLEV CNG Minimal Signal Level

15		0
0	0	MIN

MIN Minimum Signal Level for Calling Tone

In order to obtain the parameter MIN for a minimum signal level *L* the following formula can be used:

$$\mathrm{MIN} = 16384 \times 10^{L/20\ \mathrm{dB}}$$

19_h CNGRES CNG Signal Resolution

15				0
1	1	1	1	RES

RES Signal Resolution

The parameter RES depends on the noise level *L* as follows:

$$\mathrm{RES} = -4096 \times 10^{L/20\ \mathrm{dB}}$$

1A$_h$ ATDCTL0 Alert Tone Detection 0

15										0
EN	0	0	I1	0	0	0	0	0	0	ATC

Reset Value

0	0	0	0	0	0	0	0	0	0	-[1]

[1] undefined

EN **Enable alert tone detection**

0: The alert tone detection is disabled

1: The alert tone detection is enabled

I1 **Input signal selection**

ATC **Alert Tone Code**

1	0	Description
0	0	no tone
0	1	2130
1	0	2750
1	1	2130/2750

$1B_h$ ATDCTL1 Alert Tone Detection 1

15								0
MD	0	0	DEV	0	0	0	0	MIN

MD **Alert tone detection mode**

0: Only dual tones will be detected

1: Either dual or single tones will be detected

DEV **Maximum frequency deviation for alert tone**

0: 0.5%

1: 1.1%

MIN **Minimum level of alert tone signal**

For a minimum signal level *min* the parameter MIN is given by the following formula:

$$\mathrm{MIN} = 2560 \times 10^{\mathrm{min}/20\ \mathrm{dB}}$$

$1C_h$ CIDCTL0 Caller ID Control 0

15				0
EN	0	0	I1	DATA
Reset Value				
0	0	0	0	0

EN **CID Enable**

0: Disabled

1: Enabled

I1 **Input signal selection**

DATA **Last received data byte**

$1D_h$ CIDCTL1 Caller ID Control 1

15		0
NMB	NMSS	MIN

NMB Minimum Number of Mark Bits

15	14	13	12	11	10	Description
0	0	0	0	0	0	0
0	0	0			1	10
...	...	...	...	...	...	...
1	1	1	1	1	1	630

NMSS Minimum Number of Mark/Space Sequences

9	8	7	6	5	Description
0	0	0	0	0	1
0	0	0	0	1	11
...	...	...	...	...	
1	1	1	1	1	311

MIN Minimum Signal Level for CID Decoder

For a minimum signal level *min* the parameter MIN is given by the following formula:

$$\mathrm{MIN} = 640 \times 10^{\mathrm{min}/20\ \mathrm{dB}}$$

20_h CPTCTL Call Progress Tone Control

15											0
EN	MD	0	0	0	0	0	0	0	0	0	I1

Reset Value

0	0	0	0	0	0	0	0	0	0	0	0

EN **CPT Detector Enable**

0: Disabled

1: Enabled

MD **CPT Mode**

0: raw

1: cooked

I1 **Input signal selection**

21_h CPTTR Call Progress Tone Thresholds

15			0
NUM	0	SN	MIN

NUM Number of Cycles

15	14	13	cooked mode	raw mode
0	0	0	reserved	0
0	0	1	2	reserved
...	...	...	...	reserved
1	1	1	8	reserved

SN Minimal Signal-to-Noise Ratio

11	10	9	8	Description
1	1	1	1	9 dB
1	0	0	0	12 dB
0	1	0	0	15 dB
0	0	1	0	18 dB
0	0	0	0	22 dB

MIN Minimum Signal Level for CPT Detector

Value	Description
89_h	-40 dB
85_h	-42 dB
80_h	-44 dB
$9A_h$	-46 dB
95_h	-48 dB
90_h	-50 dB

22_h CPTMN CPT Minimum Times

15	0
MINB	MING

MINB Minimum Time for CPT Burst

The parameter MINB for a minimal burst time *TBmin* can be calculated by the following formula:

$$MINB = \frac{TBmin - 32\ ms}{4}$$

MING Minimum Time for CPT Gap

The parameter MING for a minimal burst time *TGmin* can be calculated by the following formula:

$$MING = \frac{TGmin - 32\ ms}{4}$$

23_h CPTMX CPT Maximum Times

15	0
MAXB	MAXG

MAXB Maximum Time for CPT Burst

The parameter MAXB for a maximal burst time of *TBmax* can be calculated by the following formula:

$$MAXB = \frac{TBmax - TBmin}{8}$$

MAXG Maximum Time for CPT Gap

The parameter MAXG for a maximal burst time of *TGmax* can be calculated by the following formula:

$$MAXG = \frac{TGmax - TGmin}{8}$$

24_h CPTDT CPT Delta Times

15	0
DIFB	DIFG

DIFB Maximum Time Difference between consecutive Bursts

The parameter DIFB for a maximal difference of *t* ms of two burst durations can be calculated by the following formula:

$$DIFB = \frac{t}{2\ ms}$$

DIFG Maximum Time Difference between consecutive Gaps

The parameter DIFG for a maximal difference of *t* ms of two gap durations can be calculated by the following formula:

$$DIFG = \frac{t}{2\ ms}$$

25_h LECCTL Line Echo Cancellation Control

15 … **0**

EN	MD	0	0	0	0	I1	I2
Reset Value							
0	0	0	0	0	0	0	0

EN **Enable**

0: Disabled

1: Enabled

MD **Mode**

0: Normal

1: Extended

I1 **Input signal selection for I_1**

I2 **Input signal selection for I_2**

26_h LECLEV Minimal Signal Level for Line Echo Cancellation

15	0
0	MIN

MIN

The parameter MIN for a minimal signal level *L* (dB) can be calculated by the following formula:

$$MIN = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

27_h LECATT Externally Provided Attenuation

15	0
0	ATT

ATT

The parameter ATT for an externally provided attenuation *A* (dB) can be calculated by the following formula:

$$\text{ATT} = \frac{512 \times \text{A}}{5 \times \log 2}$$

28_h LECMGN Margin for Double Talk Detection

15	0
0	MGN

MGN

The parameter MGN for a margin of *L* (dB) can be calculated by the following formula:

$$\text{MGN} = \frac{512 \times \text{L}}{5 \times \log 2}$$

29$_h$ DDCTL DTMF Detector Control

15							0
EN	0	0	I1	0	0	0	DTC

Reset Value

0	0	0	0	0	0	0	-[1)]

1) undefined

EN **Enable DTMF tone detection**

0: The DTMF detection is disabled

1: The DTMF detection is enabled

I1 **Input signal selection**

DTC **DTMF Tone Code**

4	3	2	1	0	Frequency	Digit
1	0	0	0	0	941 / 1633	D
1	0	0	0	1	697 / 1209	1
1	0	0	1	0	697 / 1336	2
1	0	0	1	1	697 / 1477	3
1	0	1	0	0	770 / 1209	4
1	0	1	0	1	770 / 1336	5
1	0	1	1	0	770 / 1477	6
1	0	1	1	1	852 / 1209	7
1	1	0	0	0	852 / 1336	8
1	1	0	0	1	852 / 1477	9
1	1	0	1	0	941 / 1336	0
1	1	0	1	1	941 / 1209	*
1	1	1	0	0	941 / 1477	#
1	1	1	0	1	697 / 1633	A
1	1	1	1	0	770 / 1633	B
1	1	1	1	1	852 / 1633	C

$2A_h$ DDTW DTMF Detector Signal Twist

15	0
0	TWIST

TWIST Signal twist for DTMF tone

In order to obtain a minimal signal twist *T* the parameter TWIST can be calculated by the following formula:

$$\text{TWIST} = 32768 \times 10^{(0.5\text{ dB} - \text{T})/10\text{ dB}}$$

Note: TWIST must be in the range [4096,20480]

$2B_h$ DDLEV DTMF Detector Minimum Signal Level

15										0
1	1	1	1	1	1	1	1	1	1	MIN

MIN Minimum Signal Level

5	4	3	2	1	0	Description
0	0	1	1	1	0	-50 dB
0	0	1	1	1	1	-49 dB
...	...	...	...	...	...	...
1	0	0	0	0	1	-31 dB
1	0	0	0	1	0	-30 dB

Note: Values outside the given range are reserved and must not be used.

2E$_h$ FCFCTL Equalizer Control

15						0
EN	0	ADR	0	0	0	I

Reset Value

0	0	0	0	0	0	0

EN **Enable equalizer**

0: The equalizer is disabled

1: The equalizer is enabled

ADR **Coefficient address**

13	12	11	10	9	8	Coefficient
0	0	0	0	0	0	A1
0	0	0	0	0	1	A2
0	0	0	0	1	0	A3
0	0	0	0	1	1	A4
0	0	0	1	0	0	A5
0	0	0	1	0	1	A6
0	0	0	1	1	0	A7
0	0	0	1	1	1	A8
0	0	1	0	0	0	A9
0	0	1	0	0	1	B2
0	0	1	0	1	0	B3
0	0	1	0	1	1	B4
0	0	1	1	0	0	B5
0	0	1	1	0	1	B6
0	0	1	1	1	0	B7
0	0	1	1	1	1	B8
0	1	0	0	0	0	B9
0	1	0	0	0	1	C1
0	1	0	0	1	0	D1
0	1	0	0	1	1	D2
0	1	0	1	0	0	D3
0	1	0	1	0	1	D4
0	1	0	1	1	0	D5

13	12	11	10	9	8	Coefficient
0	1	0	1	1	1	D6
0	1	1	0	0	0	D7
0	1	1	0	0	1	D8
0	1	1	0	1	0	D9
0	1	1	0	1	1	D10
0	1	1	1	0	0	D11
0	1	1	1	0	1	D12
0	1	1	1	1	0	D13
0	1	1	1	1	1	D14
1	0	0	0	0	0	D15
1	0	0	0	0	1	D16
1	0	0	0	1	0	D17
1	0	0	0	1	1	C2

I1 Input signal selection

$2F_h$ FCFCOF Equalizer Coefficient Data

15	0
V	

V **Coefficient value**

For the coefficient A_1-A_9, B_2-B_9 and D_1-D_{17} the following formula can be used to calculate V for a coefficient *c*:

$$V = 32768 \times c \qquad ; -1 \le c < 1$$

For the coefficients C_1 and C_2 the following formula can be used to calculate V for a coefficient *c*:

$$V = 128 \times c \qquad ; 1 \le c < 256$$

30_h SCCTL Speech Coder Control

15							0
EN	HQ[1)]	VC	0	0	0	I1	I2

Reset Value

0	0	0	0	0	0	0	0

1) Can be changed on the fly.

EN **Enable**

0: Disabled

1: Enabled

HQ **High Quality Mode**

0: Long Play Mode

1: High Quality Mode

VC **Voice Controlled Start of Recording**

0: Disabled

1: Enabled

I1 **Input signal selection (first input)**

I2 **Input signal selection (second input)**

31_h SCCT2 Speech Coder Control 2

15	0
TIME	MIN

TIME

The parameter TIME for a time *t* ([ms]) can be calculated by the following formula:

$$\text{TIME} = \frac{t}{32}$$

MIN

The parameter MIN for a signal level *L* ([dB]) can be calculated by the following formula:

$$\text{MIN} = 16384 \times 10^{\frac{L}{20}}$$

32$_h$ SCCT3 Speech Coder Control 3

15									0
0	LP	0	0	0	0	0	0	0	0

LP

The parameter LP for a time constant of *t* ([ms]) can be calculated by the following formula:

$$LP = \frac{256}{t}$$

34_h SDCTL Speech Decoder Control

15														0
EN	0	0	0	0	0	0	0	0	0	0	0	0		SPEED

Reset Value

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EN **Enable**

0: Disabled

1: Enabled

SPEED **Playback Speed**

1	0	Description
0	0	normal speed
0	1	0.5 times normal speed
1	0	1.5 times normal speed
1	1	2.0 times normal speed

38_h AGCCTL AGC Control

15 … 0

EN	0	0	0	0	0	I1	I2

Reset Value

0	0	0	0	0	0	0	0

EN **Enable**

0: Disabled

1: Enabled

I1 **Input signal selection for I_1**

I2 **Input signal selection for I_2**

39_h AGCATT Automatic Gain Control Attenuation

15	0
ATT	

Reset Value

0 (-100 dB)

ATT

The parameter ATT for an attenuation *A* ([dB]) can be calculated by the following formula:

$$ATT = 32768 \times 10^{\frac{A}{20}}$$

$3A_h$ AGC1 Automatic Gain Control 1

15	0
COM	AG_INIT

COM

The parameter COM for a signal level *L* ([dB]) can be calculated by the following formula:

$$COM = \begin{cases} 128 + 10^{\frac{L + 66,22}{20}} & ;L < -42,14 \text{ dB} \\ 10^{\frac{L + 42,14}{20}} & ;L > -42,14 \text{ dB} \end{cases}$$

AG_INIT

In order to obtain an initial gain *G* ([db]) the parameter AG_INIT can be calculated by the following formula:

$$AG\_INIT = \begin{cases} 128 + 10^{\frac{G + 18,06}{20}} & ;G < 24 \text{ dB} \\ 10^{\frac{G - 6,02}{20}} & ;G > 24 \text{ dB} \end{cases}$$

$3B_h$ AGC2 Automatic Gain Control 2

15	0
SPEEDL	SPEEDH

SPEEDL

This parameter has no dimension. It controls the regulation speed of the AGC for signal levels below the comparator threshold (AGC1:COM). The higher the value the faster the AGC. Setting this parameter to 0 inhibits regulation.

SPEEDH

This parameter has no dimension. It controls the regulation speed of the AGC for signal levels above the comparator threshold (AGC1:COM). The higher the value the faster the AGC. Setting this parameter to 0 inhibits regulation.

$3C_h$ AGC3 Automatic Gain Control 3

15	0
MIN	MAX

MIN

The parameter MIN for a gain *G* ([dB]) can be calculated by the following formula:

$$MIN = \begin{cases} 128 + 10^{\frac{G + 18,06}{20}} & ;G < 24\ dB \\ 10^{\frac{G - 6,02}{20}} & ;G > 24\ dB \end{cases}$$

MAX

The parameter MAX for an attenuation *A* ([dB]) can be calculated by the following formula:

$$MAX = 10^{\frac{A + 42,14}{20}}$$

$3D_h$ AGC4 Automatic Gain Control 4

15	0
DEC	LIM

DEC

The parameter DEC for a time constant *t* ([1/ms]) is given by the following formula:

$$DEC = \frac{256}{t}$$

LIM

The parameter LIM for a signal level *L* ([dB]) can be calculated by the following formula:

$$LIM = \begin{cases} 128 + 10^{\frac{L + 90,3}{20}} & ;L < 66{,}22\ dB \\ 10^{\frac{L + 66,22}{20}} & ;L > 66{,}22\ dB \end{cases}$$

$3E_h$ AGC5 Automatic Gain Control 5

15									0
0	0	0	0	0	0	0	0	1	LP

LP

The parameter LP for a time constant *t* ([1/ms]) is given by the following formula:

$$LP = \frac{16}{t}$$

40_h FCTL File Control

15								0
0	MD	MS	TS	0	0	0	0	FNO

Reset Value

0	0	0	0	0	0	0	0	0

MD Mode

0: Audio Mode

1: Binary Mode

MS Memory Space

0: R/W Memory

1: Voice Prompt Directory

TS Time Stamp

0: no update of RTC1/RTC2 entry of file descriptor

1: RTC1/RTC2 entries are updated by content of RTC1/RTC2 registers.

FNO File Number

41_h FCMD File Command

15											0
0	IN	RD	0	0	0	0	0	ABT	EIE	0	CMD

Reset Value

0	0	0	0	0	0	0	0	0	0	0	0

IN **Initialize**

0: no

1: yes (if CMD=1111)

RD **Remap Directory**

0: no

1: yes

ABT **Abort Command**

0: no

1: abort recompress

EIE **Enable Immediate Execution**

0: disabled (default, always possible)

1: enabled (restricted to certain commands and operating modes)

CMD **File Command**

4	3	2	1	0	Description
0	0	0	0	0	Open File
0	0	0	0	1	Activate
0	0	0	1	0	Seek
0	0	0	1	1	Cut File
0	0	1	0	0	Read Data
0	0	1	0	1	Write Data
0	0	1	1	0	Memory Status
0	0	1	1	1	Recompress file
0	1	0	0	0	Read File Descriptor - User
0	1	0	0	1	Write File Descriptor - User

4	3	2	1	0	Description
0	1	0	1	0	Read File Descriptor - RTC1
0	1	0	1	1	Read File Descriptor - RTC2
0	1	1	0	0	Read File Descriptor - LEN
0	1	1	0	1	Garbage Collection
0	1	1	1	0	Open Next Free File
0	1	1	1	1	Initialize
1	0	0	0	0	DMA Read
1	0	0	0	1	DMA Write
1	0	0	1	0	Erase Block
1	0	0	1	1	Set Address
1	0	1	-	-	reserved
1	1	0	-	-	reserved
1	1	1	-	-	reserved

42_h FDATA File Data

15	0
FREE	

Reset Value

0

The FDATA register contains the following information after a memory status command:

FREE Free Blocks

Number of blocks (1 kByte) currently usable for recording.

43_h FPTR File Pointer

15					0
File Pointer					
0	0	0	0	0	Phrase selector

Reset Value

0

47h SPSCTL SPS Control

15										0
POS	0	0	0	0	0	0	0	MODE	SP1	SP0

Reset Value

0	0	0	0	0	0	0	0	0	-[1]	-[1]

1) undefined

POS Position of Status Register Window

15	14	13	12	SPS_0	SPS_1
0	0	0	0	Bit 0	Bit 1
0	0	0	1	Bit 1	Bit 2
...	...	...	...	...	...
1	1	1	0	Bit 14	Bit 15

MODE Mode of SPS Interface

4	3	2	Description
0	0	0	Disabled (SPS_0 and SPS_1 zero)
0	0	1	Output of SP1 and SP0
1	0	1	Expanded address output
1	1	0	Output of STATUS register

SP1 Direct Control for SPS_1

0: SPS_1 set to 0

1: SPS_1 set to 1

SP0 Direct Control for SPS_0

0: SPS_0 set to 0

1: SPS_0 set to 1

Note: If mode 1 has been selected prior to power-down, both mode 1 and the values of SP1 and SP0 are retained during power-down and wake-up. Other modes are reset to 0 during power down.

48$_h$ RTC1 Real Time Clock 1

15					0
0	0	0	0	MIN	SEC
Reset Value					
0	0	0	0	0	0

MIN Minutes

Number of minutes elapsed in the current hour (0-59).

SEC Seconds

Number of seconds elapsed in the current minute (0-59).

49_h RTC2 Real Time Clock 2

15 DAY	HR 0

Reset Value

DAY	HR
0	0

DAY Days

Number of days elapsed since last reset (0-2047).

HR Hours

Number of hours elapsed in the current day (0-23).

$4A_h$ DOUT0 Data Out (Timeslot 0)

15				0
0	0	0	0	DATA

Reset Value

0	0	0	0	0

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{12}=1 (only if HWCONFIG1:APP=10).

Note: This register cannot be read.

$4B_h$ DOUT1 Data Out (Timeslot 1)

15				0
0	0	0	0	DATA

Reset Value

0	0	0	0	0

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{13}=1 (only if HWCONFIG1:APP=10).

Note: This register cannot be read.

$4C_h$ DOUT2 Data Out (Timeslot 2)

15				0
0	0	0	0	DATA

Reset Value

0	0	0	0	0

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{14}=1 (only if HWCONFIG1:APP=10).

Note: This register cannot be read.

$4D_h$ DOUT3 Data Out (Timeslot 3 or Static Mode)

15	0
DATA	

Reset Value

0

DATA Output Data

Output data for pins MA_0-MA_{11} while MA_{15}=1 (only if HWCONFIG1:APP=10).

Output data for pins MA_0-MA_{15} (only if HWCONFIG1:APP=01)

Note: This register cannot be read.

$4E_h$ DIN Data In (Timeslot 3 or Static Mode)

15	0
DATA	

DATA Input Data

Input data for pins MA_0-MA_{11} at falling edge of MA_{12} (only if HWCONFIG1:APP=10).
Input data for pins MA_0-MA_{15} (only if HWCONFIG1:APP=01)

$4F_h$ DDIR Data Direction (Timeslot 3 or Static Mode)

15	0
DIR	
Reset Value	
0 (all inputs)	

DIR Port Direction

Port direction during MA_{12}=1 or in static mode.

0: input

1: output

Note: This register cannot be read.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	-20 to 85	°C
Storage temperature	T_{STG}	– 65 to125	°C
Supply Voltage	V_{DD}	-0.5 to 4.2	V
Supply Voltage	V_{DDA}	-0.5 to 4.2	V
Supply Voltage	V_{DDP}	-0.5 to 6	V
Voltage of pin with respect to ground: $XTAL_1$, $XTAL_2$	V_S	0 to V_{DDA}	V
Voltage on any pin with respect to ground	V_S	If V_{DDP} < 3 V: – 0.4 to V_{DD} + 0.5 If V_{DDP} > 3 V: – 0.4 to V_{DDP} + 0.5	V

ESD integrity (according MIL-Std. 883D, method 3015.7): 2 kV

Exception: The pins $\overline{INT}$, SDX, DU/DX, DD/DR, SPS_0, SPS_1 and MD_0-MD_7 are not protected against voltage stress >1 kV.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.2 DC Characteristics

V_{DD}/V_{DDA} = 3.3 V ± 0.3 V; V_{DDP} = 5 V ± 10%; V_{SS}/V_{SSA} = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input leakage current	I_{IL}	– 1.0		1.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
H-input level (except MA_0-MA_{15}, $XTAL_1$,OSC_1)	V_{IH1}	2.0		V_{DDP} + 0.3	V	
H-input level (OSC_1)	V_{IH2}	0.8 V_{DD}		V_{DDA} + 0.3	V	
H-input level (MA_0-MA_{15}, MCTL[1)])	V_{IH3}	2.0		V_{DD}	V	
L-input level (except pins $XTAL_1$,OSC_1)	V_{IL1}	– 0.3		0.8	V	

V_{DD}/V_{DDA} = 3.3 V ± 0.3 V; V_{DDP} = 5 V ± 10%; V_{SS}/V_{SSA} = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
L-input level (OSC_1)	V_{IL2}	– 0.3		0.2 V_{DDA}	V	
H-output level (except DU/DX, DD/DR, MA_0-MA_{15}, SPS_0, SPS_1, MD_0-MD_7)	V_{OH1}	V_{DD} – 0.45			V	I_O = 2 mA
H-output level (SPS_0, SPS_1, MD_0-MD_7, SDX, $\overline{INT}$)	V_{OH2}	V_{DD} – 0.6			V	I_O = 2 mA
H-output level (MA_0-MA_{15})	V_{OH3}	V_{DD} – 0.45			V	I_O = 5 mA
H-output level (DU/DX, DD/DR)	V_{OH4}	V_{DD} – 0.6			V	I_O = 7 mA
L-output level (except DU/DX, DD/DR, MA_0-MA_{15})	V_{OL1}			0.45	V	I_O = – 2 mA
L-output level (MA_0-MA_{15}) (address mode or APP output)	V_{OL2}			0.45	V	I_O = – 5 mA
L-output current (MA_0-MA_{15}) (after reset)	I_{LO}	50	150	240	µA	RST=1
H-output current (MCTL[1])	I_{HO}	25	65	120	µA	RST=1
L-output level (pins DU/DX, DD/DR)	V_{OL3}			0.45	V	I_O = – 7 mA
Internal pullup current ($\overline{FRDY}$)	I_{LI}	350	750	1300	µA	
Input capacitance	C_I			10	pF	
Output capacitance	C_O			15	pF	
V_{DD} supply current (power down, no refresh, no RTC)	I_{DDS1}		10	50	µA	
V_{DD} supply current (power down, refresh, RTC)	I_{DDS2}		20	70	µA	
V_{DD} supply current operating	I_{DDO}		55	70	mA	V_{DD} = 3.3 V
V_{DDP} supply current	I_{DDP}		1	10	µA	

[1] MCTL signals are ($\overline{W}$/$\overline{FWE}$, $\overline{VPRD}$/FCLE, $\overline{RAS}$/$\overline{FOE}$, $\overline{CAS_0}$/ALE, $\overline{CAS_1}$/$\overline{FCS}$)

4.3 AC Characteristics

Digital inputs are driven to 2.4 V for a logical “1” and to 0.45 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and 0.8 V for a logical “0”. The AC-testing input/output waveforms are shown below.

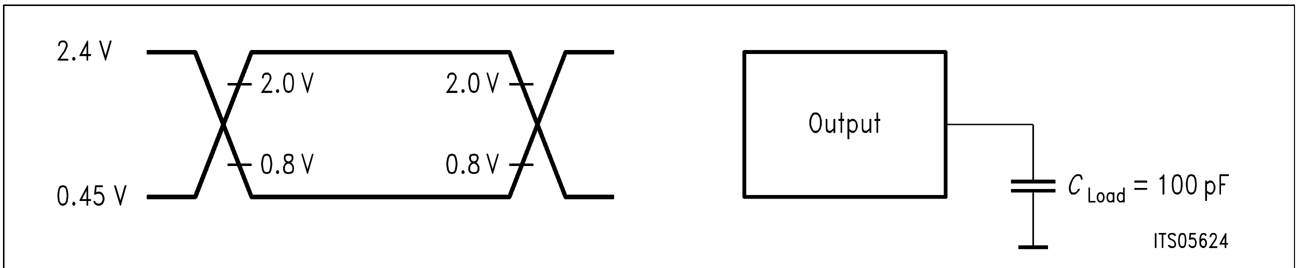


Figure 55 Input/Output Waveforms for AC-Tests

DTMF Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-1.5		1.5	%	
Frequency deviation reject		3.5		-3.5	%	
Acceptance level		-45		0	dB	rel. to max. PCM
Rejection level				-50	dB	rel. to max. PCM
Twist deviation accept		+/-2		+/-8	dB	programmable
Noise Tolerance				12	dB	
Signal duration accept		40			ms	
Signal duration reject				23	ms	
Gap duration accept		18			ms	

CPT Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency acceptance range		300		640	Hz	
Frequency rejection range		800		200	Hz	
Acceptance level		-45		0	dB	rel. to max. PCM
Rejection level				-50	dB	rel. to max. PCM
Signal duration accept		50			ms	programmable
Signal duration reject				10	ms	

Caller ID Decoder

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-2		2	%	
Acceptance level		-45		0	dB	rel. to max. PCM
Transmission rate		1188	1200	1212	baud	
Noise Tolerance				-12	dB	

Alert Tone Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-0.5		0.5	%	ATDCTL1:DEV=0
Frequency deviation accept		-1.1		1.1	%	ATDCTL1:DEV=1
Frequency deviation reject		3.5		-3.5	%	
Acceptance level		-40		0	dB	rel. to max. PCM
Rejection level				-5	dB	rel. to acceptance level
Twist deviation accept				+/-7	dB	
Noise Tolerance				20	dB	
Signal duration accept		75			ms	
Gap duration accept		40			ms	

CNG Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-40		40	Hz	
Frequency deviation reject		-50		50	Hz	
Acceptance level		-45		0	dB	SNR >10 dB
Acceptance level		-50		0	dB	SNR >15 dB
Rejection level		-3 dB			dB	rel. to CNGLEV:MIN
Signal duration reject				-1	%	rel. to CNGBT:TIME

Status Register Update Time

The individual bits of the STATUS register may change due to an event (like a recognized DTMF tone) or a command. The timing can be divided into four classes

Table 74 Status Register Update Timing

Class	Timing		Comment
	Min.	Max.	
I	0	0	Immediately after command has been issued
A	0	125 µs[1]	Command has been accepted
D	125 µS	250 µs	Deactivation time after command has been issued
E	-	-	Associated event has happened

[1] one FSC period

With these definitions the timing of the individual bits in the STATUS register can be given as shown in table:

Bit	RDY	ABT	CIA	CD	CPT	CNG	SD	ERR	BSY	DTV	ATV
0->1	A	E	E	E	E	E	E	E	A[1]	E	E
1->0	I	A	A,D	E,D	E,D	D	E,D	A	E	E,D	E,D

[1] up to 30 ms if command is either SDCTL:EN=1 or SCCTL:EN=1

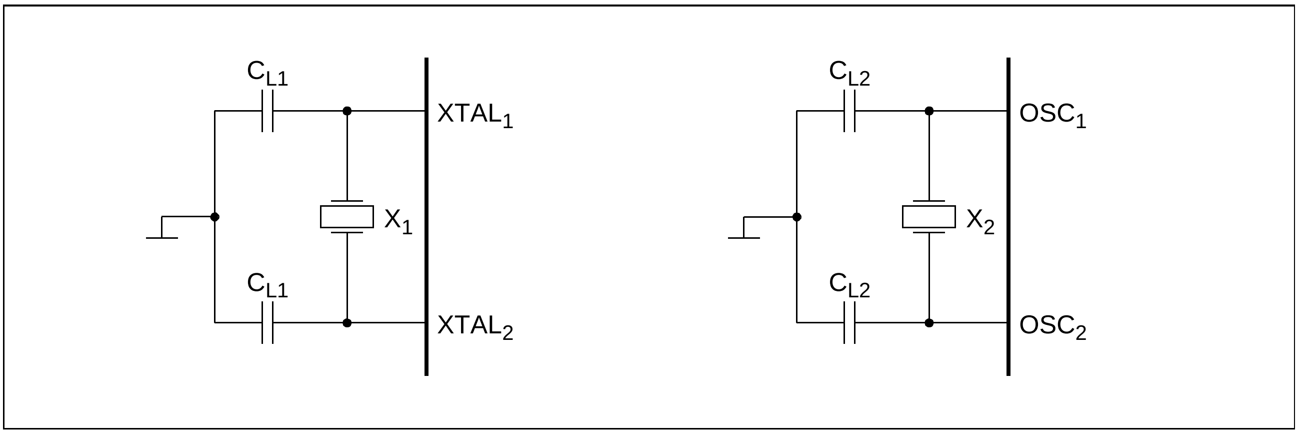


Figure 56 Oscillator Circuits

Recommended Values Oscillator Circuits	Value			Unit
	Min	Typ	Max	
Load CL_1			40	pF
Static capacitance X_1			5	pF
Motional capacitance X_1			17	fF
Resonance resistor X_1			60	Ω
Load CL_2			30	pF
Static Capacitance X_2		1.7		pF
Motional capacitance X_2		3.5		fF
Resonance resistor X_2		18	40	kΩ
Frequency deviation			100	ppm

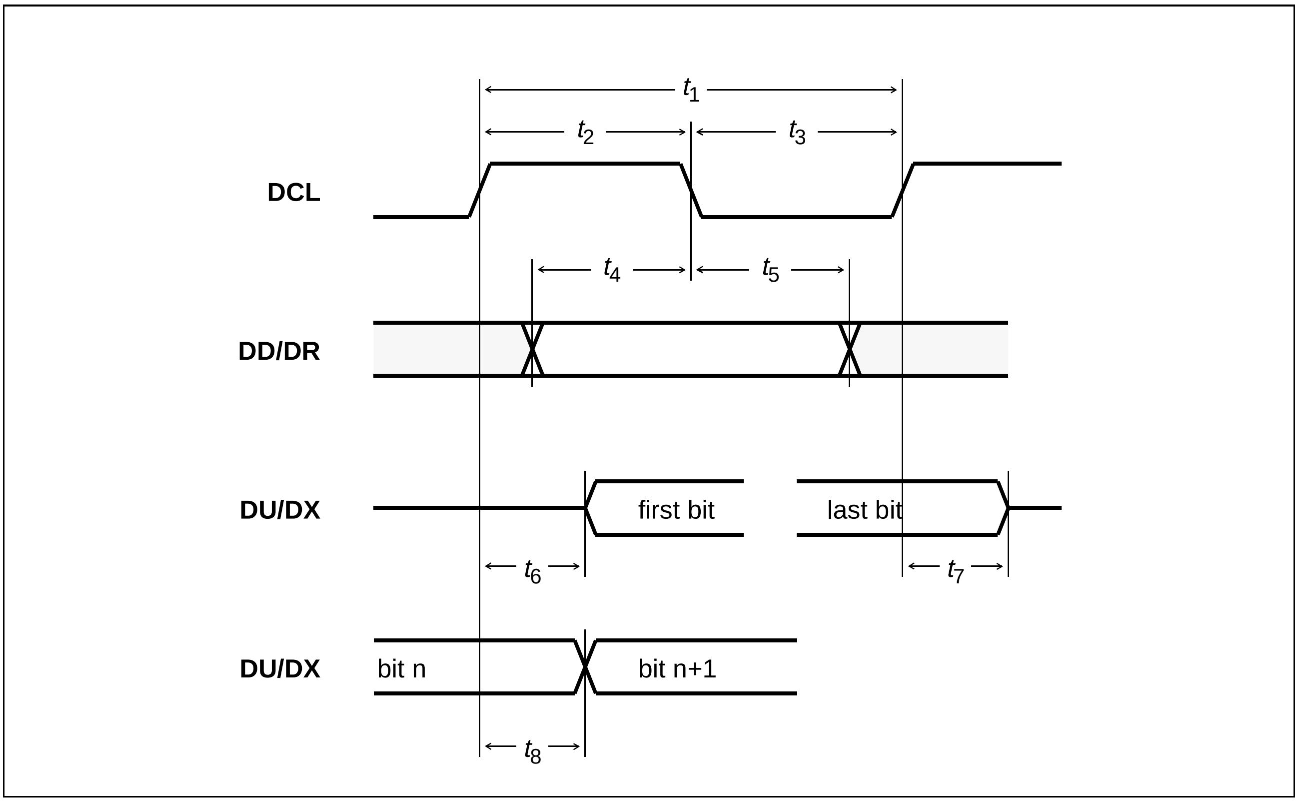


Figure 57 SSDI/IOM®-2 Interface - Bit Synchronization Timing

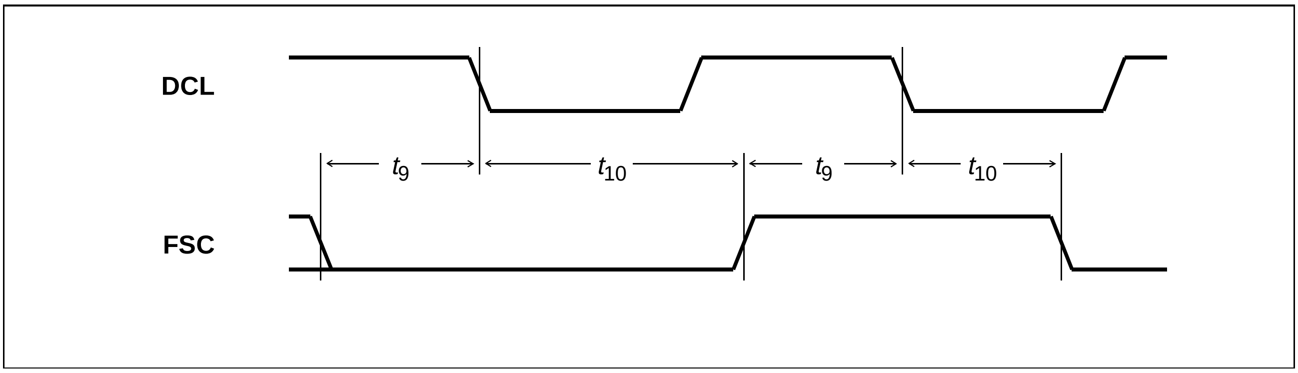


Figure 58 SSDI/IOM®-2 Interface - Frame Synchronization Timing

Parameter SSDI/IOM®-2 Interface	Symbol	Limit values		Unit
		Min	Max	
DCL period	t_1	90		ns
DCL high	t_2	35		ns
DCL low	t_3	35		ns
Input data setup	t_4	20		ns

Parameter **SSDI/IOM®-2 Interface**	Symbol	Limit values		Unit
		Min	Max	
Input data hold	t_5	20		ns
Output data from high impedance to active (FSC high or other than first timeslot)	t_6		30	ns
Output data from active to high impedance	t_7		30	ns
Output data delay from clock	t_8		30	ns
FSC setup	t_9	40		ns
FSC hold	t_{10}	40		ns
FSC jitter (deviation per frame)		-200	200	ns

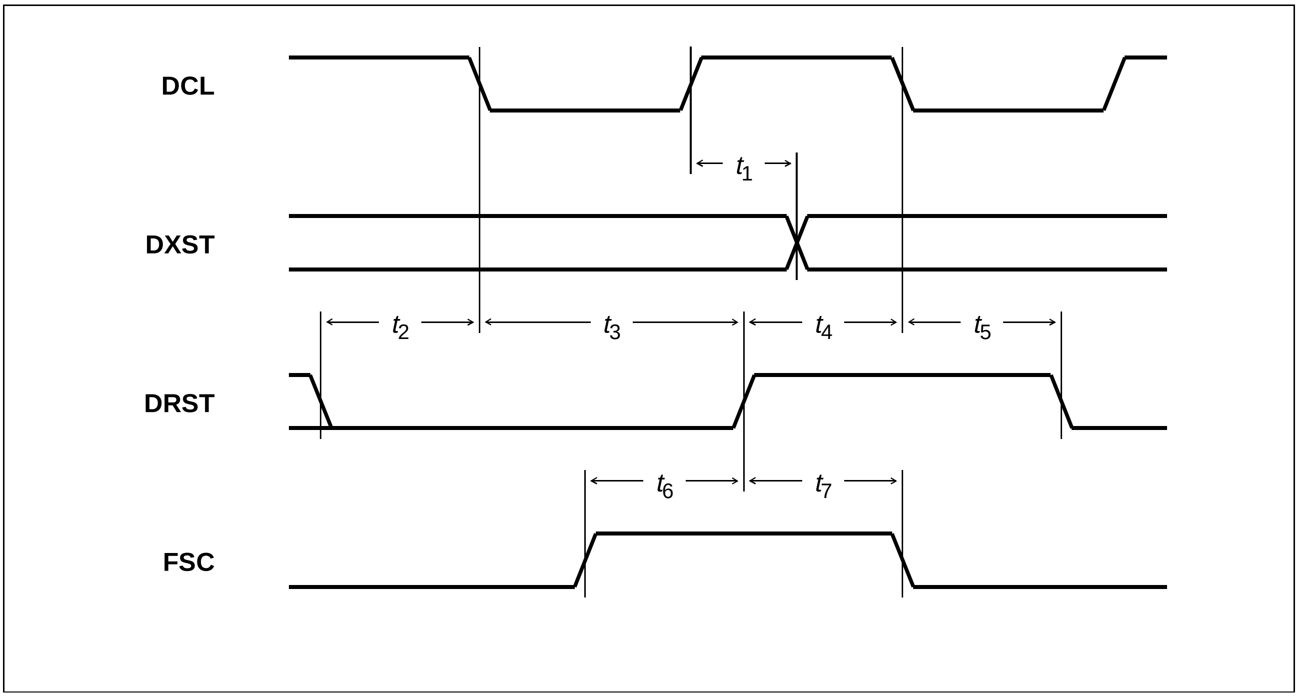


Figure 59 SSDI Interface - Strobe Timing

Parameter SSDI Interface	Symbol	Limit values		Unit
		Min	Max	
DXST delay	t_1		20	ns
DRST inactive setup	t_2	20		ns
DRST inactive hold	t_3	20		ns
DRST active setup	t_4	20		ns
DRST active hold	t_5	20		ns
FSC setup	t_6	8		DCL cycles
FSC hold	t_7	40		ns

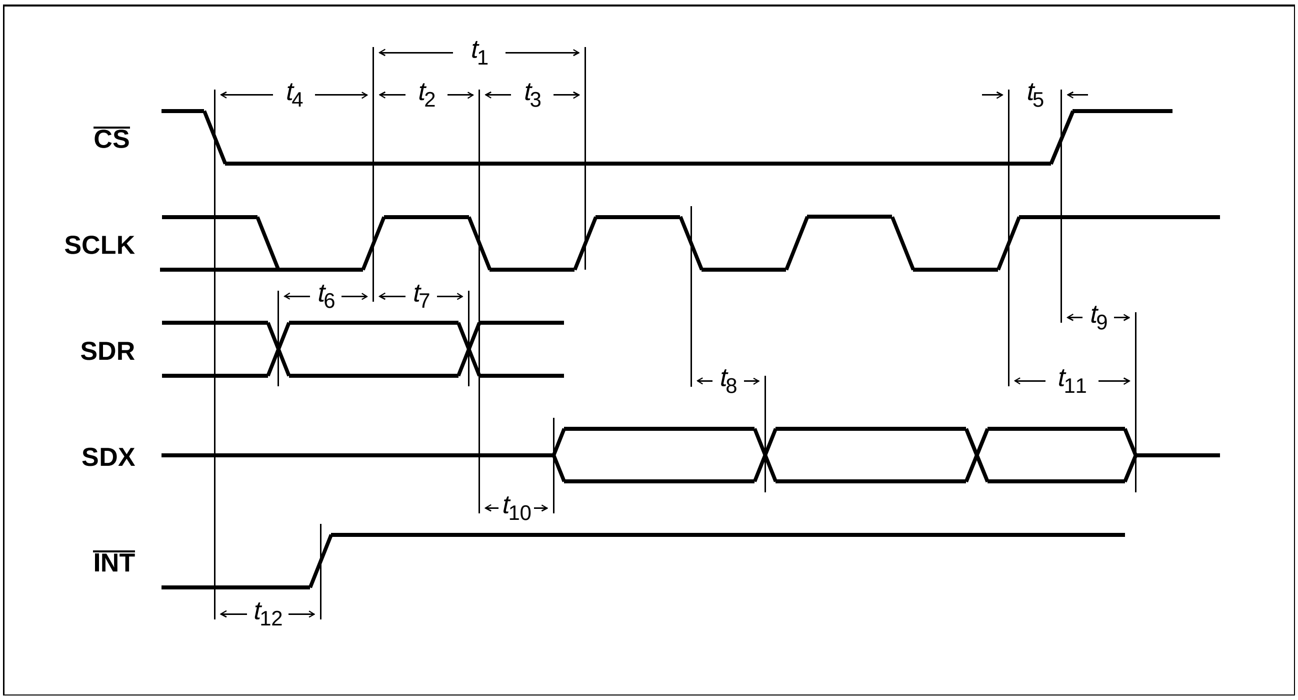


Figure 60 Serial Control Interface

Parameter SCI Interface	Symbol	Limit values		Unit
		Min	Max	
SCLK cycle time	t_1	500		ns
SCLK high time	t_2	100		ns
SCLK low time	t_3	100		ns
$\overline{CS}$ setup time	t_4	40		ns
$\overline{CS}$ hold time	t_5	10		ns
SDR setup time	t_6	40		ns
SDR hold time	t_7	40		ns
SDX data out delay	t_8		80	ns
$\overline{CS}$ high to SDX tristate	t_9		40	ns
SCLK to SDX active	t_{10}		80	ns
SCLK to SDX tristate	t_{11}		40	ns
$\overline{CS}$ to $\overline{INT}$ delay	t_{12}		80	ns

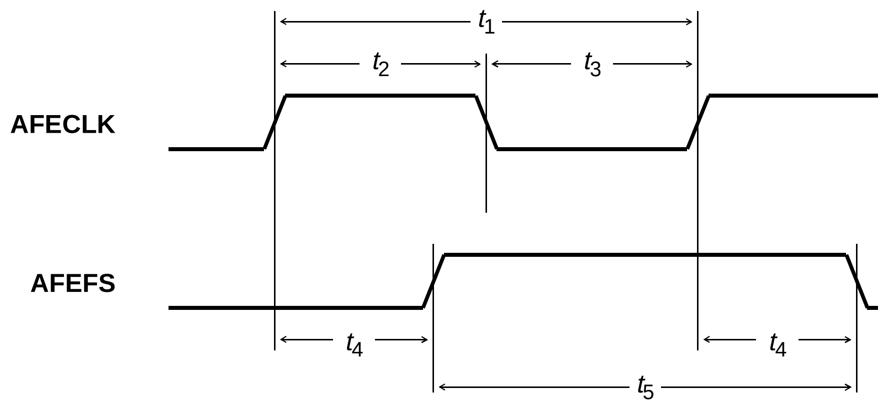


Figure 61 Clock Master Timing

Parameter AFE Interface	Symbol	Limit values		Unit
		Min	Max	
AFECLK period (HWCONFIG3:CM0=0)	t_1	13.5*p[1)]/ f_{XTAL} -10	13.5*p/f_{XTAL} +10	ns
AFECLK period (HWCONFIG3:CM0=1)	t_1	4.5*p/f_{XTAL} -10	4.5*p/f_{XTAL} +10	ns
AFECLK high	t_2	4*1/f_{XTAL}		
AFECLK low	t_3	4*1/f_{XTAL}		
AFEFS output delay	t_4		30	ns
AFEFS high	t_5	4*t_1		

1) The factor *p* is determined by HWCONFIG1:XTAL (see register description)

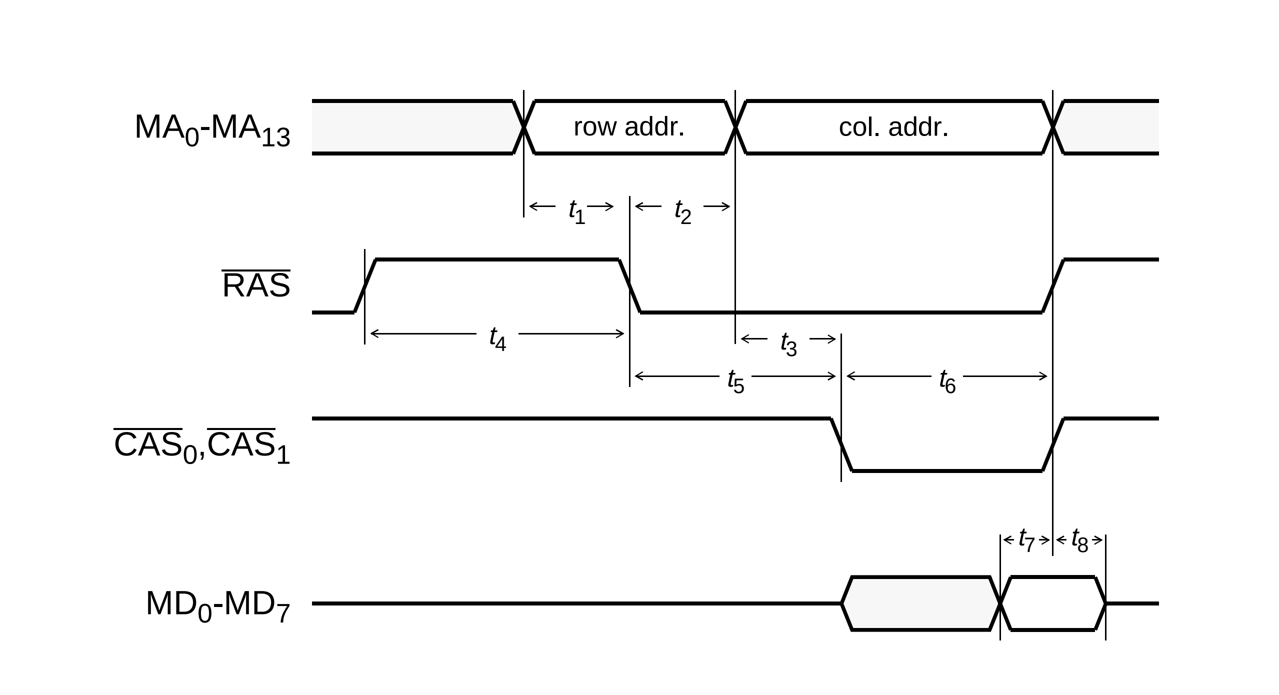


Figure 62 Memory Interface - DRAM Read Access

Parameter Memory Interface - DRAM Read Access	Symbol	Limit values		Unit
		Min	Max	
row address setup time	t_1	50		ns
row address hold time	t_2	50		ns
column address setup time	t_3	50		ns
$\overline{\text{RAS}}$ precharge time	t_4	110		ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	t_5	110	2000	ns
$\overline{\text{CAS}}$ pulse width	t_6	110	2000	ns
Data input setup time	t_7	40		ns
Data input hold time	t_8	0		ns

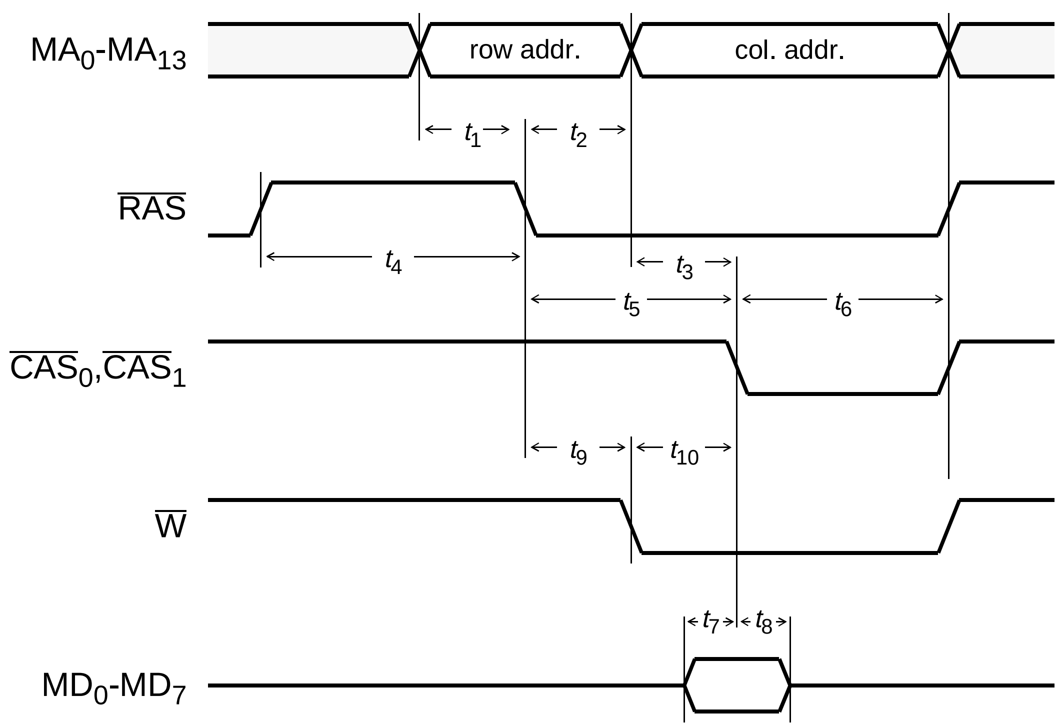


Figure 63 Memory Interface - DRAM Write Access

Parameter **Memory Interface - DRAM Write Access**	**Symbol**	**Limit values**		**Unit**
		Min	**Max**	
row address setup time	t_1	50		ns
row address hold time	t_2	50		ns
column address setup time	t_3	50		ns
$\overline{RAS}$ precharge time	t_4	110		ns
$\overline{RAS}$ to $\overline{CAS}$ delay	t_5	110	2000	ns
$\overline{CAS}$ pulse width	t_6	110	2000	ns
Data output setup time	t_7	100		ns
Data output hold time	t_8	50		ns
$\overline{RAS}$ to $\overline{W}$ delay	t_9	50		ns
$\overline{W}$ to $\overline{CAS}$ setup	t_{10}	50		ns

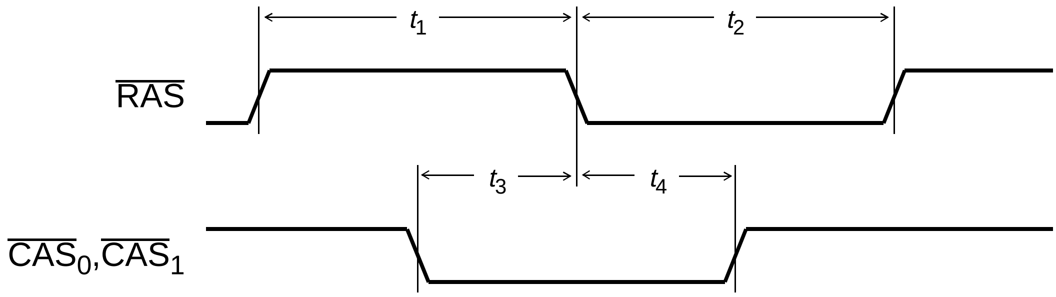


Figure 64 Memory Interface - DRAM Refresh Cycle

Parameter Memory Interface - DRAM Refresh Cycle	Symbol	Limit values		Unit
		Min	Max	
$\overline{RAS}$ precharge time	t_1	100		ns
$\overline{RAS}$ low time	t_2	200	5000	ns
$\overline{CAS}$ setup	t_3	100		ns
$\overline{CAS}$ hold	t_4	100		ns

Note: The frequency of the DRAM refresh cycle depends on the selected mode. In active mode or normal refresh mode (during power down) the minimal frequency is 64 kHz. In battery backup mode, the refresh frequency is 8 kHz.

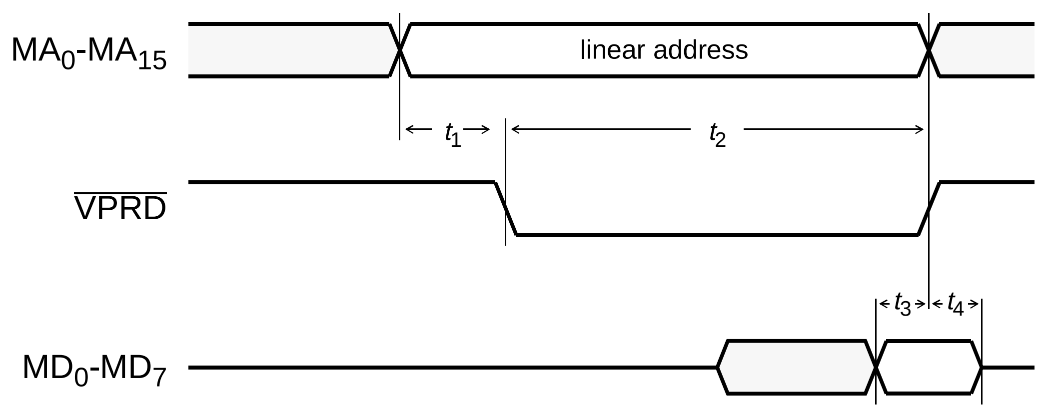


Figure 65 Memory Interface - EPROM Read

Parameter **Memory Interface - EPROM Read**	**Symbol**	**Limit values**		**Unit**
		Min	**Max**	
Address setup before $\overline{VPRD}$	t_1	110		ns
$\overline{VPRD}$ low time	t_2	500		ns
Data setup time	t_3	40		ns
Data hold time	t_4	0		ns

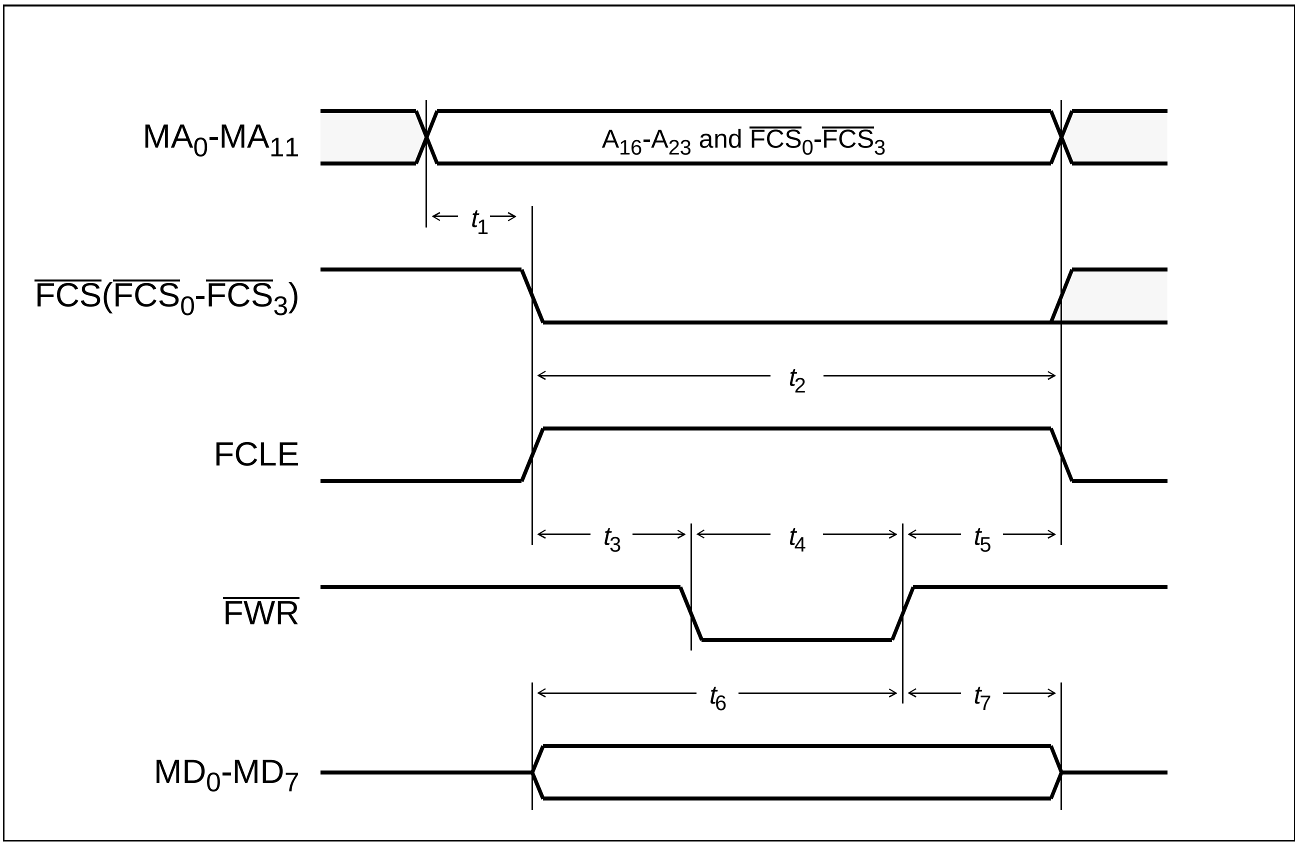


Figure 66 Memory Interface - Samsung Command Write

Parameter Memory Interface - Samsung Command Write	Symbol	Limit values		Unit
		Min	Max	
Address setup before $\overline{FCS}$, FCLE	t_1	100		ns
$\overline{FCS}$ low time, FCLE high time	t_2	400		ns
$\overline{FWR}$ hold after FCLE rising	t_3	100		ns
$\overline{FWR}$ low time	t_4	200		ns
$\overline{FWR}$ setup before FCLE falling	t_5	100		ns
Data setup time	t_6	200		ns
Data hold time	t_7	50		ns

Note: $\overline{FCS}$ stays low if other cycles follow for the same access.

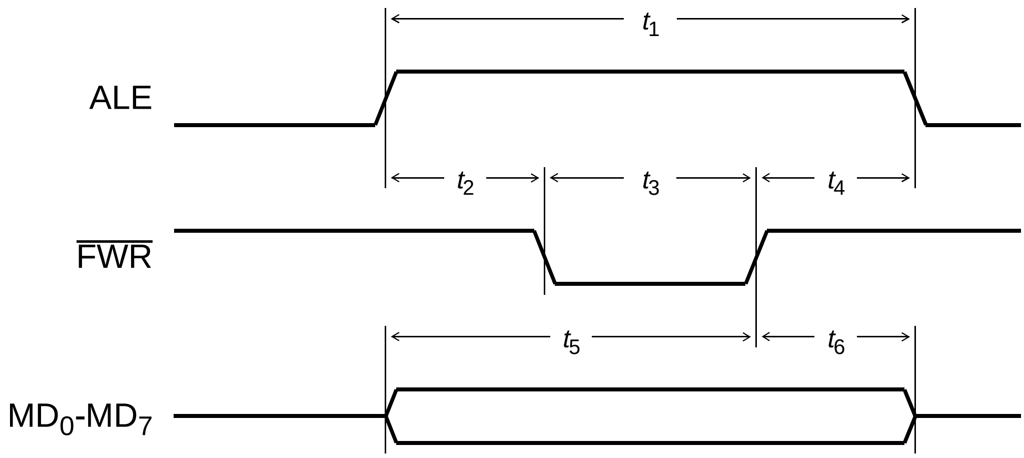


Figure 67 Memory Interface - Samsung Address Write

Parameter Memory Interface - Samsung Address Write	Symbol	Limit values		Unit
		Min	Max	
ALE high time	t_1	400		ns
$\overline{\text{FWR}}$ hold after ALE rising	t_2	100		ns
$\overline{\text{FWR}}$ low time	t_3	200		ns
$\overline{\text{FWR}}$ setup before ALE falling	t_4	100		ns
Data setup time	t_5	200		ns
Data hold time	t_6	50		ns

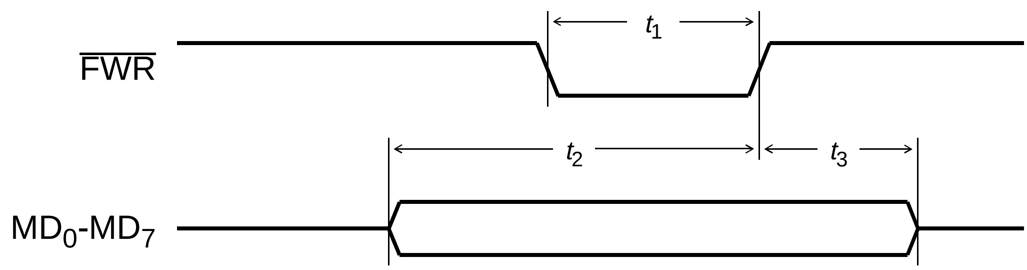


Figure 68 Memory Interface - Samsung Data Write

Parameter Memory Interface - Samsung Data Write	Symbol	Limit values		Unit
		Min	Max	
$\overline{FWR}$ low time	t_1	200		ns
Data setup time	t_2	200		ns
Data hold time	t_3	50		ns

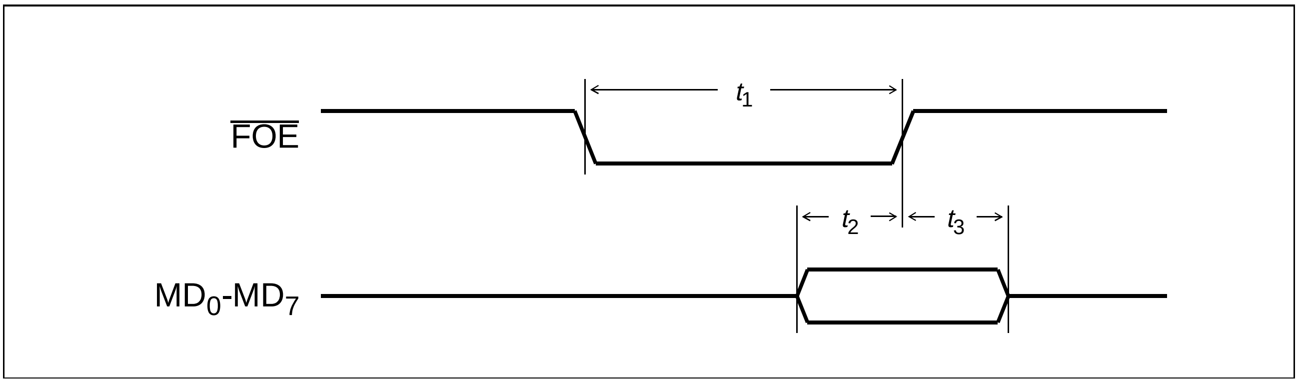


Figure 69 Memory Interface - Samsung Data Read

Parameter Memory Interface - Samsung Data Read	Symbol	Limit values		Unit
		Min	Max	
$\overline{\text{FOE}}$ low time	t_1	200		ns
Data setup time	t_2	40		ns
Data hold time	t_3	0		ns

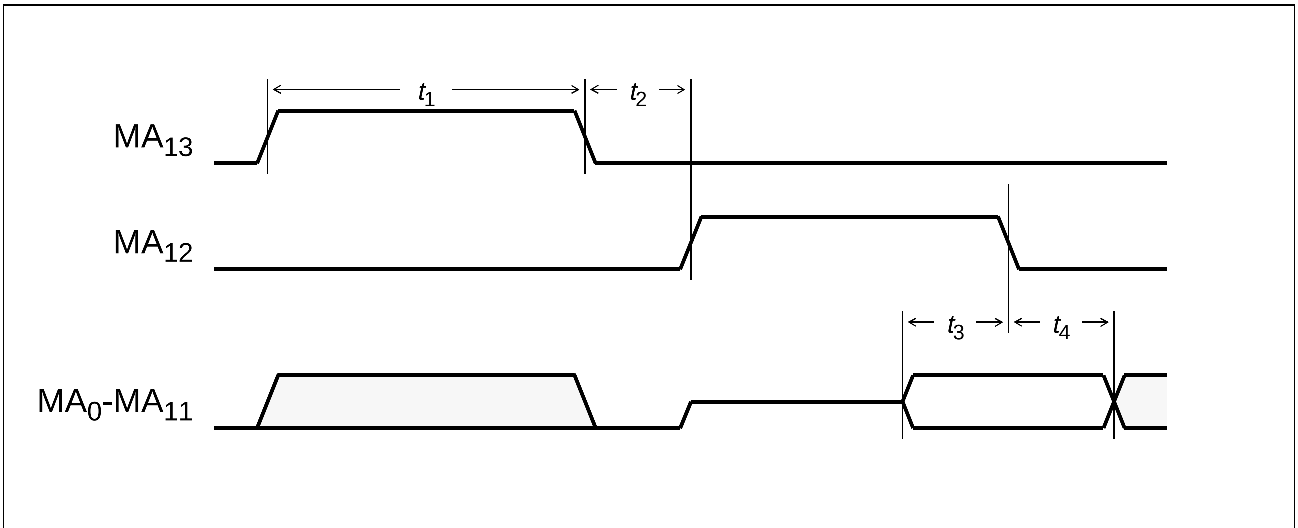


Figure 70 Auxiliary Parallel Port - Multiplex Mode

Parameter **Auxiliary Port Interface - Multiplex Mode**	**Symbol**	**Limit values**			**Unit**
		Min	**Typ**	**Max**	
Active time (MA_0-MA_{15})	t_1		2		ms
Gap time (MA_0-MA_{15})	t_2		125		µs
Data setup time	t_3	50			ns
Data hold time	t_4	0			ns

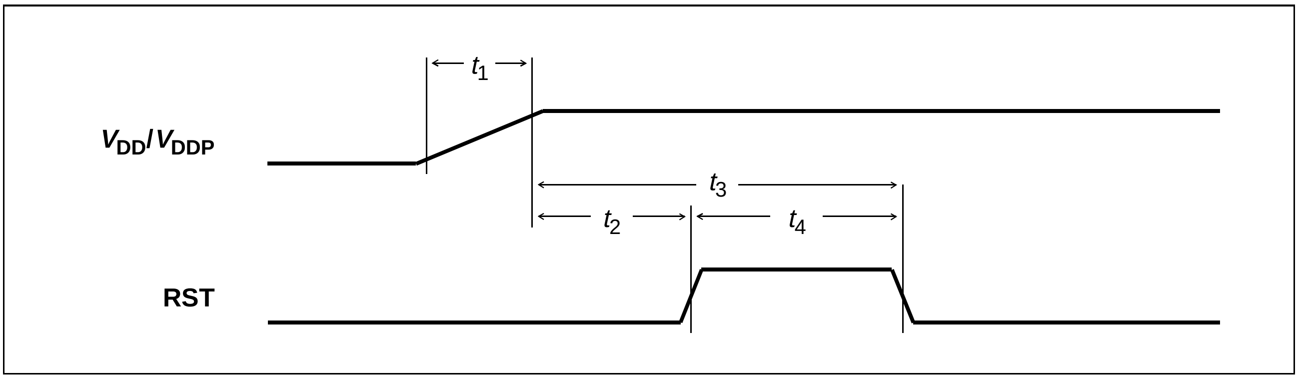
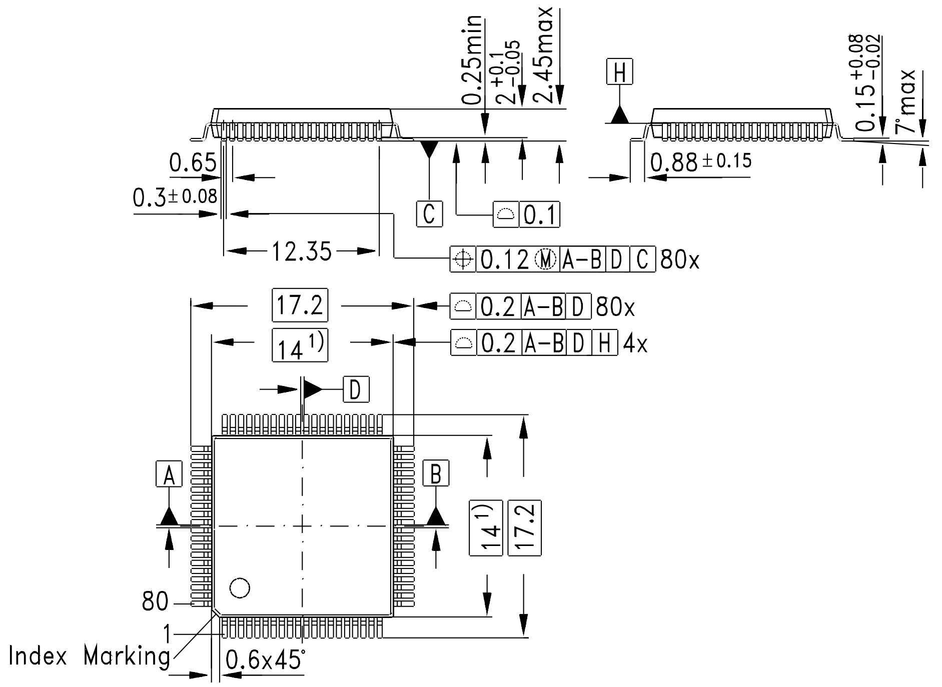


Figure 71 Reset Timing

Parameter **Reset Timing**	**Symbol**	**Limit values**		**Unit**
		Min	**Max**	
$V_{DD}/V_{DDP}/V_{DDA}$ rise time 5%-95%	t_1		20	ms
Supply voltages stable to RST high	t_2	0		ns
Supply voltages stable to RST low	t_3	0.1		ms
RST high time	t_4	1000		ns

5 Package Outlines

Plastic Package, P-MQFP-80 (SMD)
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

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