SIEMENS

ICs for Communications

Audio Ringing Codec Filter
Basic Function
ARCOFI®-BA

PSB 2161 Version 1.1

User's Manual 11.97

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1 Overview

The PSB 2161 ARCOFI-BA provides the design engineer with a cost-optimized **A**udio, **R**inging, **Co**dec, **Fi**lter processor solution for simple digital terminals. It offers the minimum functions necessary to develop a low-cost telephone with the high flexibility by the DSP technics.

Remark: For more sophisticated digital terminals (e.g. comfort telephones offering speakerphone, voice/data terminals) we recommend the use of the Siemens ARCOFI-SP PSB 2163.

The typical applications of the ARCOFI-BA are:

- low-cost digital telephone
- low-cost facsimile terminal
- low-cost answering machine

Note: Throughout this whole document "ARCOFI" refers to ARCOFI-BA PSB 2161.

The ARCOFI performs all encoding, decoding and filtering functions according to the ITU-T and ETSI (NET33) norms.

Full featured applications are possible without any external elements. All the necessary hardware and software is implemented.

Two transducer correction filters (one for each direction) can be programmed for an optimum adaptation to different transducer frequency characteristics.

The ARCOFI provides a universal tone generator for automatic generation of multitone sequences which can be used for tone alerting, call progress tones or other audible feedback tones.

A DTMF generator for the transmit direction is also available. This flexible tone generator concept fulfills a wide range of applications.

The interfacing to a handset mouth and earpiece is facilitated by a flexible analog front end. A loudspeaker output has also been integrated on the chip as well as a secondary input for a handsfree microphone. All analog inputs and outputs are gain programmable through software.

At the digital side an ISDN-Oriented Modular (IOM-2) interface for terminal (TE) and non-terminal (NON-TE) applications or a Serial Control/Data Interface (SCI & SDI) is realized to connect layer-1/2 devices to the ARCOFI.

The ARCOFI is a BICMOS-device, available in a P-DSO-28-1 package. It operates from a single + 5 V supply and features a power-down state with very low power consumption.

1.1 Comparison between PSB 2161 and PSB 2160

Table of main differences:

PSB 2161	PSB 2160	Comment
0.8 µ BICMOS technology	2 µ CMOS technology	
P-DSO-28-1	P-DIP-24 and P-LCC-28	
Single + 5 V supply Reduced power consumption in power down and operating modes	± 5 V supply	
IOM-2 NON-TE Interface; Serial Control/Data Interface Flexible configuration concept Buffered Dual Port Coefficient-RAM (reprogramming of the Coefficient-RAM in operating modes without acoustical effects)	SLD Interface	
Separate digital output for a piezo ringer	Multiplexed digital output for a piezo ringer	
Fully programmable, high performance AFE in BICMOS technology	Partial programmable Analog Front End (AFE)	
Ringing directly via loudspeaker (simultaneously signalling over the loudspeaker and voice over the earpiece is possible)	Ringing via loudspeaker only over the common receiver path (simultaneously signaling over the loudspeaker and voice over the earpiece is not possible)	
Sidetone gain stage with higher resolution (two byte coefficient)	Sidetone gain stage with low resolution (one byte coefficient)	
Extended tone generation unit for receive and transmit direction	Simple tone generation unit for the receive direction and a DTMF generator for the transmit direction	
Digital high pass in receive direction Monitoring mode for digital and analog voice recording Additional test loops		
ETSI (NET33) & ITU-T G.712	ITU-T G.712	

Note: Many slightly improvements realized in the PSB 2161 are not documented in this table.

1.2 Table of Symbols

AD	Address of the ARCOFI (IOM-2 mode)
A/D	Analog to Digital converter
ADI	ARCOFI Digital Interface
AFE	Analog Front End
AHO	Handset Output Amplifier
AIMX	Analog Input Multiplexer control bits (ATCR)
ALC	Analog Loop via Converter (TFCR)
ALF	Analog Loop via Front End (TFCR)
ALI	Analog Loop via Interface (TFCR)
ALN	Analog Loop via Noise Shaper (TFCR)
ALS	Loudspeaker Amplifier
ALTF	Analog Loop & Test Function bits (TFCR)
ALZ	Analog Loop via Z-side tone gain stage
AMI	Microphone Amplifier
ARCOFI	Audio Ringing Codec Filter
ASP	ARCOFI Signal Processor
AXI	Auxiliary Input
BM	Beat Mode bit (TGCR)
BT	Beat Tone bit (TGCR)
CAM	Chip Address Mode bit (IOM-2 two chip mode; GCR)
CCITT	International Telegraph and Telephone Consultative Committee
CG	Control Generator bit (TGCR)
CMDR	Command Register
COP	Coefficient Operation (CMDR)
CR	Configuration Register
CRAM	Coefficient RAM
$\overline{CS}$	Chip Select active low (serial control interface)
D/A	Digital to Analog converter
DCE	Double Clock Enable at DCLK pin (SDICR)
DCL	IOM-2 interface clock
DCLK	Data Clock pin (serial data interface)
DD	IOM-2 Data Downstream pin
DEC	Decimation filter
DHON	Disable pin HON (XCR)
DHOP	Disable pin HOP (XCR)
DHPR	Disable High Pass Receive bit (PFCR)
DHPX	Disable High Pass Transmit bit (PFCR)
DLN	Digital Loop via Noise Shaper (TFCR)
DLP	Digital Loop via PCM-register (TFCR)

Table of Symbols (cont'd)

DLS	Digital Loop via Signal processor (TFCR)
DLSN	Disable pin LSN (XCR)
DLSP	Disable pin LSP (XCR)
DLTF	Digital Loop and Test Function bits (TFCR)
DR	Data Receive pin (serial data interface)
DRAM	Data RAM
DSP	Digital Signal Processor
DT	Dual Tone bit (TGCR)
DTMF	Dual Tone Multi Frequency bit (TGSR)
DU	IOM-2 Data Upstream pin
DX	Data Transmit pin (serial data interface)
EP	Earpiece
EPP0	Enable Push-Pull at pin DU/DX (SDICR)
EPP1	Enable Push-Pull at pin SA/SDX (SDICR)
ETF	Enable Tone Filter bit (TGCR)
ETSI	European Telecommunications Standards Institute
EVX	Enable Voice Transmit bit (GCR)
EVREF	Enable VREF buffer bit (ATCR)
EWDF	Electrical Wave Digital Filter
FR	Frequency correction Receive bit (PFCR)
FSC	IOM-2 and SDI-Frame Synchronization pin (8 kHz)
FX	Frequency correction Transmit bit (PFCR)
GR	Receive Gain bit (PFCR); Receive gain stage
GX	Transmit Gain bit (PFCR); Transmit gain stage
GZ	Z-side tone Gain bit (PFCR); Z-side tone Gain stage
HO	Handset Output
HOC	Handset Output Control bits (ARCR)
HON	Handset earpiece Output – pin
HOP	Handset earpiece Output + pin
HPR	High-pass filter receive
HPX	High-pass filter transmit
IDENT	Identification Code
IDR	Initialize Data RAM (TFCR)
INT	Interpolation filter
IOM	ISDN-Oriented Modular
ISDN	Integrated Services Digital Network
ITU-T	International Telecommunication Union -Telephone

Table of Symbols (cont'd)

LAW	A-Law/µ-Law bit (GCR)
LIN	Linear data mode (VDM; DFICR)
LS	Loudspeaker
LSC	Loudspeaker Control bits (ARCR)
LSN	Loudspeaker output – pin
LSP	Loudspeaker output + pin
MCLK	Master Clock pin (synchronized system clock)
MCLKR	Master Clock Rate (SDICR)
MIC	Microphone Control bits (ATCR)
MIN1/2	Microphone inputs – pins
MIP1/2	Microphone inputs + pins
NOP	No Operation (CMDR)
NOT	No Test mode (TFCR)
PABX	Private Automatic Branch Exchange
PCI	Peripheral Control Interface
PCM	Pulse Code Modulation
PM	Piezo Mode; output to digital pins PZ1/PZ2 (TGSR)
POR	Power-On Reset
PU	Power-Up bit (GCR)
RCM	Reverse Channel Mode (CMDR)
RS	Reset pin
R/W	Read/Write operation bit (CMDR)
RX	Receive path
SA-SD	PCI I/O pins; I/O control bits (SDICR)
SCI	Serial Control Interface
SCLK	Serial Clock pin (serial control interface)
SDI	Serial Data Interface
SDR	Serial Data Receive pin (serial control interface)
SDX	Serial Data Transmit pin (serial control interface)
SLOT	IOM-2 Slot select for TE mode (GCR)
SM	Stop Mode bit (TGCR)
SOP	Status Operation (CMDR)
SQTR	Square/Trapezoid mode bit (TGCR)
S/T	Square/Trapezoid Generator

Table of Symbols (cont'd)

TE	Terminal Equipment
TG	Tone Generator bit (TGCR)
TR	Three party conferencing (VDM; DFICR)
TRL	Tone Ringing via Loudspeaker (TGSR)
TRR	Tone Ringing Receive bit (TGSR)
TRX	Tone Ringing Transmit bit (TGSR)
TS	Time-Slot Selection in SDI-mode (TSCR)
TX	Transmit path
V_{DD}	Voltage supply (+ 5 V)
V_{DDP}	Analog Voltage supply for Power amplifiers (+ 5 V)
VDM	Voice Data Manipulation bits (DFICR)
V_{REF}	Reference Voltage output pin
V_{SSA}	Analog ground (0 V)
V_{SSD}	Digital ground (0 V)
V_{SSP}	Analog ground for Power amplifiers (0 V)
WDF	Wave Digital Filter
XOP	Extended Operation (CMDR)

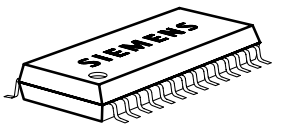
Audio Ringing Codec Filter Basic Function ARCOFI-BA

PSB 2161

Version 1.1

BICMOS

1.3 Features



P-DSO-28-1

- Applications in digital terminal equipment featuring voice functions
- Digital signal processing performs all CODEC functions
- Fully compatible to the ITU-T G. 712 and ETSI (NET33) specification
- PCM A-Law/µ-Law (G. 711 ITU-T) and 16-bit linear data
- Flexible configuration of all internal functions
- IOM-2 interface (TE and NON-TE mode), Serial Control Interface (SCI) and Serial Data Interface (SDI)
- Three analog inputs: two differential, high performance inputs for microphones and a single-ended auxiliary input
- Two differential outputs for a handset earpiece (200 Ω) and a loudspeaker (50 Ω)
- 100 mW sine wave and 200 mW square wave loudspeaker driver capability
- Separate digital output for a piezo ringer
- Flexible Peripheral Control Interface (PCI) in IOM-2 TE mode
- Flexible test and maintenance loopbacks in the analog front end and the digital signal processor
- Independent gain programmable amplifiers for all analog inputs and outputs
- Buffered Dual Port Coefficient-RAM (reprogramming of the Coefficient-RAM in operating modes without acoustical effects)
- Two transducer correction filters
- Side tone gain adjustment
- Flexible DTMF, tone and ringing generator
- Single 5 V power supply
- Low power consumption: standby < 1 mW, operating consumption is dependent on the selected operating mode
- Advanced 0.8 µ BICMOS technology

Type	Ordering Code	Package
PSB 2161	Q67101-H6763	P-DSO-28-1

1.4 Pin Configurations

P-DSO-28-1

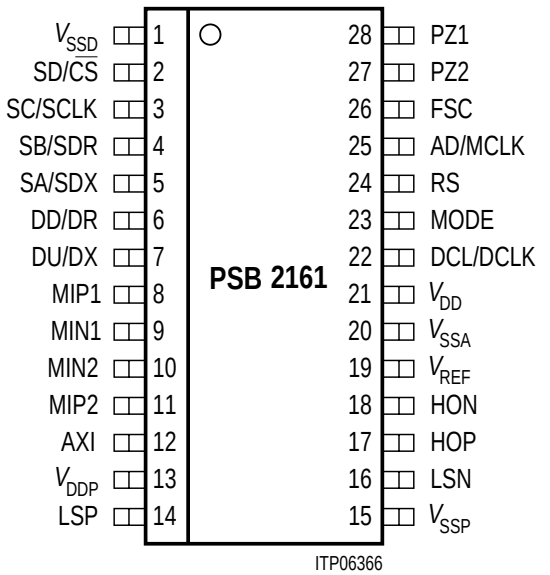


Figure 1

1.5 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O) Open Drain (OD)	Function
21	V_{DD}	–	Power supply (5 V ± 5 %)
13	V_{DDP}	–	Power supply (5 V ± 5 %)
1	V_{SSD}	–	Digital Ground (0 V)
20	V_{SSA}	–	Analog Ground (0 V)
15	V_{SSP}	–	Analog Ground (0 V)
23	MODE	I	**Mode Selection:** IOM-2 or serial control/data interface
25	AD	I	**IOM® Address:** Chip address in IOM-2 two chip mode
	MCLK	I	**Master Clock:** Synchronous system clock when serial control/data interface is selected
24	RS	I	**Reset:** A high signal on this pin forces the ARCOFI into reset state
26	FSC	I	**Frame Sync:** 8-kHz frame synchronization signal (IOM-2 and SDI mode)
22	DCL	I	**DCL-System Clock:** 1.536 MHz supplied by the application system clock when IOM-2 mode is selected
	DCLK	I	**DCLK Data Clock:** Data clock of the serial data interface (SDI)
6	DD	I/(OD) [1]	**Data Downstream:** Receive data from layer-1 IOM-2 controlling device
	DR	I	**Data Receive:** Receive data of the serial data interface (SDI)
28 27	PZ1 PZ2	O O	**Digital Piezo Ringer Output:** When selected the tone ringer is routed to this output (PZ1 & PZ2 are in opposite phases)

[1] See DD/DU-voice channel swapping (XOP_D)

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O) Open Drain (OD)	Function
7	DU	OD/I [1]	**Data Upstream:** Transmit data to the layer-1 IOM-2 controlling device
	DX	OD/O [2]	**Data Transmit:** Transmit data of the serial data interface (SDI)
2	SD	IO	**Programmable I/O PCI Pin SD:** This port pin is only available in IOM-2 TE mode
	$\overline{CS}$	I	**Chip Select:** A low level indicates a microprocessor access to the serial control interface (SCI)
3	SC	IO	**Programmable I/O PCI Pin SC:** This port pin is only available in IOM-2 TE mode
	SCLK	I	**Serial Clock:** Clock signal of the serial control interface (SCI)
4	SB	IO	**Programmable I/O PCI Pin SB:** This port pin is only available in IOM-2 TE mode
	SDR	I	**Serial Data Receive:** Receive data line of the serial control interface (SCI)
5	SA	IO	**Programmable I/O PCI Pin SA:** This port pin is only available in IOM-2 TE mode
	SDX	OD/O [3]	**Serial Data Transmit:** Transmit data line of the serial control interface (SCI)
19	V_{REF}	O	**2.4 V Output:** Output for biasing analog single-ended inputs
8 9	MIP1 MIN1	I I	**Microphone Input 1:** This highly symmetrical differential input has been designed for commonly used telephone microphones

[1] See DD/DU voice channel swapping (XOP_D)
[2] Programmable via bit SDICR.EPP0
[3] Programmable via bit SDICR.EPP1

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O) Open Drain (OD)	Function
11 10	MIP2 MIN2	I I	**Microphone Input 2:** This highly symmetrical differential input has been designed for commonly used telephone microphones
12	AXI	I	**Auxiliary Input:** Single-ended auxiliary input
14 16	LSP LSN	O O	**Loudspeaker Output:** LSP, LSN are differential output pins which can drive a 50 Ω loudspeaker directly; a piezo transducer can also be used for ringing signal instead of the loudspeaker
17 18	HOP HON	O O	**Handset Earpiece Output:** HOP, HON are differential output pins which can drive handset earpiece transducers directly

1.6 Logic Symbol

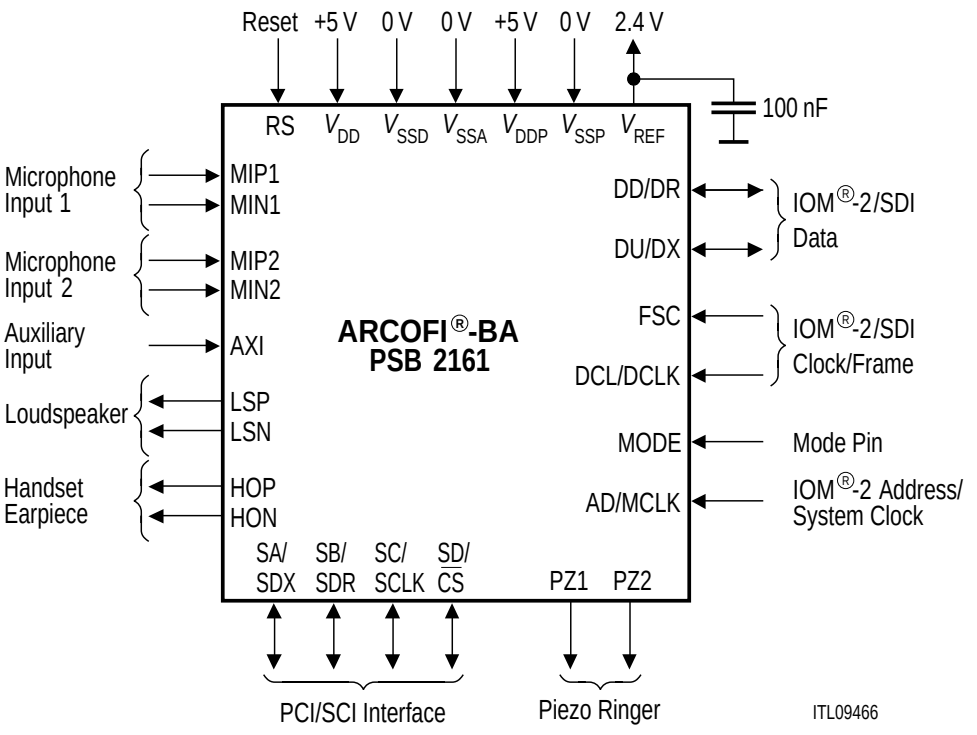


Figure 2
Logic Symbol of the ARCOFI®

1.7 Functional Block Diagram

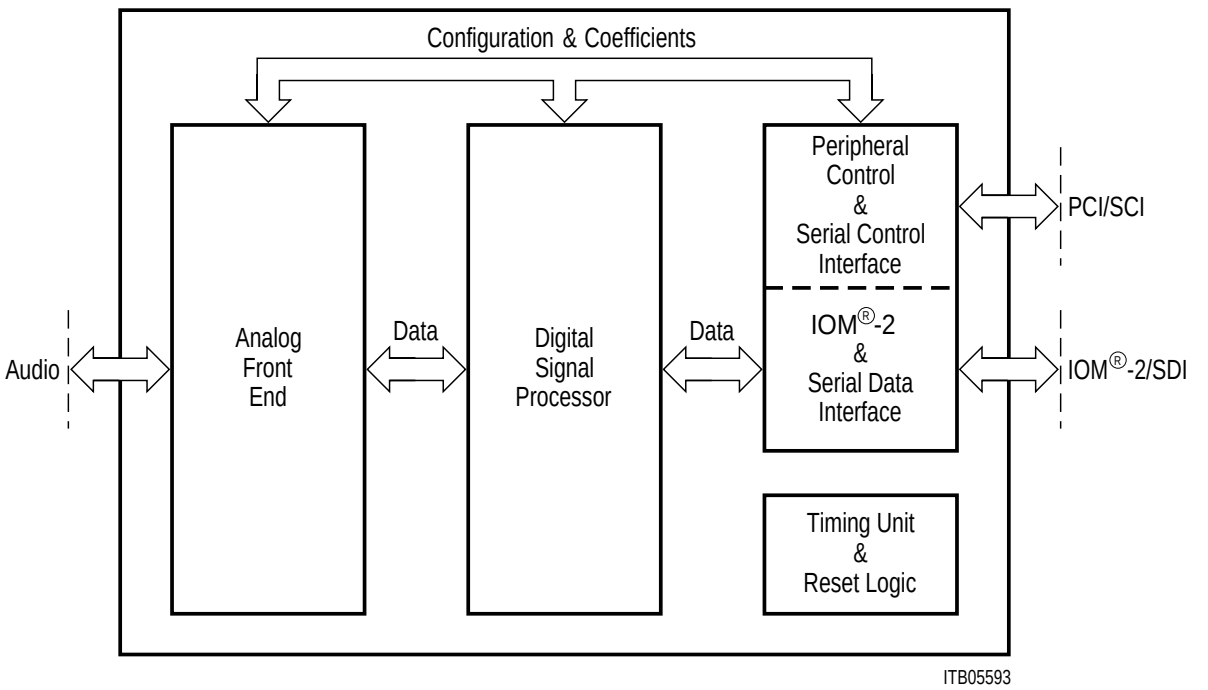


Figure 3
Block Diagram of the ARCOFI®

1.8 System Integration

The complete family of ICs for digital terminals offered by Siemens simplifies the development of these devices and gives a cost-effective solution to the design engineer. The architecture of these terminals is based on a modular interface especially conceived for ISDN and named IOM-2.

Figure 4 shows an example of an integrated multifunctional ISDN terminal using the ISAC-S TE. The ISAC-S TE (ISAC-S: ISDN S-Access controller PSB 2186) provides the S-interface and separates the B and D channels.

A voice processor is connected to the programmable digital signal processing codec filter (ARCOFI-BA) via IC1 and a data encryption module to a data device via IC2. B1 is used for voice communication and B2 for data communication.

Typical terminal applications are described in the next sections.

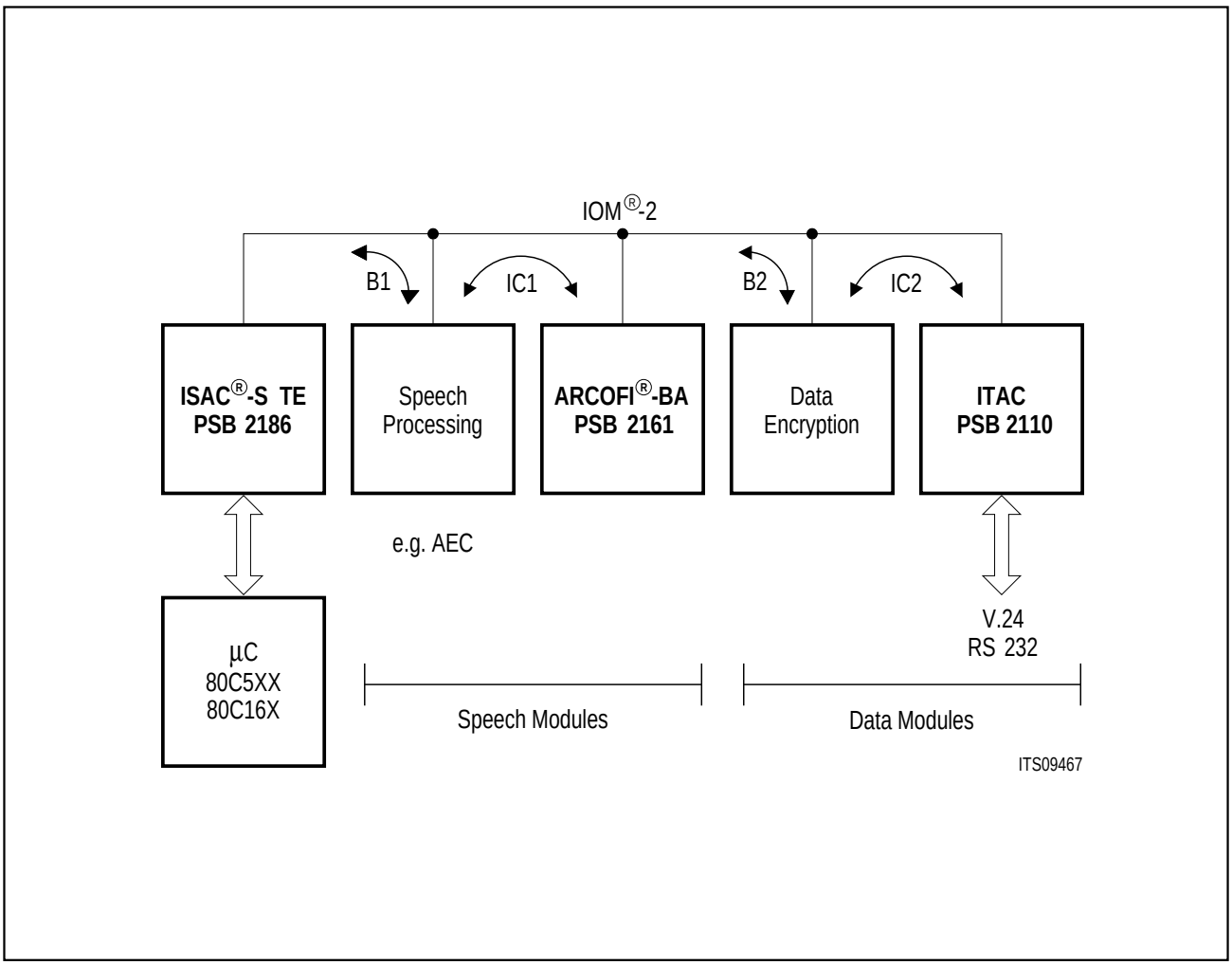


Figure 4
Example of ISDN Voice/Data Terminal

1.8.1 ISDN-Voice Terminal

Figure 5 shows a typical solution for a voice terminal for S interface.

The ARCOFI offers the functions of CODEC and filtering. It also carries out the functions of tone ringing, DTMF, and A/D and D/A conversions. The ARCOFI permits the direct connection of a handset and a loudspeaker.

The ARCOFI can be programmed and read out by the µC via the lOM-2 interface and the ISAC-S TE. The same µC supervises the keyboard functions and the function hook-ON/OFF.

The S-interface functions such as activation/deactivation, clock recovery, clock resynchronization as well as the layer-2 functions like LAPD protocol handling are executed by the ISDN Subscriber Access Controller.

A U-interface telephone can easily be derived from the voice terminal shown on **figure 5** by replacing the ISAC-S with the ISDN Communication Controller ICC PEB 2070 and the ISDN-Echo Cancellation Unit IEC-Q NTE (PSB 21910).

Figure 6 shows such a typical solution for a voice terminal with U-interface.

In both cases the whole terminal is power supplied by the ISDN DC Converter Circuit IDCC PEB 2023.

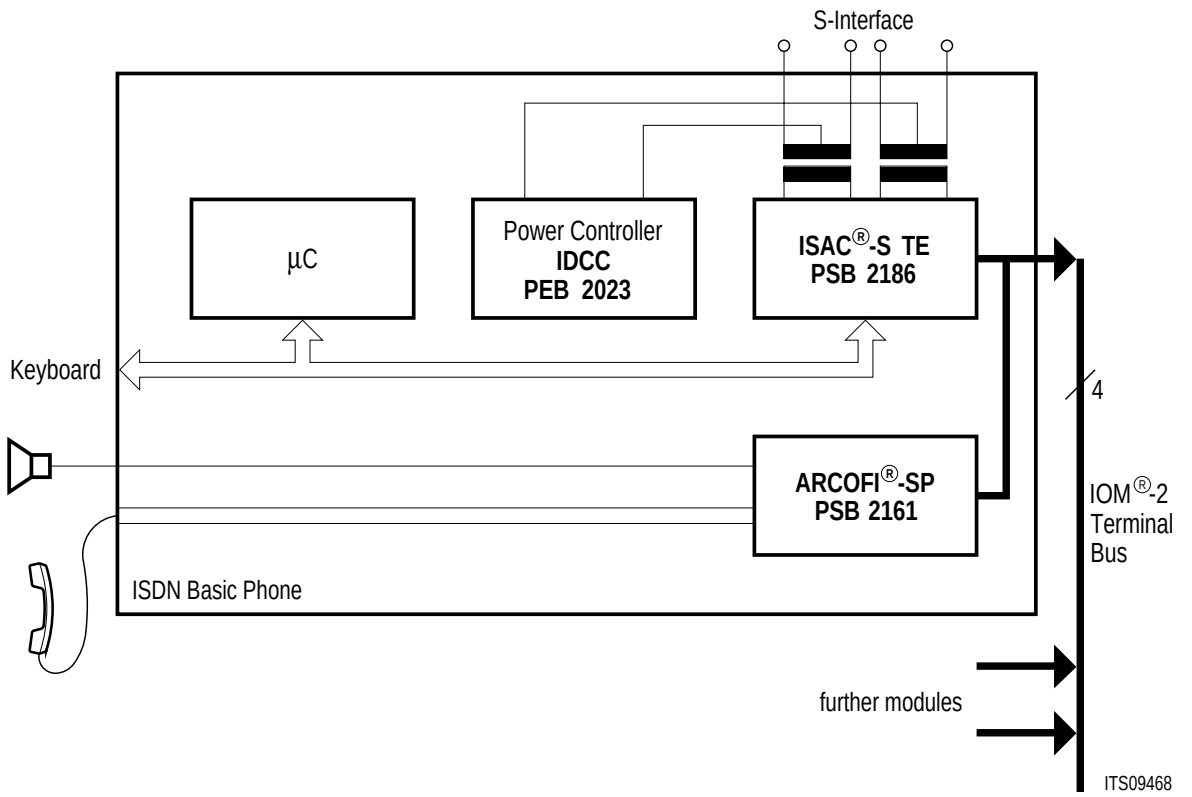


Figure 5
Basic ISDN S-Voice Terminal

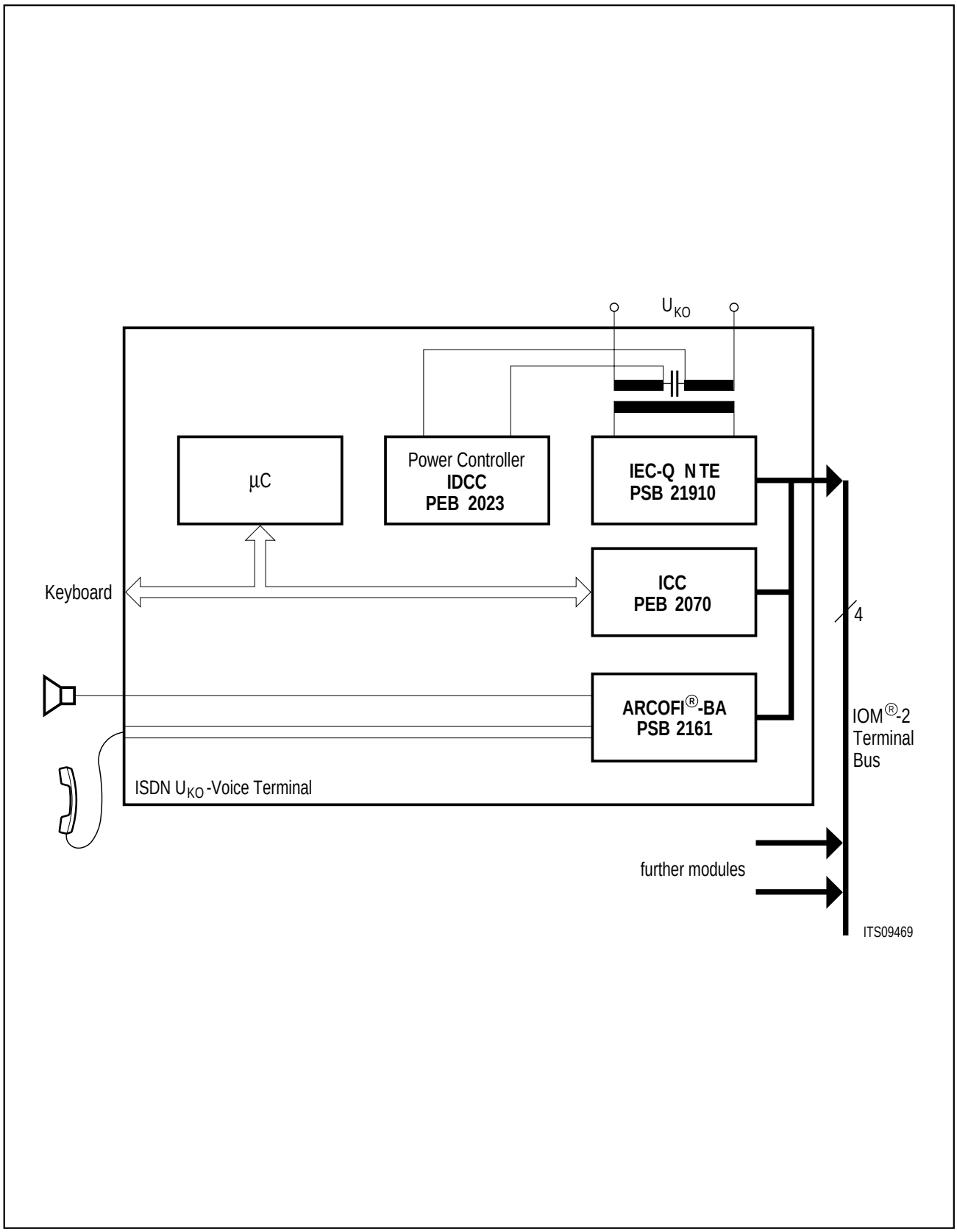


Figure 6
Basic ISDN U-Voice Terminal

1.8.2 Digital PABX Voice Terminal

The Serial Control Interface allows the ARCOFI to be programmed directly from a serial port of a microcontroller.

The voice data may be transmitted via the IOM-2 interface or on a PCM interface provided from other transceiver devices. If the Serial Data Interface (SDI) is selected the PCM data rate can vary from 64 kbit/s up to 4096 kbit/s.

Figure 7 shows a PABX voice terminal using the ISAC-P TE PSB 2196 together with a microcontroller. **Figure 8** shows a PABX-voice terminal using a transceiver device without IOM-2 interface.

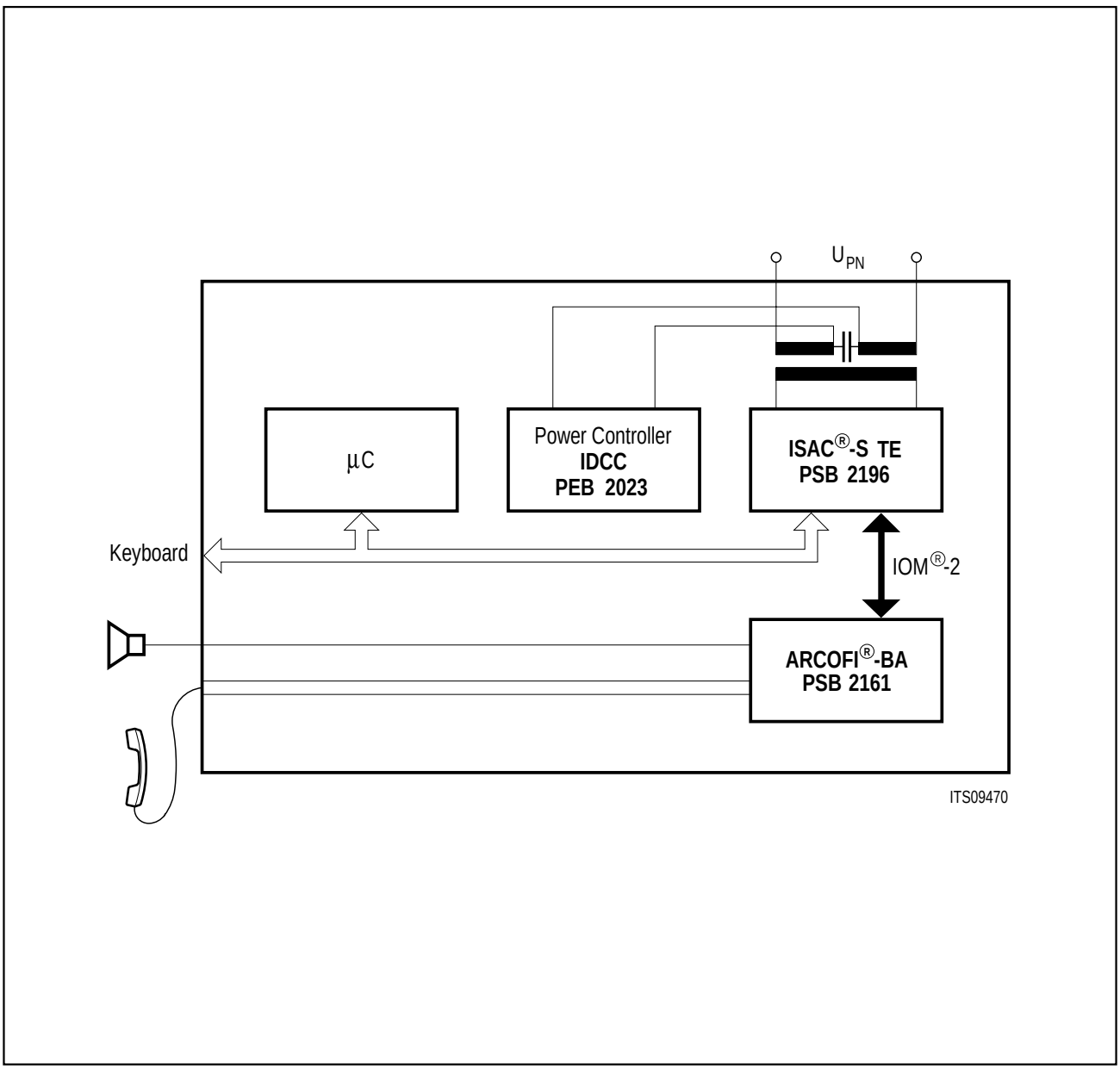


Figure 7
U_{PN} PABX Voice Terminal

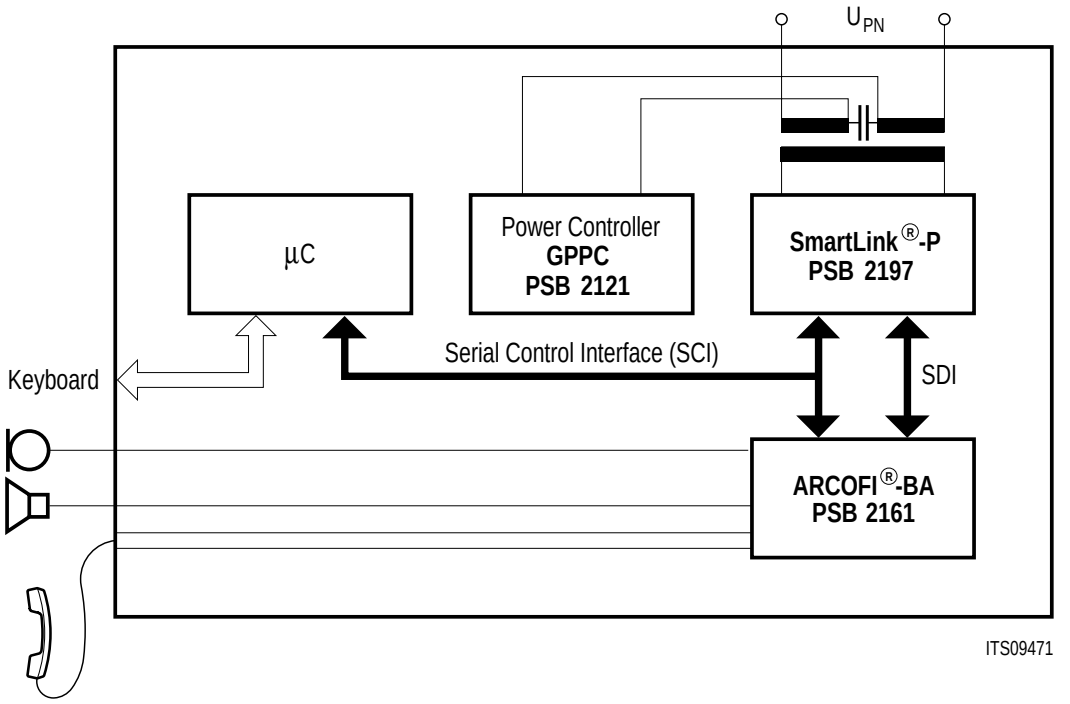


Figure 8
PABX Voice Terminal in NON-IOM®-2 Architecture

1.8.3 Terminal Adapter for Analog Telephones

Figure 9 shows how to implement a terminal adapter (tip/ring) connecting analog telephones to the ISDN world. A SLIC can be connected to the ARCOFI.

The tip and ring information is transmitted transparently through the ARCOFI via the C/I-channel of the IOM channel 1 through the ISAC-S TE to the µC.

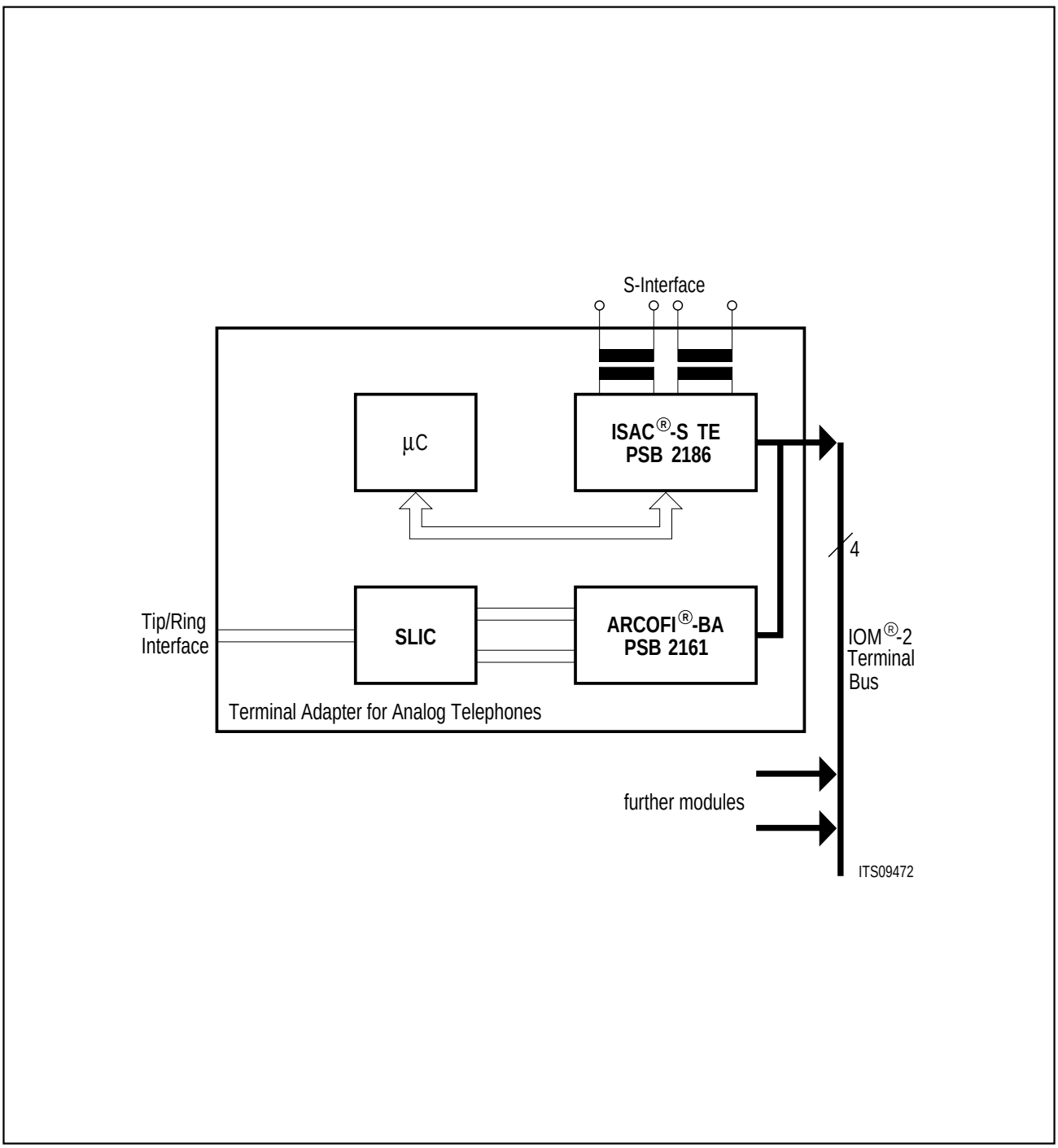


Figure 9
Terminal Adapter Tip/Ring for Analog Telephones

1.8.4 Voice/Data Terminal (PC-Card)

Figure 10 shows a voice/data terminal developed on a PC-card. The HSCX-TE (PSB 21525) offers a low cost data interface (e.g. X.25) from the host to the ISDN world via the IOM-2 interface.

The card is powered by the PC, and thus no power controller is necessary.

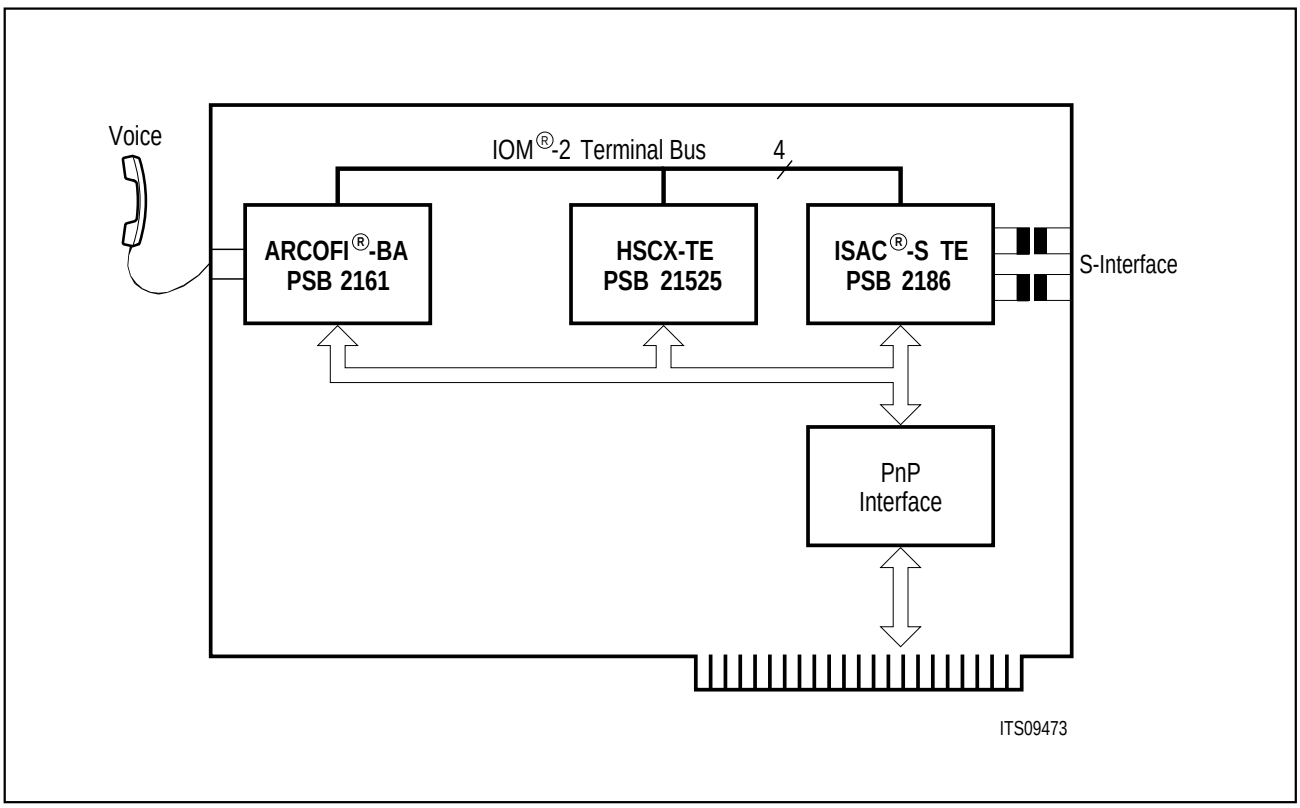


Figure 10
PC-Card as an ISDN Voice/Data Terminal

1.8.5 Multifunctional ISDN Terminal

Figure 11 gives an example of a multifunctional terminal. The HSCX-TE PSB 21525 (High-Level Serial Communications Controller Extended for Terminal Applications) simplifies the realization of an intelligent X.25 terminal adapter module whereas the ITAC PSB 2110 offers X.21, V.24, V.110 or V.120 interfaces for non ISDN terminals.

The µC connected to the ISAC-S TE PSB 2186 is the system master. The two other µCs are the slaves. When a slave µC wants access to the µC bus, it informs the master via the C/I-channel of IOM-2 channel 1.

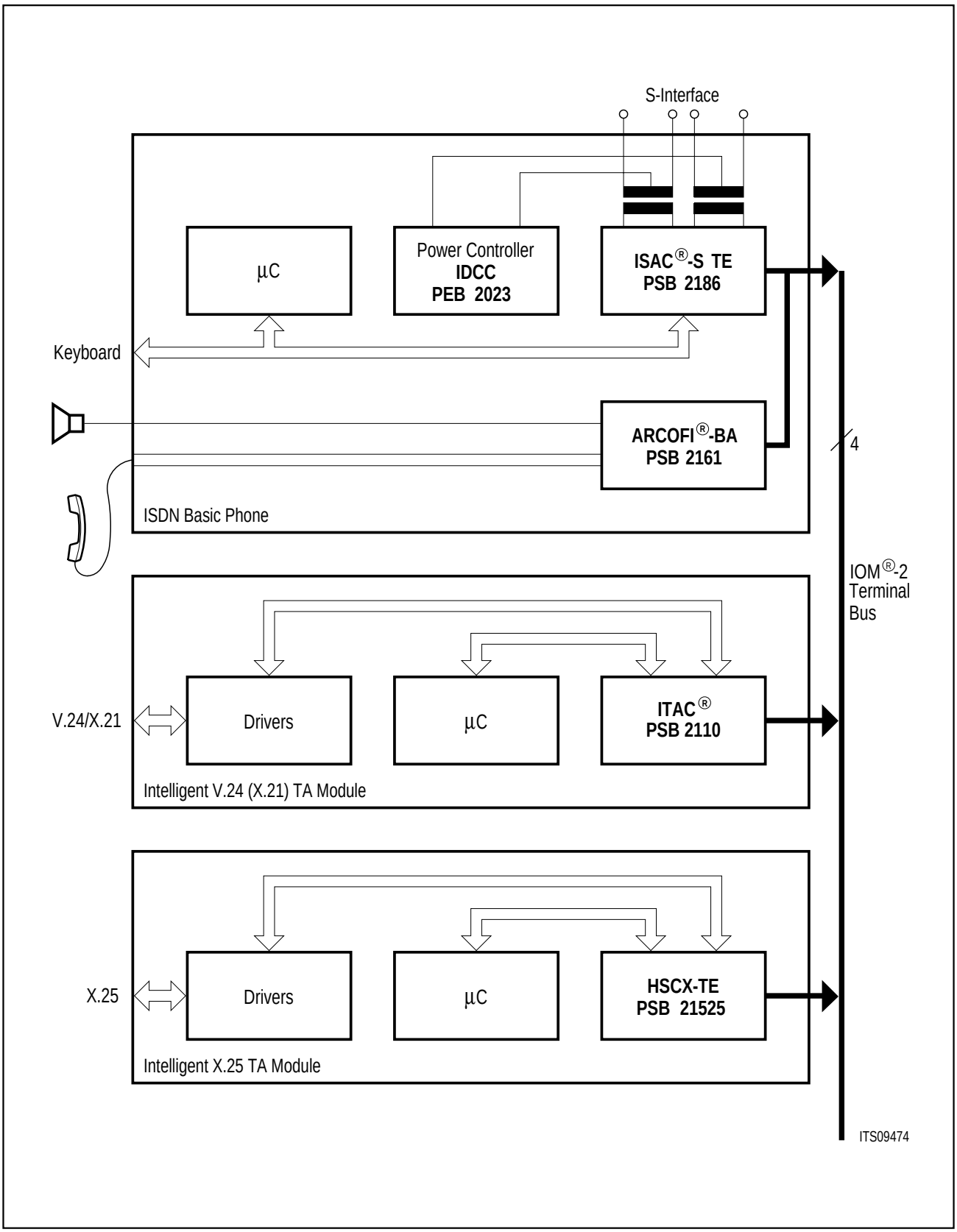


Figure 11
Multifunctional ISDN Terminal

1.8.6 IOM®-2 Line Card Application

Some applications require the ARCOFI to connect directly to the IOM-2 interface of a line card. The lOM channel is selected via pin-strapping. The ARCOFI is programmed via the MONITOR channel of the selected lOM channel. Up to two ARCOFIs can be distinguished via AD input on the same IOM channel.

This configuration allows control of up to 16 ARCOFIs at one IOM-2 interface of a line card controller.

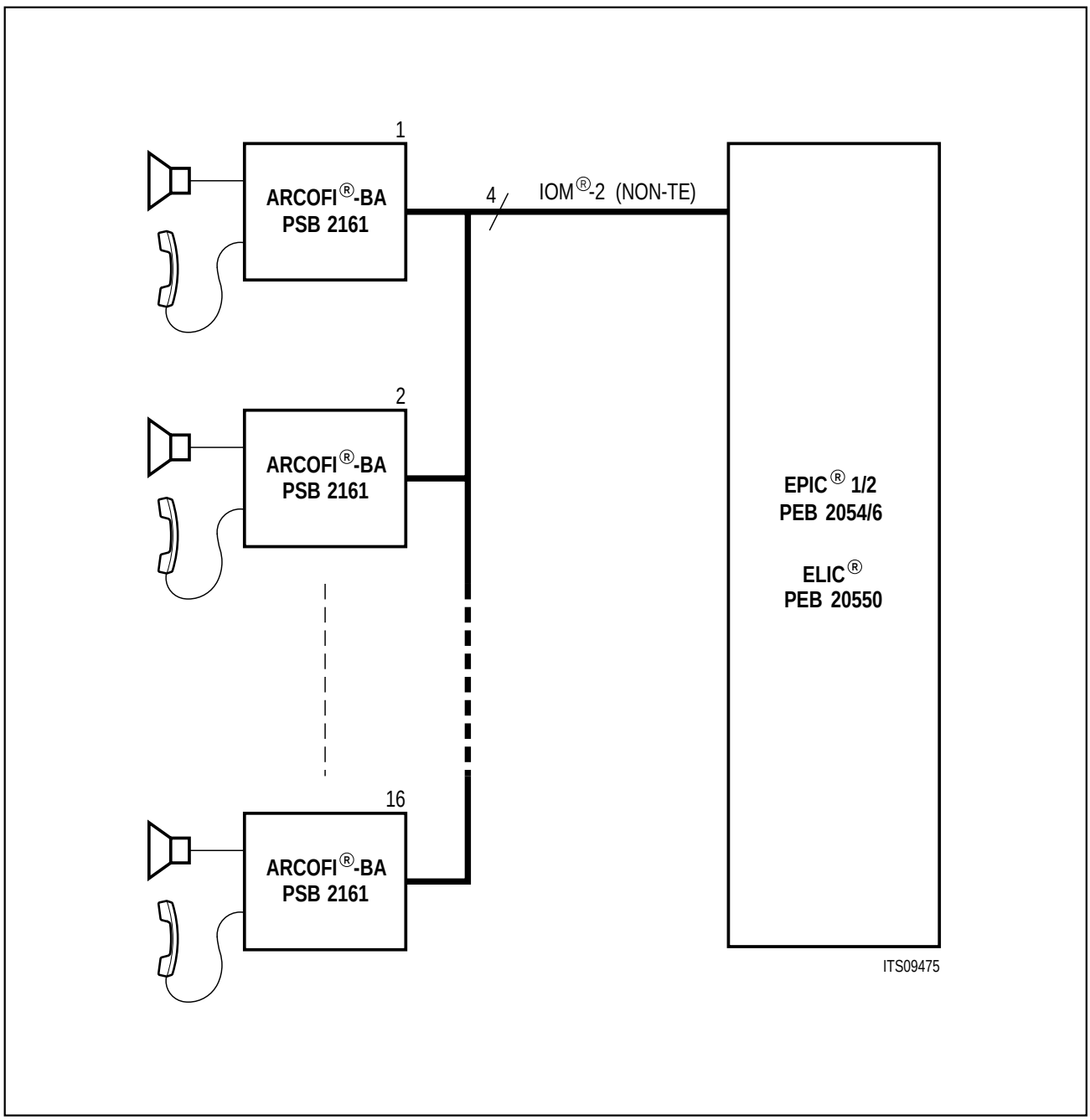


Figure 12
ARCOFI® Line Card Application

1.8.7 Group 3 Fax/Modem Adapter

The ARCOFI can be connected to a standard fax or modem chip set designed for analog networks. The ARCOFI converts the analog signal to PCM data which are transmitted over the digital network.

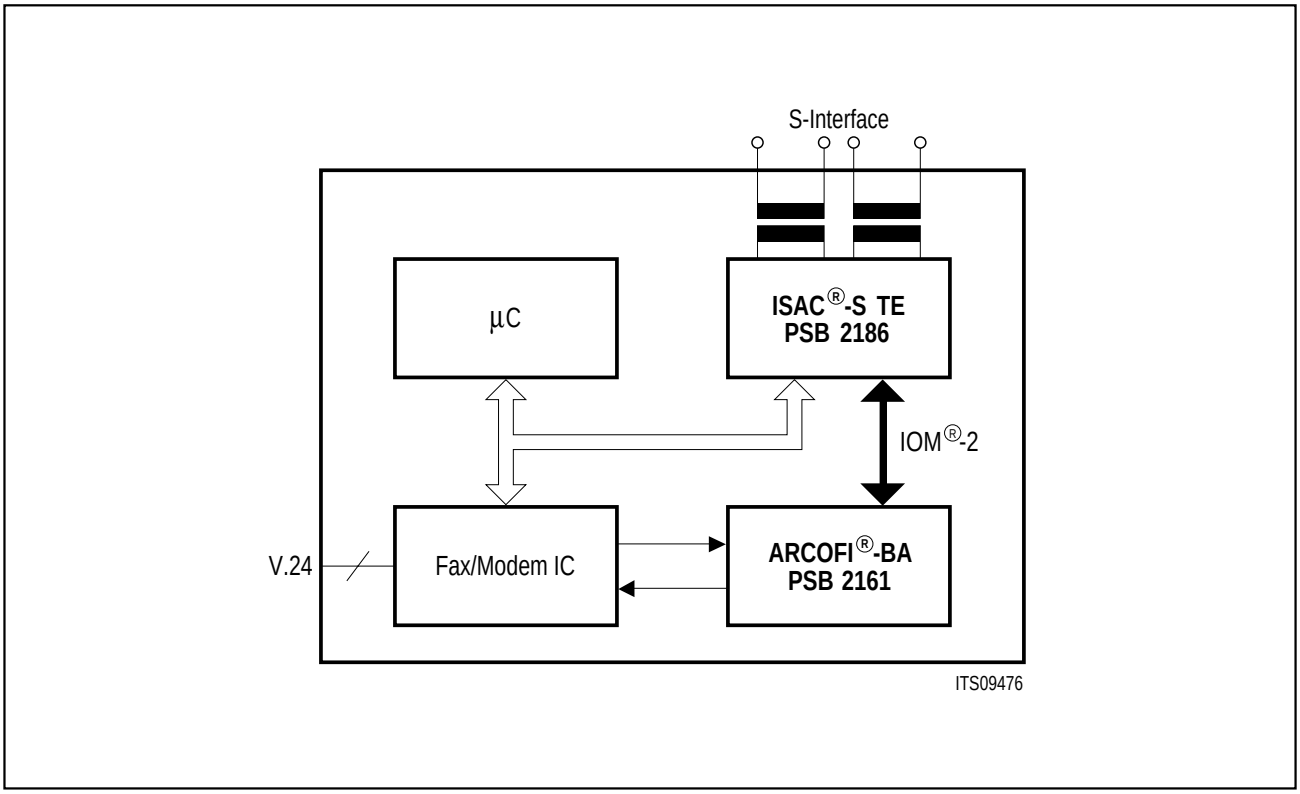


Figure 13
Group 3 Fax/Modem Adapter

2 Functional Description

The ARCOFI bridges the gap between the audio world of microphones, earphones, loudspeakers and the PCM digital world by providing a full PCM Codec with all the necessary transmit and receive filters. A block diagram of the ARCOFI is shown in **figure 14**.

The ARCOFI can be subdivided in three main blocks:

- The ARCOFI Analog Front End (AFE)
- The ARCOFI Signal Processor (ASP)
- The ARCOFI Digital Interface (ADI)

A detailed description can be found in the following chapters.

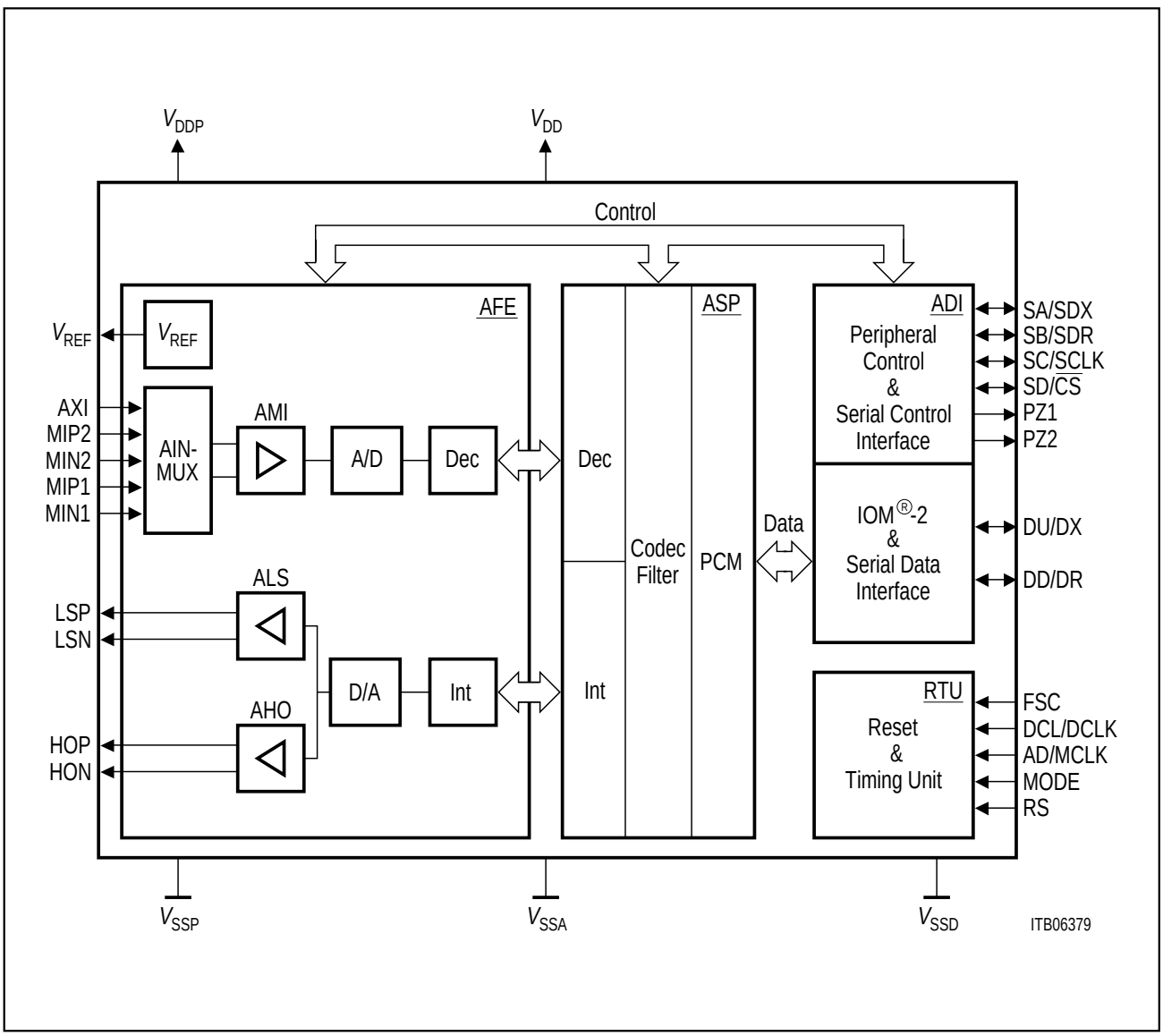


Figure 14
Architecture of the ARCOFI®

2.1 Analog Front End (AFE) Description

The Analog Front End section of the ARCOFI is the interface between the analog transducers and the digital signal processor. In the transmit direction, the AFE function is to amplify the transducer input signals (microphones) and to convert them into digital signals. In the AFE receive section, the incoming digital signal is converted to an analog signal which is output to an earpiece and/or a loudspeaker.

A block diagram of the AFE is shown in **figure 15**.

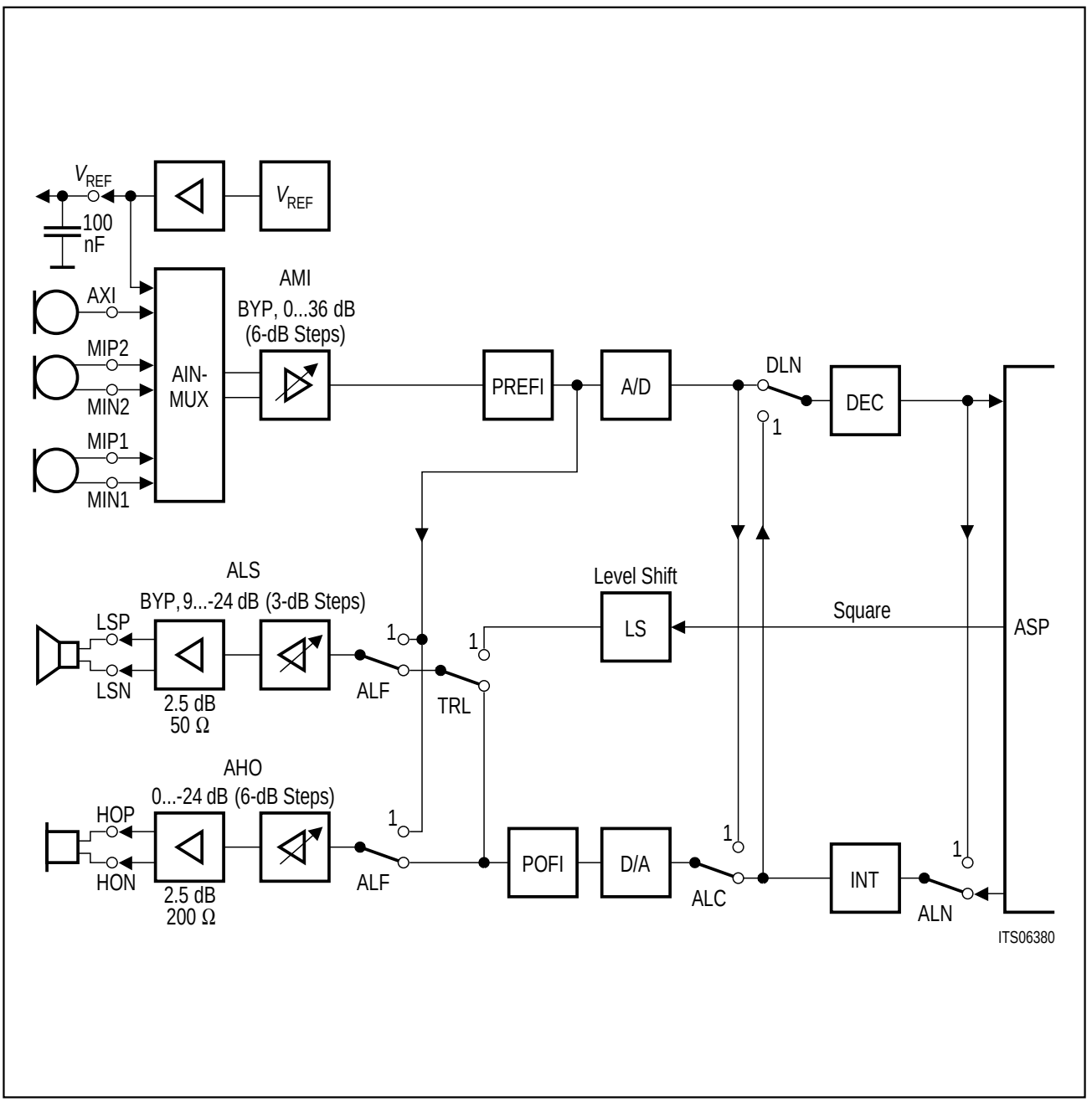


Figure 15
Signal Flow Graph of the AFE

2.1.1 Description of the Analog I/O

Two differential inputs (MIP1/MIN1 and MIP2/MIN2) and one single-ended input (AXI) are connected to the amplifier AMI via an analog input multiplexer. The programmable amplifier AMI provides a coarse gain adjustment range. Fine gain adjustment is performed in the digital domain via the programmable gain adjustment stage GX (see signal processor section). This allows a perfect level adaptation to various types of microphone transducers without loss in the signal to noise performance.

Fully differential output HOP/HON connects the amplifier AHO to a handset earpiece. Differential output LSP/LSN is provided for use with a 50 Ω loudspeaker. Up to 100 mW (sine wave) of power can be delivered to the loudspeaker via the amplifier ALS. The programmable amplifiers AHO and ALS provide a coarse gain adjustment range. Fine gain adjustment is performed in the digital domain via the programmable adjustment stage GR.

Two implemented AFE configuration registers (ATCR, ARCR) provide a high flexibility to accommodate an extensive set of user procedures and terminal attributes.

2.1.2 AFE Attenuation Plan

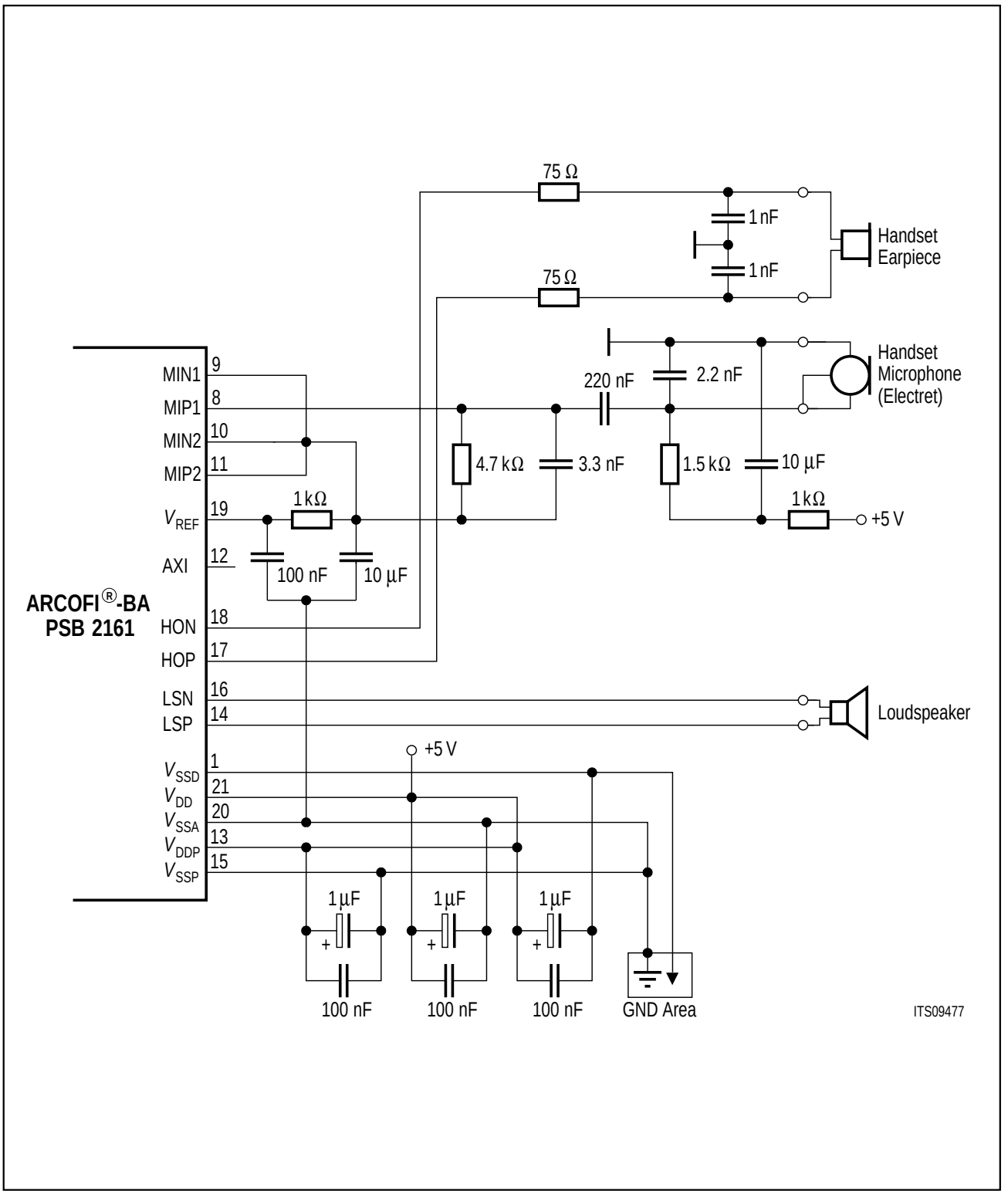
Transmit Direction

Parameter **Transmit**	**Limit Values**		**Unit**	**Reference**
	0dBm0	**max.**		
MIP1/MIN1 MIP2/MIN2 Microphone input level at max gain AMI = 36 dB	2.65E-02 1.87E-02 – 36 – 32.33	3.81E-02 2.70E-02 – 32.86 – 29.19	Vp Vrms dBm0 dBm	V V 1.18 V 0.775 V
MIP1/MIN1 MIP2/MIN2 Microphone input level at min gain AMI = 0 dB	1.67E-00 1.18E-00 0 3.67	2.40E-00 1.70E-00 3.14 6.81	Vp Vrms dBm0 dBm	V V 1.18 V 0.775 V
AXI Input level at max gain AMI = 24 dB	1.06E-01 7.46E-02 – 24 – 20.37	1.51E-01 1.07E-01 – 20.86 – 17.19	Vp Vrms dBm0 dBm	V V 1.18 V 0.775 V
AXI Input level at min gain AMI = 0 dB	8.36E-01 5.91E-01 – 6 – 2.33	1.20E-00 8.49E-01 – 2.86 0.81	Vp Vrms dBm0 dBm	V V 1.18 V 0.775 V

Receive Direction

Parameter Receive	Limit Values		Unit	Reference
	0dBm0	max.		
LSP/LSN Output level symmetrical in a 50-Ω load ALS = 2.5 dB	2.23E-00 1.58E-00 2.5 6.17	3.20E-00 2.26E-00 5.64 9.31	Vp Vrms dBm0 dBm	V V 1.18 V 0.775 V
LSP/LSN Output level symmetrical in a 50-Ω load ALS = – 21.5 dB	1.41E-01 9.95E-02 – 21.5 – 17.83	2.02E-01 1.43E-01 – 18.36 – 14.69	Vp Vrms dBm0 dBm	V V 1.18 V 0.775 V
HOP/HON Output level symmetrical in a 200-Ω load AHO = 2.5 dB	2.23E-00 1.58E-00 2.5 6.17	3.20E-00 2.26E-00 5.64 9.31	Vp Vrms dBm0 dBm	V V 1.18 V 0.775 V
HOP/HON Output level symmetrical in a 200-Ω load ALS = – 21.5 dB	1.41E-01 9.95E-02 – 21.5 – 17.83	2.02E-01 1.43E-01 – 18.36 – 14.69	Vp Vrms dBm0 dBm	V V 1.18 V 0.775 V

2.1.3 Interface to Acoustic Transducers



Note: ESD and EMV requirements are not included.

Figure 16
Example to Connect the AFE to Acoustic Transducers

2.2 ARCOFI® Signal Processor (ASP) Description

The ARCOFI signal processor (ASP) has been conceived to perform all ITU-T and ETSI (NET33) recommended filtering in transmit and receive paths and is therefore fully compatible to the ITU-T G.712 and ETSI (NET33) specifications. The data processed by the ASP is provided in the transmit direction by an oversampling A/D-converter situated in the analog front end (AFE). Once processed, the speech signal is converted into an 8-bit A-law or μ-law PCM format or remains as a 16-bit linear word (2s complement) if the compander is bypassed. The bypassing of the companding depends on the bit setting in the configuration register DFICR (VDM-bits).

In the receive direction, the incoming PCM stream is expanded into a linear format (if the linear mode is selected, the expansion logic is bypassed) and subsequently processed until it is passed to the oversampling D/A-converter.

Additionally to these standard codec functions, the ARCOFI provides a universal tone generation unit.

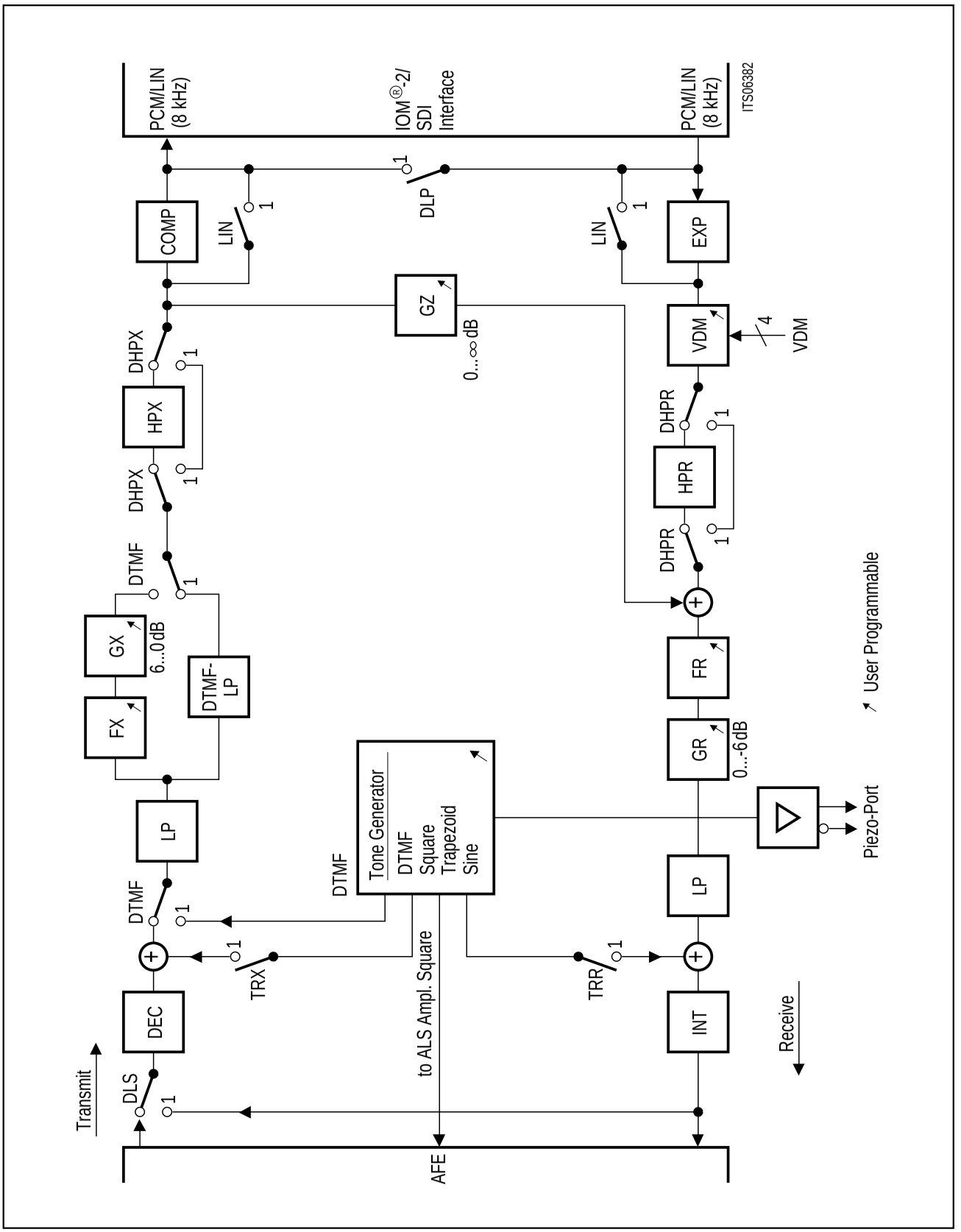


Figure 17
Processor Signal Flow Graph

2.2.1 Transmit Signal Processing

In the transmit direction a series of decimation filters reduces the sampling rate down to the 8-kHz PCM-rate. These filters attenuate the out-of-band noise by limiting the transmit signal to the voice band.

The decimation stages end with a EWDF low-pass filter which band limits the voice signal to the ITU-T G.712 and ETSI (NET33) recommendations. The ARCOFI meets or exceeds all the ITU-T and ETSI (NET33) recommendations on attenuation distortion and group delay distortion.

If the tone generation unit is connected to the transmit direction (TGSR.DTMF = 1), a special 2-kHz DTMF low-pass filter is placed in the transmit path. This filter guarantees an attenuation of all unwanted frequency components, if DTMF signals are transmitted. Additionally, it is possible to add a programmable tone signal to the transmit voice signal (TGSR.TRX = 1).

The GX-gain adjustment stage is digitally programmable allowing the gain to be programmed from + 6 to 0 dB in steps of ≤ 0.25 dB (– ∞ dB and others are also possible). Two bytes are necessary to set GX to the desired value. On reset, the GX-gain stage is bypassed.

The transmit path contains a programmable high performance frequency response correction filter FX allowing an optimum adaptation to different types of microphones (dynamic, piezoelectric or electret). Twelve bytes are necessary to set FX to the desired frequency correction function. On reset, the FX-frequency correction filter is bypassed. **Figure 18** shows the architecture of the FX/FR-filter.

A high-pass filter (HPX) is also provided to remove power line frequencies.

The voice signal, after being linearly processed, can be output as an 8-bit PCM-word according to the ITU-T G.711 A-law or the North-American µ-law format. If desired the companding stage can be bypassed, a 16-bit linear word (2s complement) is then output to the IOM-2 or SDI interface.

2.2.2 Receive Signal Processing

In the receive path the incoming PCM-signal is expanded into a linear code according to the selected A-law or µ-law. If the linear mode is chosen, the PCM-expander circuit is bypassed and a 16-bit linear word (2s complement) has to be provided to the processor.

The block VDM offers several possibilities of voice/data manipulation for special applications.

A programmable sidetone gain stage GZ adds a sidetone signal to the incoming voice signal. The sidetone gain can be programmed from – 54 to 0 dB within a ± 1 dB tolerance range (– ∞ dB and others are also possible). Respectively two bytes are coded in the CRAM to set GZ to the desired value. On reset, the GZ-gain stage is disabled (– ∞ dB).

A high-pass filter (HPR) is also provided to remove disturbances from 0 to 50/60 Hz due to the telecommunication network.

The FR-frequency correction response filter is similar to the FX-filter allowing an optimum adaptation to different types of loudspeakers or earpieces. Twelve bytes are necessary to set FR to the desired frequency correction function. On reset, the FR-frequency correction filter is bypassed.

The GR-gain adjustment stage is digitally programmable from – 6 to 0 dB in steps ≤ 0.25 dB (– ∞ dB and others are also possible). Respectively two bytes are coded in the CRAM to set GR to the desired value. On reset, the GR-gain stage is bypassed.

A low-pass EWDF-filter limits the signal bandwidth in the receive direction according to ITU-T and ETSI (NET33) recommendations.

A series of low-pass interpolation filters increases the sampling frequency up to the desired value.The last interpolator feeds the D/A-converter.

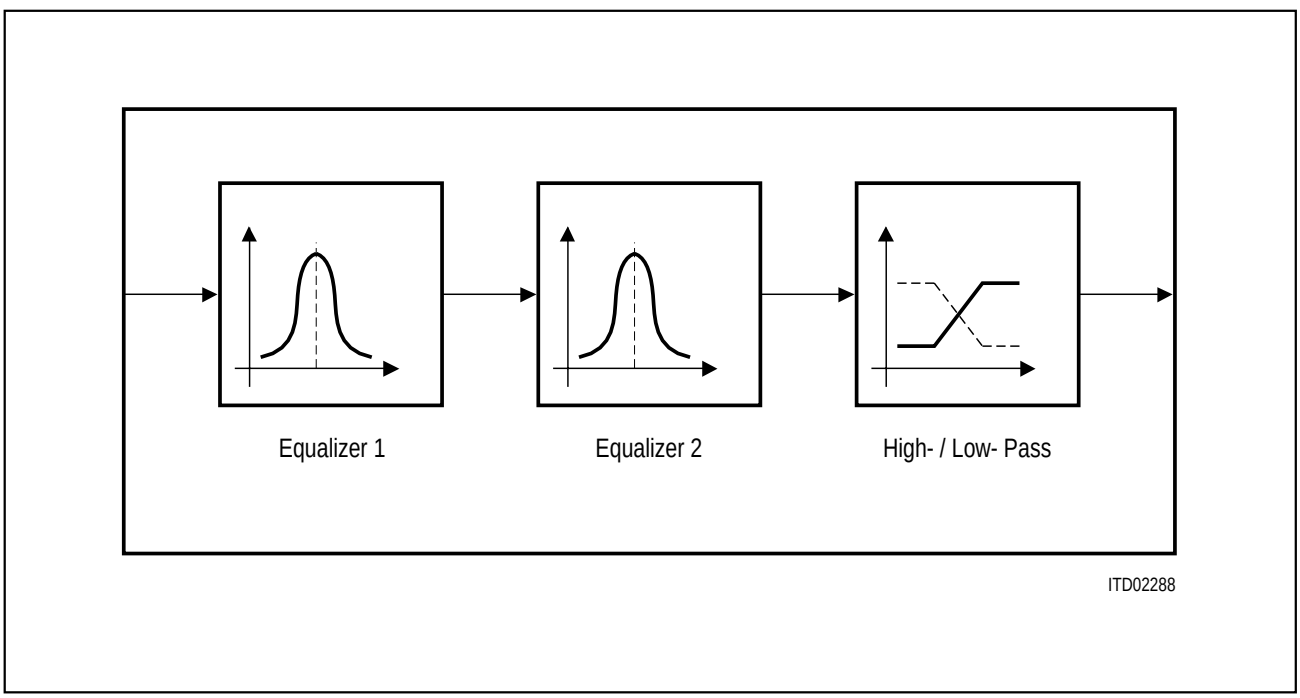


Figure 18
Architecture of the FX- and FR-Correction Filter

2.2.3 Programmable Coefficients

This section gives a short overview of important programmable coefficients. For more detailed information and about special applications, a special coefficient software package is available (ARCOS-SP PLUS SIPO 2163).

Description of the programmable level adjustment parameters:

Parameter	No. of CRAM Bytes	Range	Comment
GX	2	12 to – ∞ dB **6 to 0 dB**	Transmit gain adjustment Transmission characteristics guaranteed
GR	2	12 to – ∞ dB **0 to – 6 dB**	Receive gain adjustment Transmission characteristics guaranteed
GZ	2	0 to – ∞ dB	Sidetone gain adjustment

Coefficients for GX, GR and GZ:

Gain [dB]	MSB	LSB	Gain [dB]	MSB	LSB	Gain [dB]	MSB	LSB
12.0	10_H	01_H	0	$A0_H$	01_H	– 12.0	$A9_H$	01_H
11.0	10_H	31_H	– 0.5	$B3_H$	42_H	– 13.0	$9C_H$	51_H
10.0	10_H	13_H	– 1.0	$A3_H$	$2B_H$	– 14.0	99_H	13_H
9.0	01_H	$4B_H$	– 1.5	$A2_H$	32_H	– 15.0	$8C_H$	$1B_H$
8.0	20_H	94_H	– 2.0	BB_H	$4A_H$	– 16.0	82_H	$7B_H$
7.0	30_H	94_H	– 2.5	BB_H	13_H	– 17.0	84_H	$4B_H$
6.0	13_H	51_H	– 3.0	BA_H	29_H	– 18.0	89_H	$6A_H$
5.5	$B0_H$	39_H	– 3.5	BA_H	$5B_H$	– 19.0	$8B_H$	$0C_H$
5.0	$A0_H$	49_H	– 4.0	$A2_H$	01_H	– 20.0	84_H	$1C_H$
4.5	23_H	01_H	– 4.5	AA_H	$1B_H$	– 21.0	$8C_H$	$1C_H$
4.0	22_H	$B4_H$	– 5.0	$9B_H$	$3A_H$	– 22.0	82_H	$7C_H$
3.5	23_H	12_H	– 5.5	AA_H	33_H	– 23.0	84_H	$4C_H$
3.0	32_H	$A4_H$	– 6.0	AA_H	22_H	– 24.0	89_H	$6B_H$
2.5	$B1_H$	BC_H	– 7.0	$B9_H$	$2C_H$	– 25.0	$8B_H$	$0D_H$
2.0	$B1_H$	03_H	– 8.0	$9A_H$	BC_H	– 26.0	84_H	$1D_H$
1.5	33_H	39_H	– 9.0	$9B_H$	13_H	– ∞	88_H	01_H
1.0	$B2_H$	$5A_H$	– 10.0	$9B_H$	32_H			
0.5	$B3_H$	49_H	– 11.0	93_H	02_H			

2.2.4 Tone Generation

2.2.4.1 Tone Generation Architecture

The ASP contains a universal tone generator which can be used for tone alerting, call progress tones, DTMF signals or other audible feedback tones.

For the receive channel, a universal switching to each signal path (earpiece, loudspeaker and piezo ringer) is implemented. In the earpiece and loudspeaker direction, an addition of the programmed tone sequence (sine-wave, trapezoid, square-wave and DTMF) with the incoming voice signal is possible.

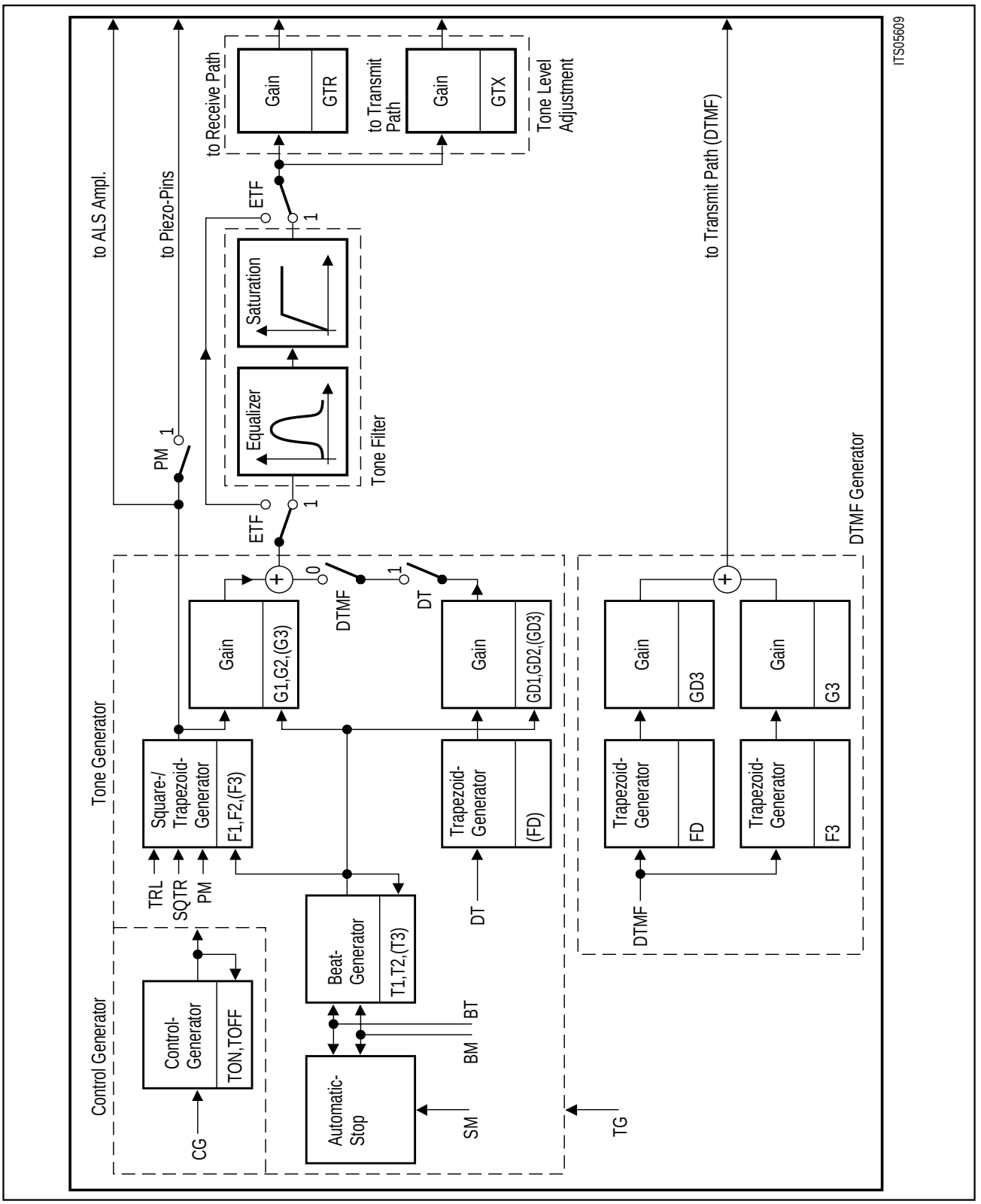
For the transmit direction, a supplementary DTMF generator is implemented. If the DTMF generator is active (TGSR.DTMF = 1), only a part of the tone generator (TG) is available for the receive direction (one or two tone sequences). In addition, a universal switching to the transmit path is also possible (TGSR.TRX).

All the tone generation configurations are programmable in the registers TGCR and TGSR (see description in **chapter 4**). A signal flow graph of the ARCOFI tone generation unit is shown in **figure 20**.

The tone generation can be subdivided into five main blocks:

- Control Generator (CG)
- Tone Generator (TG)
- Tone Filter (TF)
- Tone Level Adjustment (TLA)
- DTMF Generator (DTG)

A detailed description of the five main tone generation blocks follows in the next subsections.



Note: Adjustments in brackets are only available if the DTMF generator is switched off (TGCR.DTMF = 0).

Figure 19
Signal Flow Graph of the Tone Generation Unit

2.2.4.2 Control Generator

In conjunction with the control generator it is possible to generate very complex signal sequences without reprogramming the necessary parameters (e.g. pulsed three tone calls). Four typical applications for the control generator programming are shown in **figure 20**.

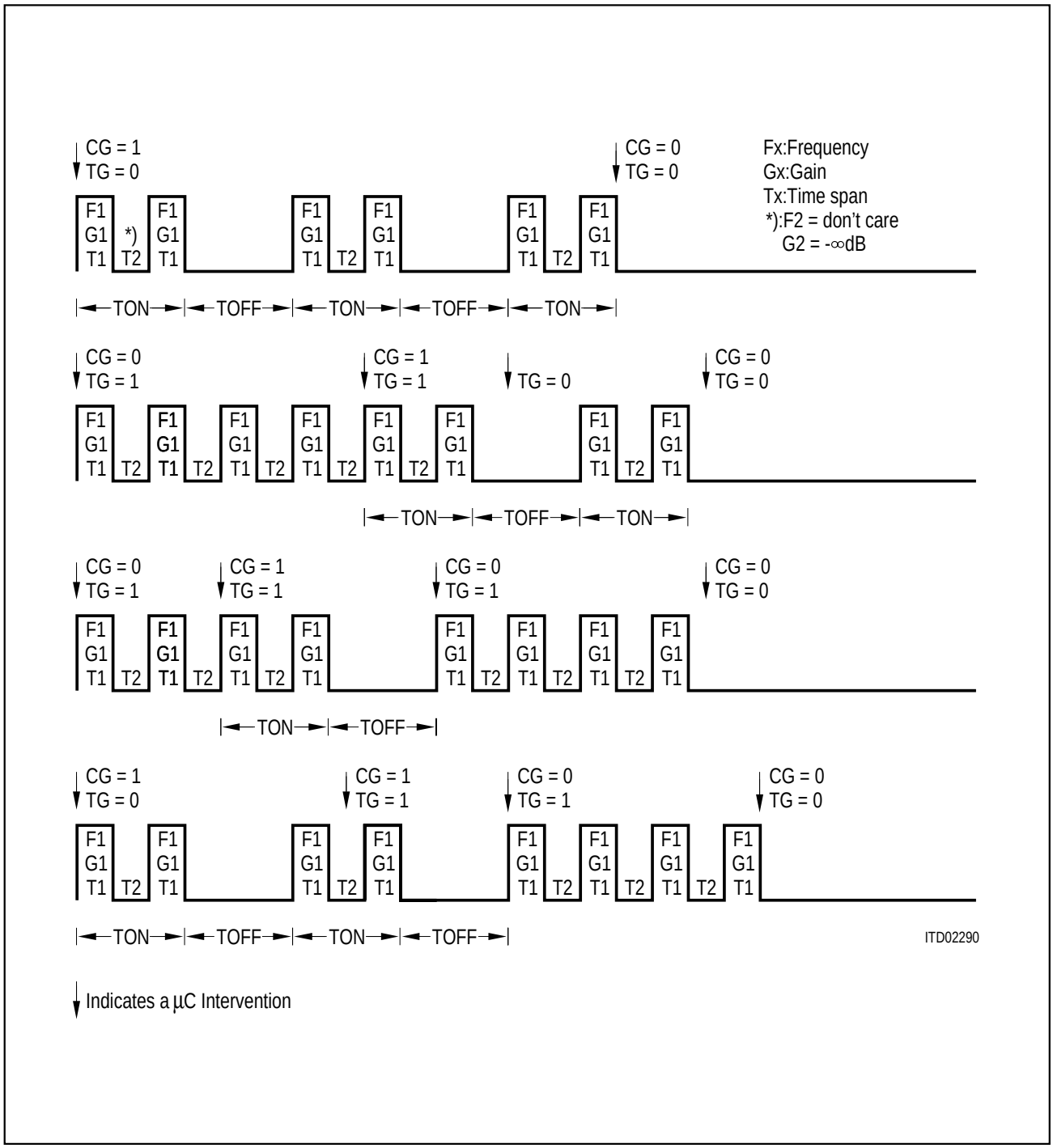


Figure 20
Typical Control Generator Application

Function table of CG/TG-bit setting in TGCR:

TON/TOFF	CG	TG	Generator Output
X	0	0	No tone
X	0	1	Ringing sequence F1, F2, F3 without break
TOFF	1	X	Break between two ringing sequences of F1, F2, F3
TON	1	X	Ringing sequence until next break

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
TON	2	20 ms to 16 min	Period while the tone generator is turned on
TOFF	2	20 ms to 16 min	Period while the tone generator is turned off

2.2.4.3 Tone Generator

The tone generator contains a beat generator, a square/trapezoid generator, a second trapezoid generator and an automatic stop for two and three tone ringing signals. With the automatic stop function (SM-bit setting in TGCR) the multitone generation can be stopped after a sequence is completed. This avoids unpleasant sounds when stopping the tone generator.

If the control generator is activated (TGCR.CG = 1) the bit setting of TG is insignificant. Otherwise (TGCR.CG = 0) the TG-bit setting controls the activities of the tone generator.

A functional diagram of the tone generator is shown in **figure 21**.

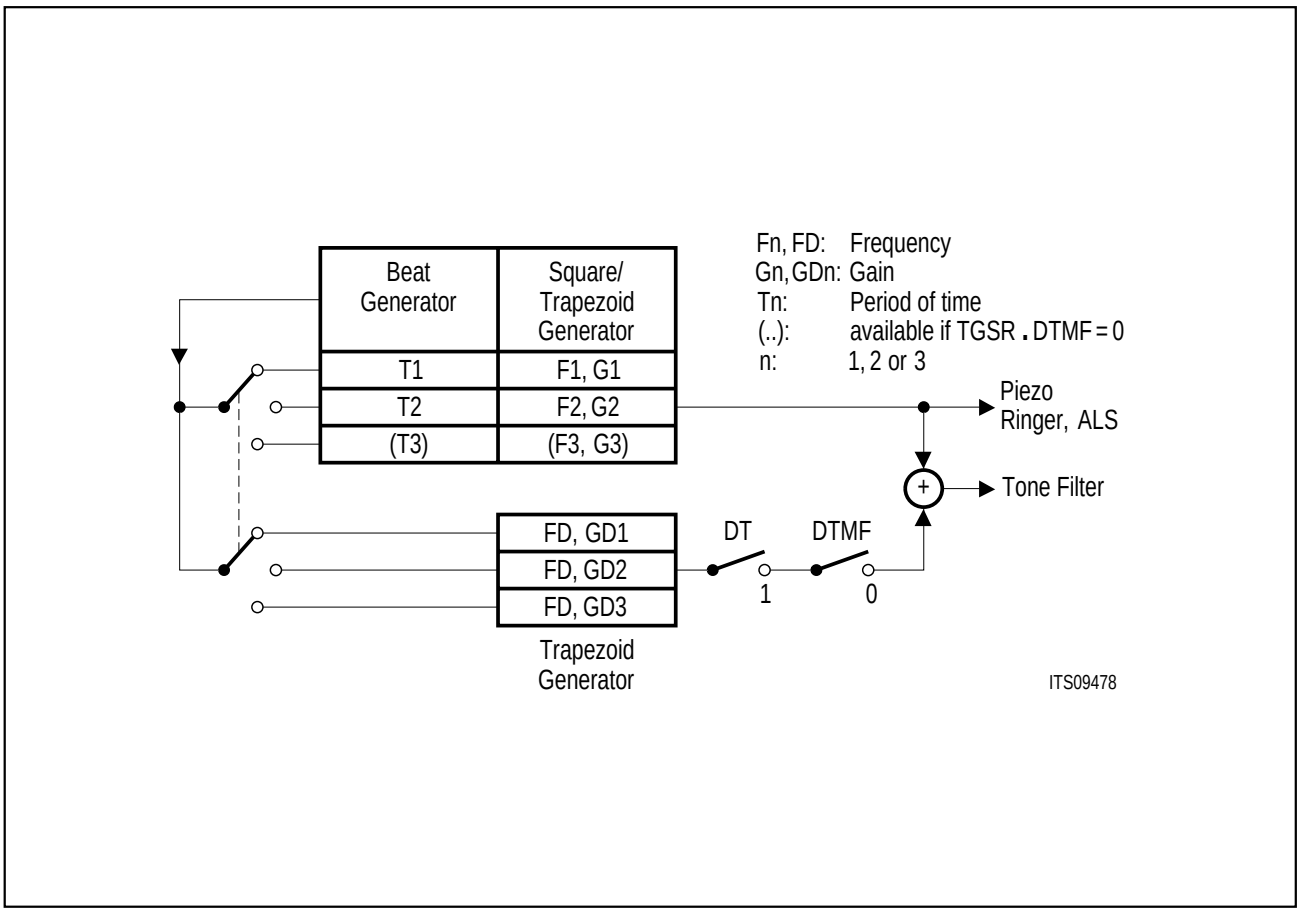


Figure 21
Functional Diagram of the Tone Generator

Distinctive alerting signals, allowing for example the use of different multitone ringing patterns, are all programmable using the beat tone generator in conjunction with the square/trapezoid generator. In the case of two or three tone ringing signals, the square/ trapezoid generator controls the output frequency pitch whilst the beat generator controls the repetition rate. Either square or trapezoid shaped tones can be generated depending on the TGCR.SQTR bit setting. If the piezo mode (PM or TRL in TGSR) is chosen, only a square-wave is available (fixed amplitude of V_{DD}). In this case the SQTR-bit in TGCR has no effect.

A secondary trapezoid generator is also built into the ARCOFI. Depending on the DT-bit setting in the TGCR, the output signal of this generator is added to the output signal of the Square/Trapezoid (S/T) generator. In conjunction with the S/T generator, a wide variety of different dual tone signals can be programmed.

If the beat generator (TGCR.BT = 1) is enabled, the automatic stop function (SM-bit setting in TGCR) can be activated. This prevents an uncontrolled turn-off of the tone generator. Only when the generation of the frequency F2 or F3 (depending on the BM-bit setting in TGCR) has been completed, the tone generator will switch off.

Beat generator programming:

BT	BM	DT	Generator Output
0	0	0	Continuous signal F1, G1
0	0	1	Continuous signal F1, G1 + FD, GD1
0	1	0	Continuous signal F2, G2
0	1	1	Continuous signal F2, G2 + FD, GD2
1	0	0	Alternating signal F1, G1, T1; F2, G2, T2
1	0	1	Alternating signal F1, G1, T1; F2, G2, T2 + FD, GD1, T1; FD, GD2, T2
1	1	0	Alternating signal F1, G1, T1; F2, G2, T2; F3, G3, T3
1	1	1	Alternating signal F1, G1, T1; F2, G2, T2; F3, G3, T3 + FD, GD1, T1; FD, GD2, T2; FD, GD3, T3

Description of the programmable parameters:

Parameter	No. of CRAM Bytes	Range	Comment
Fn	2/2/2	50 Hz to 4 kHz	Trapezoid shaped tone
		16 kHz/m; (m ≥ 3)	Square-wave signal
Gn	1/1/1	0 dB to – 48 dB	Gain adjustment for square/trapezoid generator
Tn	2/2/2	10 ms to 8 s	Period of time for two or three tone sequences
FD	2	50 Hz to 4 kHz	Trapezoid shaped tone
GDn	1/1/1	0 dB to – 48 dB	Gain adjustment for trapezoid generator

n is either 1, 2 or 3

Note: 0 dB gain setting of G1, G2 or G3 and GD1, GD2 or GD3 corresponds to the maximum PCM level (A-Law: + 3.14 dBm0)

2.2.4.4 Tone Filter

The tone filter contains a programmable equalizer and a saturation amplifier (**see figure 19**). If no filter function is necessary, a bypass mode can be used (TGCR.ETF = 0). A brief description of the tone filter follows below.

The equalizer is realized as a band-pass filter. The filter parameters (center frequency, bandwidth, and attenuation of the stopband) are programmable.

A generated square-wave or trapezoid signal can be converted by the equalizer into a sine-wave signal. A maximum attenuation of the first harmonic frequency of 50 dB is possible.

The two main purposes of the programmable saturation amplification are:

- Level balancing of the filtered signal (avoidance of overload effects).
- Amplification up to + 12 dB followed by a saturation (3.14 dBm0) of the incoming signal. This saturation amplification converts a sine-wave signal into a square-wave or a trapezoid signal where their edges are eliminated. This method produces pleasant ringing tones.

Description of the programmable parameters:

Parameter	No. of CRAM Bytes	Range	Comment
A1	1	200 Hz to 4 kHz	Center frequency
A2	1	0 to – 1	Determines with A1 and K the bandwidth. The closer A2 comes to -1, the smaller the bandwith.
K	1	0 to 54 dB	Attenuation of the stopband
GE	1	+ 12 to – 12 dB	Saturation amplification

2.2.4.5 Tone Level Adjustment

The two level adjustment stages GTR and GTX determines the output levels of the tone generation (**see figure 19**).

Description of the programmable parameters:

Parameter	No. of CRAM Bytes	Range	Comment
GTX	1	0 dB to – 50 dB (also – ∞ dB)	Level adjustment for the output which is connected to the transmit channel
GTR	1	0 dB to – 50 dB (also – ∞ dB)	Level adjustment for the output which is connected to the receive channel

2.2.4.6 DTMF Generator (transmit)

The DTMF generator contains two independent trapezoid generators which can be programmed in a wide frequency and gain range. If the DTMF generator is active (TGSR.DTMF = 1), the output signal is automatically switched to the transmit direction. In this case the attenuation of the unwanted frequency components is executed by a special DTMF low-pass filter to the following limits:

Frequency Band	Min. Attenuation
0 – 300 Hz	33 dB
300 – 3400 Hz	20 dB
3400 – 4000 Hz	33 dB

The pre-emphasis of 2 dB between the high and the low DTMF frequency groups has to be set with the independent gain stages for the two trapezoid generators (G3 and GD3). All generated DTMF frequencies are guaranteed within a ± 1 % deviation.

DTMF-frequency (F3, FD) programming:

ITU-T Q.23	ARCOFI® Nominal	Relative Deviation from ITU-T	Coefficients	
			high	low
Low Group				
697	697.1	+ 143 ppm	4F	16
770	770.3	+ 390 ppm	A6	18
852	852.2	+ 235 ppm	45	1B
941	941.4	+ 425 ppm	20	1E
High Group				
1209	1209.5	+ 414 ppm	B4	26
1336	1336.9	+ 674 ppm	C8	2A
1477	1477.7	+ 474 ppm	49	2F
1633	1632.8	– 122 ppm	40	34

Note: The deviations due to the inaccuracy of the incoming clock DCL/MCLK, when added to the nominal deviations tabulated above give the total absolute deviation from the ITU-T recommended frequencies.

Description of the programmable parameters:

Parameter	No. of CRAM Bytes	Range	Comment
F3	2	50 Hz to 4 kHz	Trapezoid shaped tone 1
G3	1	0 dB to – 48 dB	Gain adjustment for trapezoid generator 1
FD	2	50 Hz to 4 kHz	Trapezoid shaped tone 2
GD3	1	0 dB to – 48 dB	Gain adjustment for trapezoid generator 2

2.3 ARCOFI® Digital Interface (ADI)

The ADI-function consists of two interface blocks:

- The Peripheral Control Interface (PCI) or the Serial Control Interface (SCI)
- The IOM-2 interface (TE or NON-TE timing mode) or the Serial Data Interface (SDI)

Supplementary functions are accessed by strapping the pins MODE and AD according to the following table:

Pin MODE	Pin AD	Mode	Description
0	0	IOM-2 TE	IOM-2 TE timing mode (AD = 0)
0	1	IOM-2 TE	IOM-2 TE timing mode (AD = 1)
0	MCLK	Test	
1	0	IOM-2 NON TE	IOM-2 NON-TE timing mode (AD = 0)
1	1	IOM-2 NON TE	IOM-2 NON-TE timing mode (AD = 1)
1	MCLK	SDI	Serial Data Interface

A detailed description is in the following chapter.

2.3.1 PCI-Interface

The Peripheral Control Interface (PCI) provides 4 programmable l/O pins to control the peripheral devices (for more detailed information see section 4, DFICR). These four interface pins are only available in the IOM-2 terminal mode (TE mode).

Otherwise three pins (SB, SC, SD) are used as slot select pins in the IOM-2 NON-TE mode or used as a Serial Control Interface (SCI).

SA-SD	Mode
PCI	IOM-2 TE
Slot Select	IOM-2 NON TE
SCI	Serial Mode

2.3.2 IOM®-2 Frame Structure and Timing Modes

This interface consists of one data line per direction (DD: Data Downstream; DU: Data Upstream). Two additional signals define the data clock (DCL) and the frame synchronization (FSC).

In terminal applications, the IOM-2 constitutes a powerful backplane bus offering intercommunication and sophisticated control capabilities for peripheral modules.

The channel structure of the IOM-2 is described in **figure 22**.

Figure 22
Channel Structure of IOM-2

- The 64-kbit/s channels, B1 and B2, are conveyed in the first two bytes.
- The third byte (monitor channel) is used for programming and controlling devices attached to the IOM-2 interface.
- The fourth byte (control channel) contains two bits for the 16-kbit/s D-channel, four command/indication bits for controlling activation/deactivation and for additional control functions, two bits MR and MX for supporting the handling of the MONITOR channel.

In case of an IOM-2 interface the frame structure depends on whether TE or NON-TE mode is selected.

NON-TE Timing Mode

The frame of this mode is a multiplex of eight IOM-2 channels (**figure 23**), each channel has the structure as shown in **figure 22**.

The ARCOFI is assigned to one of eight channels (0 to 7) by strapping SB to SD according to the following table:

Pin SD	Pin SC	Pin SB	Selected IOM-2 Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Pin SA is not used in this mode and should be connected to V_{DD} or V_{SSD}.

Thus the data rate per channel is 256 kbit/s, whereas the bit rate is 2.048 kbit/s. The IOM-2 interface signals are:

DD, DU : 2048 kbit/s
DCL : 4096 kHz (double clock rate)
FSC : 8 kHz

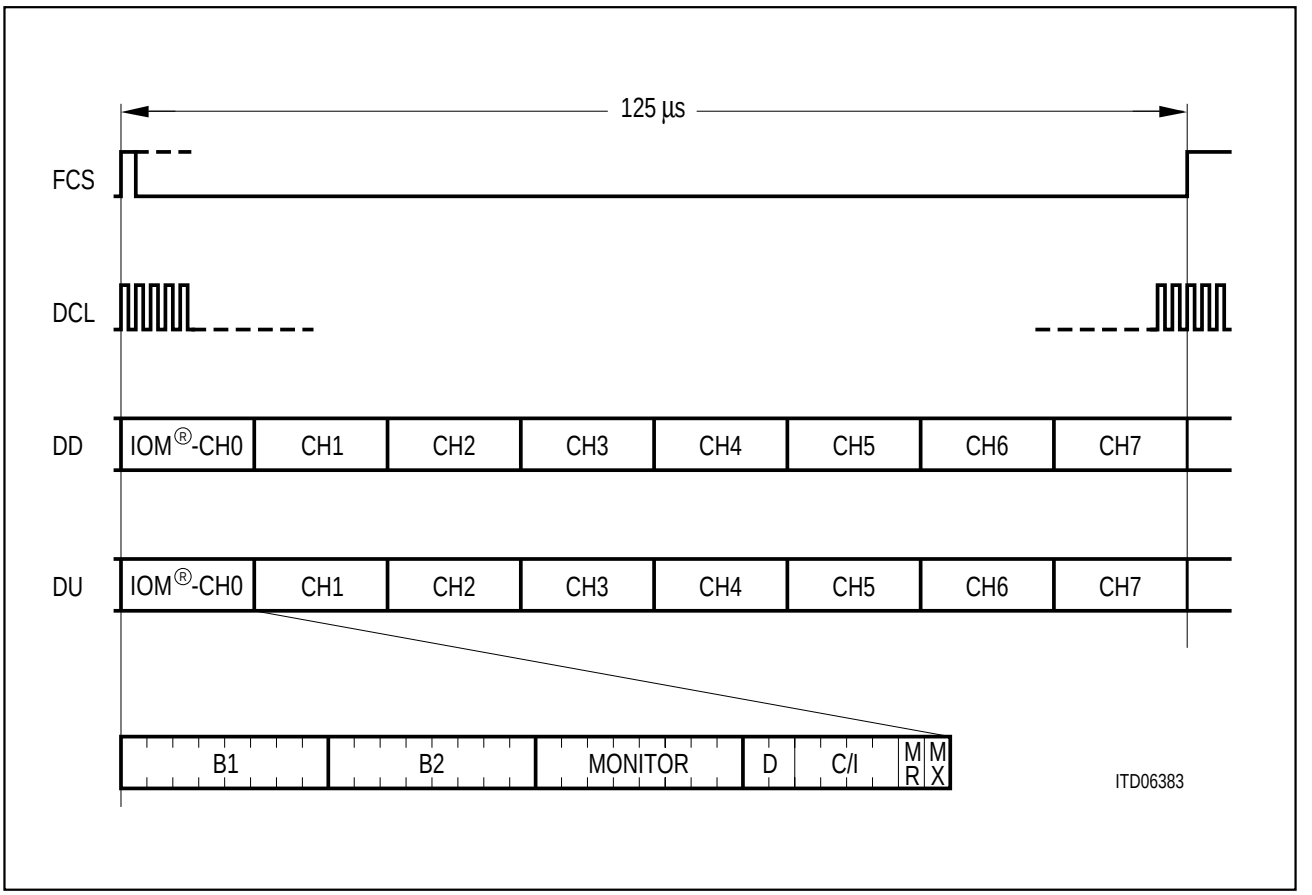


Figure 23
Multiplexed Frame Structure of the IOM®-2 Interface in NON-TE Timing Mode

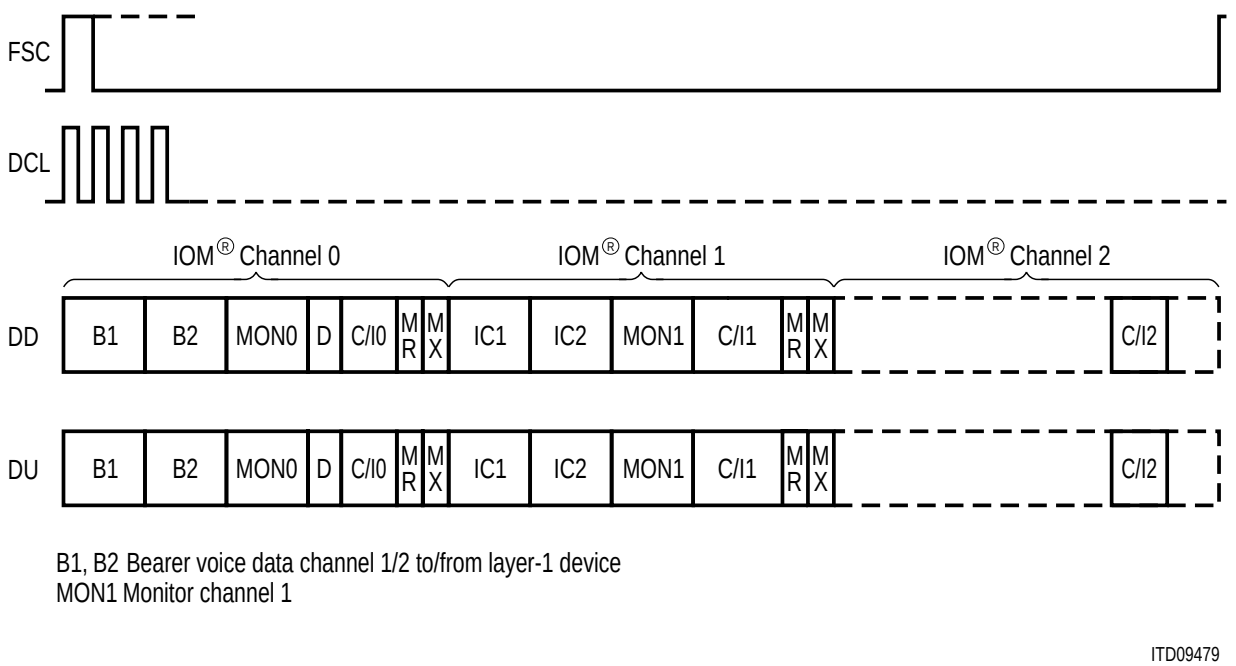
TE Timing Mode

The IOM-2 frame provides three complete IOM channels (**figure 24**):

- Channel 0 contains 144 kbit/s (2B + D) plus monitor and command/indication channels for the layer-1 device.
- Channel 1 contains two 64-kbit/s intercommunication channels plus monitor and command/indication channels for other IOM-2 devices (e.g. ARCOFI).
- Channel 2 is used for D-channel arbitration.

The IOM-2 signals are:

DD, DU : 768 kbit/s
DCL : 1536 kHz (double clock rate)
FSC : 8 kHz



B1, B2 **Bearer voice data channel 1/2 to/from layer-1 device**
MON1 **Monitor channel 1**
C/I1 **Command/Indicate channel 1**
IC1, IC2 **Intercommunication channel 1/2**

Figure 24
IOM®-2 Interface Structure in TE Mode

2.3.3 Serial Control Interface

When the MODE pin is tied high and the AD/MCLK pin is used as system clock input (MCLK), the internal configuration registers and the coefficient RAM of the ARCOFI are programmable via the serial control interface. It consists of 4 lines: SCLK, SDR, SDX (open drain or push-pull) and $\overline{CS}$.

$\overline{CS}$ is used to start a serial access to the ARCOFI registers and the coefficient RAM. Following a falling edge on $\overline{CS}$, the first eight bits transmitted on SDR specify the command. The subsequent one, two, four or eight bytes (depending on command) read(s) or write(s) the contents of the selected registers or RAM-locations until the $\overline{CS}$ line becomes inactive. If a read command is chosen, the first byte after the command is the identification code (<IDENT>) of the ARCOFI-SP PSB 2161 (**see also chapter 3.4.2.1**). After one command sequence is completed at least one NOP-command is required (**see figure 25**).

A transfer sequence can be broken by setting $\overline{CS}$ high. All bytes already sent when $\overline{CS}$ changes to high are valid, except the last one.

The data transfer is synchronized by the SCLK input. SDX changes with the falling edge of SCLK while the contents of SDR is latched on the rising edge of SCLK.

Figure 25 shows the timing of a serial control interface transfer (one byte transfer).

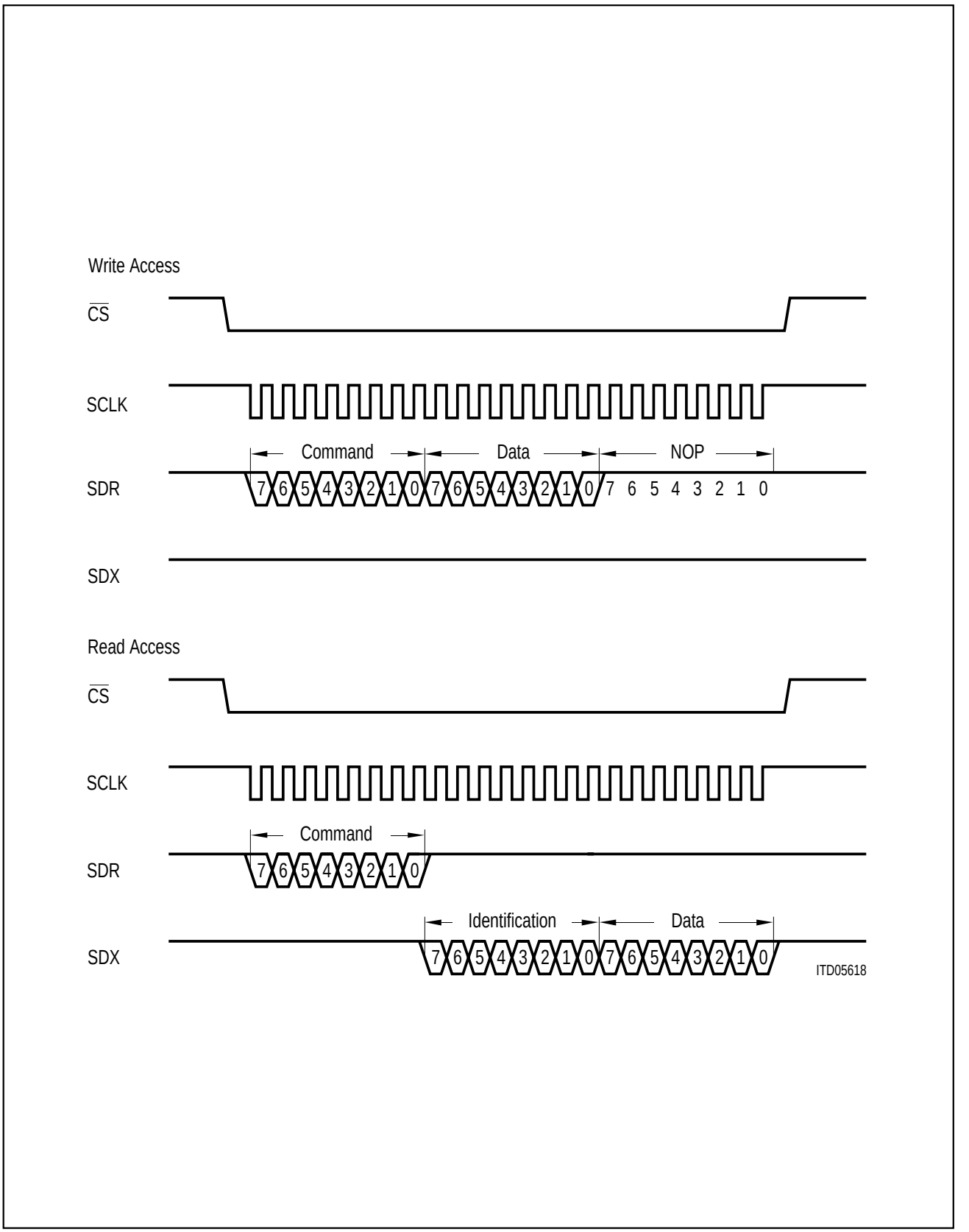


Figure 25
Serial Control Interface Timing

2.3.4 Serial Data Interface

If the serial control interface is selected, the ARCOFI supports an additional serial data interface for B-channel transfer. This control interface consists of five lines: FSC, DCLK, DX, DR and MCLK.

FSC is a 8-kHz frame synchronization signal.

The DCLK is the clock signal to synchronize the data transfer on both data lines DX and DR. The rising edge indicates the start of the bit while the falling edge is used to latch the contents of the received data line DR. If the double clock rate is chosen (twice of the transmission rate) the first rising edge indicates the start of a bit while the second falling edge is used to latch the content of the data line.

The data rate of the interface can vary from 64 kbit/s to 4.096 Mbit/s. A frame may consist of up to 64 time-slots of 8 bits each. The last 6 bits of TSCR (Time Slot Configuration Register) indicate the selected time slot from 0 to 63. If a 16-bit mode (linear mode) is chosen, the lowest data rate is 128 kbit/s and the time-slot must be set to an even number.

The pin AD/MCLK is a system clock synchronized with FSC (necessary to synchronize internal PLL).

Figure 26 shows the timing of a serial data interface (256 kbit/s with single clock rate).

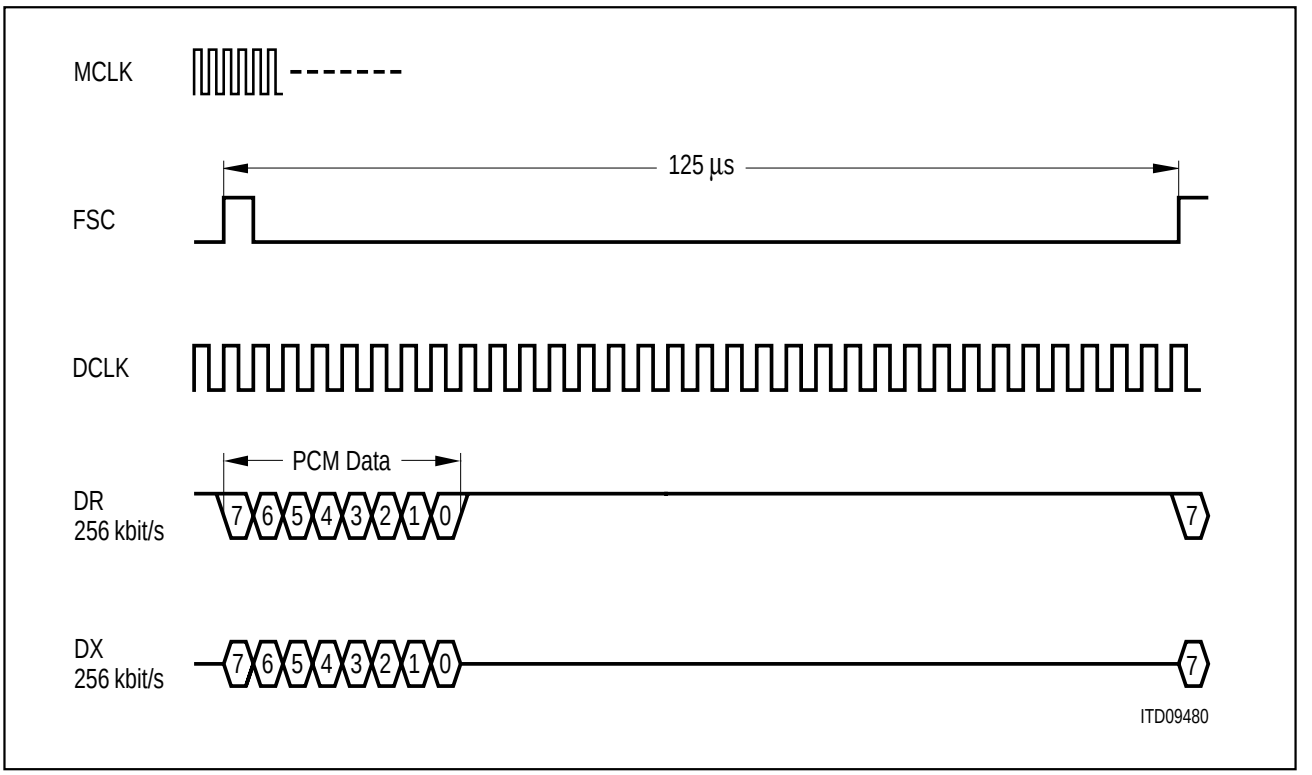


Figure 26
Serial Data Interface Timing

2.4 Test Functions

The ARCOFI provides several test and diagnostic functions which can be grouped as follows:

- All programmable configuration registers and coefficient RAM-locations are readable
- Digital loop via PCM-register (DLP)
- Digital loop via signal processor (DLS)
- Digital loop via noise shaper (DLN)
- Analog loop via analog front end (ALF)
- Analog loop via converter (ALC)
- Analog loop via noise shaper (ALN)
- Analog loop via Z-sidetone (ALZ); sidetone gain stage GZ must be enabled (PFCR.GZ = 1) and sidetone gain must be programmed with 0 dB; depending on the VDM-bit setting (DFICR) an addition to the incoming voice signal is possible
- Analog loop via digital interface (ALI).

3 Operational Description

3.1 Reset

After a RESET (hardware reset at pin RS or software reset via XOP_E) the pins SA to SD are programmed as inputs. All other output pins are in high-impedance state (HOP/HON, LSP/LSN, V_{REF}, PZ1, PZ2, DU/DX).

Note: After a Reset (only TE and NON-TE mode) the coefficient RAM-locations have defined reset values.

The defined reset values of the ARCOFI-registers are listed below:

Register	Value after RESET [hex]	Meaning
CMDR	BF	– No operation (NOP)
GCR	00	– Disable voice transmit – IOM-2 channel 0 selected (IOM-2 TE-mode) – Power-down mode – IOM-2 two chip mode (IOM-2 TE-mode) – A-Law
DFICR	F0	– SA to SD programmed as inputs – PCM-mode; receive voice blocked
PFCR	00	– Programmable digital gain disabled – Programmable sidetone gain disabled – Correction filters disabled – 50/60-Hz receive HP active – 50/60-Hz transmit HP active
TGCR	00	– Tone generator inactive – Control generator inactive
TGSR	00	– No tone generator connection to any signal path
ATCR	00	– Microphone amplifier is in power-down mode – Reference voltage buffer is in power-down mode – Pins MIP1/MIN1 are directed to the microphone amplifier AMI
ARCR	00	– Earpiece amplifier AHO is in power-down mode – Loudspeaker amplifier ALS is in power-down mode
TFCR	00	– Analog test mode disabled – Digital test mode disabled
SDICR	00	– Single clock rate (DCLK) is enabled – DX and SDX are configured as open drain outputs – Master clock rate is 512 kHz
TSCR	00	– Time-slot 0 (SDI) is selected
XCR	00	– AHO and ALS are in the differential mode
CRAM	00	– All locations (TE and NON-TE)

3.2 Initialization

During initialization a subset of configuration registers and coefficient RAM-locations has to be programmed to set the configuration parameters according to the application and desired features.

Configuration Registers

Register	Bit	Effect	Restricted to
GCR	EVX	Enable voice transmit	
	SLOT	IOM-2 slot select	IOM-2 TE
	PU	Power-up/down mode	
	CAM	IOM-2 address mode	IOM-2
	LAW	A-Law/µ-Law	
DFICR	SA-SD	PCI-port configuration	IOM-2 TE
	VDM	Voice data manipulation	
PFCR	GX	TX digital gain	
	GR	RX digital gain	
	GZ	Sidetone gain	
	FX	TX-frequency correction filter	
	FR	RX-frequency correction filter	
	DHPR	Disable high-pass (50/60 Hz) receive	
	DHPX	Disable high-pass (50/60 Hz) transmit	
TGCR	TG	Tone generator	
	DT	Dual tone mode	
	ETF	Enable tone filter	
	CG	Control generator	
	BT	Beat tone generator	
	BM	Beat mode	
	SM	Stop mode	
	SQTR	Square/trapezoid shaped signal	
TGSR	PM	Piezo mode	
	TRL	Tone ringing via loudspeaker	
	TRR	Tone ringing in receive direction	
	DTMF	DTMF-signal in transmit direction	
	TRX	Tone ringing in transmit direction	

Configuration Registers (cont'd)

Register	Bit	Effect	Restricted to
ATCR	MIC	Microphone amplifier control	
	EVREF	Enable 2.4 V reference voltage at pin V_{REF}	
	AIMX	Analog input multiplexer	
ARCR	HOC	Handset amplifier control	
	LSC	Loudspeaker amplifier control	
TFCR	ALTF	Analog Loops and test functions	
	DLTF	Digital Loops and test functions	
SDICR	EPP0	Enable push/pull (DX)	SDI
	EPP1	Enable push/pull (SDX)	SDI
	DCE	Double clock enable	SDI
TSCR	MCLKR	Master clock rate	SDI
XCR	TS	Time slot select	SDI
	DHOP	Disable HOP (tristate)	
	DHON	Disable HON (tristate)	
	DLSP	Disable LSP (tristate)	
	DLSN	Disable LSN (tristate)	

Note: Before accessing the ARCOFI PCI (IOM-2 TE mode) interface, a GCR-write command (SOP_0 or SOP_F) has to be sent.

Coefficient RAM-locations

Mnemonic	No. of Bytes	Effect
COP_0: Tone generator parameter set 1		
F1	2	Tone generator frequency
G1	1	Tone generator amplitude
GD1	1	Trapezoid generator amplitude
T1	2	Beat tone time
	2	not used
COP_1: Tone generator parameter set 2; tone generator level adjustment		
F2	2	Tone generator frequency
G2	1	Tone generator amplitude
GD2	1	Trapezoid generator amplitude
T2	2	Beat tone time span
GTR	1	Level adjustment for receive path
GTX	1	Level adjustment for transmit path
COP_2: Tone generator parameter set 3; Parameter set for the DTMF-generator (TGSR.DTMF = 1)		
F3	2	Tone generator frequency
G3	1	Tone generator amplitude
GD3	1	Trapezoid generator amplitude
T3	2	Beat tone time span
FD	2	Dual tone frequency
COP_3: Tone filter		
K	1	Attenuation of the stop-band
A1	1	Center frequency
A2	1	Bandwidth
GE	1	Saturation amplification
COP_4: Control generator		
TON	2	Turn-on period of the tone generator
TOFF	2	Turn-off period of the tone generator
COP_5: Receive and transmit gain		
GX	2	Transmit gain
GR	2	Receive gain
	4	Not used

Coefficient RAM-locations (cont'd)

Mnemonic	No. of Bytes	Effect
COP_6: Sidetone gain		
GZ	2 2	Sidetone gain not used
COP_7/COP_8: Transmit correction filter		
FX	12	Transmit correction filter coefficients
COP_8/COP_9: Receive correction filter		
FR	12	Receive correction filter coefficients

3.3 ARCOFI® Operating Modes

The most currently used ARCOFI operating modes are documented in the following table. The 12 ARCOFI configuration registers have enough build-in flexibility to accommodate an extensive set of user calling procedures.

The following operating mode description table is not exhaustive but should be used as an example of possible functions performed by the ARCOFI.

State	Description
POR	Power-on reset: when power is supplied to the ARCOFI an internal power-on reset is generated. In addition a hardware reset via an RC-network connected to input pin RS will force all ARCOFI internal registers to default values. The ARCOFI-registers reset state is described in section 3.1 and 4.
STAND BY	The system microprocessor can initialize the ARCOFI via the IOM-2 or the SCI-bus with a different set of filter and configuration values. Whilst remaining in power-down (GCR.PU = 0) a new set of filter coefficients and configuration bits can be loaded in the ARCOFI.
HANDSET	The system MPU detects activity from the hookswitch or from the keyboard. The ARCOFI can be placed in HANDSET state where all handset l/O are enabled (AMI & AHO activated).
RINGING	The system MPU detects an incoming call, the ARCOFI can be placed in a RINGING state by activating the tone ringer via TGCR/TGSR and configuring the ARCOFI such that either the LSP/LSN-output or the piezo output (pins PZ1/PZ2) are enabled. An emergency ringing is also implemented. In this mode, only the tone ringer and the loudspeaker amplifier are active (AMI- and AHO-amplifier are disabled by the user). The tone ringer signal is directly switched to the loudspeaker amplifier ALS.
DTMF	All audio inputs can be disabled by forcing the AMI-amplifier (ATCR) to power-down. DTMF tones are generated with the tone generator and are output to the transmit path.
PULSE DIAL	Handset audio path can be enabled by forcing a HANDSET mode. A single tone can be superimposed into the audio receive path so as to provide audible feedback when dialling.
LOUDHEARING (MONITORING)	The handset l/O and the loudspeaker outputs LSP/LSN are active (ATCR & ARCR).

Operating mode description table (cont’d)

State	Description
MUTE	The ARCOFI can be placed in a MUTE state by powering down the AMI. In handset mode the outputs HOP/HON remain enabled while in speakerphone mode the outputs LSP/LSN are enabled. All other analog I/O's being disabled.
FEATURE TONE	A single tone can be superimposed to the incoming PCM-voice signal. Applications requiring system function audible feedback are therefore made possible.

3.4 IOM®-2 Interface Protocol

The following description of the IOM-2 interface comprises all ARCOFI relevant functions in the terminal and non-terminal mode (see IOM-2 interface specification for general information).

Note: Channels IC1 & IC2 are only available in the IOM-2 TE mode. MON channel means MON1 channel in the IOM-2 TE mode or by pinstrapping selected MON channel in IOM-2 NON TE mode.

3.4.1 B- and IC-Channels (IOM®-2 TE Mode)

The ARCOFI can receive and transmit voice data in the IOM-2 B1- & B2-channels as well as in the IC1 & IC2 intercommunication channels located in IOM-2 channels 0 and 1 respectively. The voice/data channel allocation is programmable via the channel select bit SLOT in the GCR-register. B1 or B2 or respectively IC1 or IC2 can be programmed by use of the RCM-bit in the CMDR-register.

The IC1 and IC2 intercommunication channels can be used in the terminal for local data communication (e.g. answering machine). This makes post-processing of voice/data information possible (e.g. data encryption).

3.4.2 Monitor Channel

All programming data required by the ARCOFI including coefficients are transmitted exclusively in the MON time slot of the IOM-2 channel. The MON channel allows a point to multipoint access where the layer-2 component acts as the master to program devices like the ARCOFI. Each programmable device is accessed by sending a specific address byte at the start of each SOP or COP command stream. Before executing a command, the programmable device compares the received address byte with its own address. The latter consists of 8 bits whose 4th MSB-bit must correspond to the AD-wire (AD/MCLK pin) strapped IOM-2 address.

3.4.2.1 MON Channel Data Structure

The data to control and program the ARCOFI are transferred in the MON channel via the IOM-2 interface by a procedure utilizing read/write registers in the ARCOFI.

The messages transmitted in the monitor channel may have different kinds of data structures. Therefore, the first byte of the message is used to indicate the data structure (first four bits).

Identification Command

In order to be able to identify unambiguously different devices by software, the following identification command is used:

DD 1st byte value	1	0	1	X	0	0	0	0
DD 2nd byte value	0	0	0	0	0	0	0	0

The ARCOFI responds to this DD identification sequence by sending a DU identification sequence:

DU 1st byte value	1	0	1	X	0	0	0	0	
DU 2nd byte value	1	0	DESIGN						<IDENT>

X: logical 0 (active low): AD = 0 (A-chip)
logical 1 (passive high): AD = 1 (B-chip)

DESIGN:six bit code, specific for each device in order to identify differences in operation

e.g.	000000	ARCOFI	PSB 2160
	000010	ARCOFI-SP	PSB 2165
	000100	ARCOFI-SP	PSB 2163
	001000	ARCOFI-BA	PSB 2161

This identification sequence is usually done once, when the terminal is connected for the first time.This function is used so that the software can distinguish between different possible hardware configurations. However this sequence is not compulsory.

Programming Sequence

An ARCOFI programming sequence is characterized by a “1” being sent in the LSB nibble of the first incoming identification code.

DD 1st byte value	1	0	1	X	0	0	0	1
DD 2nd byte value	0	RCM	CMDx					

All programmed configurations and coefficients can be read back when issuing an appropriate CMDR read (CMDR.R/W = 1). The ARCOFI responds by sending an IOM-2 specific address byte identifying the chip followed by the requested data.

3.4.2.2 MON Transfer Protocol

The transfer of a stream of commands in the MON channel is regulated by a handshake protocol mechanism implemented by two bits MX and MR in the fourth slot of the IOM-2 channel. The procedure is as follows (**figure 27**):

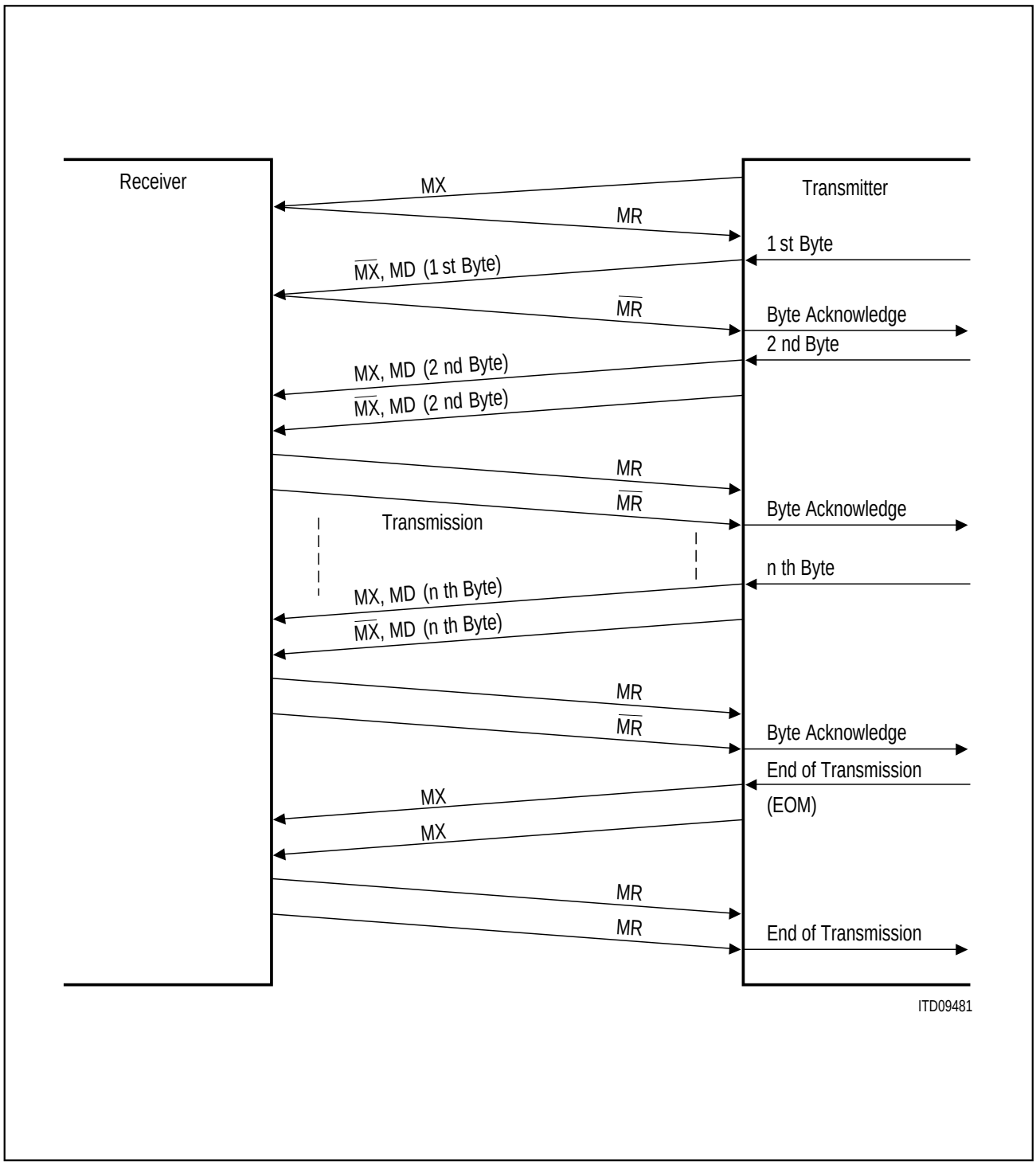


Figure 27
Monitor Channel Handshake Procedure

Monitor transfer protocol rules:

- A pair of MX and MR in the inactive state for two or more consecutive frames indicates an idle state or an end of transmission (EOM).
- A command stream initiated by a transmitter in the MON slot is accompanied by an activated downstream MX-bit.
- The receiver acknowledges a received byte by toggling the upstream MR-bit from inactive to active in the subsequent IOM-2 frame for at least one frame.
- The transmitter indicates a new byte in the MON slot by the transition of the MX-bit from the active to the inactive state. The MX-bit returns to the active state after one frame. Two frames with the MX-bit in the inactive state indicate the end of transmission.
- The receiver acknowledges each new byte by a similar one frame transition of the MR-bit to the inactive state. Two frames with the MR-bit set to inactive indicate a receiver request for abort.
- The transmitter can delay a transmission sequence by sending the same byte continuously. In that case the MX-bit remains active in the IOM-2 frame following the first byte occurrence.
- Delaying a transmission sequence is only possible while the receiver MR-bit and the transmitter MX-bit are active.
- Since the receiver is able to receive the MON slot data at least twice (in two consecutive frames), the receiver waits for the reception of two successive identical bytes.
- To control this handshake procedure a collision detection mechanism is implemented in the transmitter. This is done by making a collision check per bit on the transmitted MON data (MD).

3.4.2.3 Implementation of the MON-Channel Protocol

The MON receiver has the following features:

- Transparent interface between IOM-2 interface and any device internal block (sink) with respect to handshake procedure, i.e. any acknowledge, EOM, abort or request for abort is conveyed transparently through the receiver.

Figure 28 shows the state diagram of the MON receiver. The following signals are used:

MR: MR-bit sent by the receiver
MX: MX-bit received
LL: Last two bytes were identical

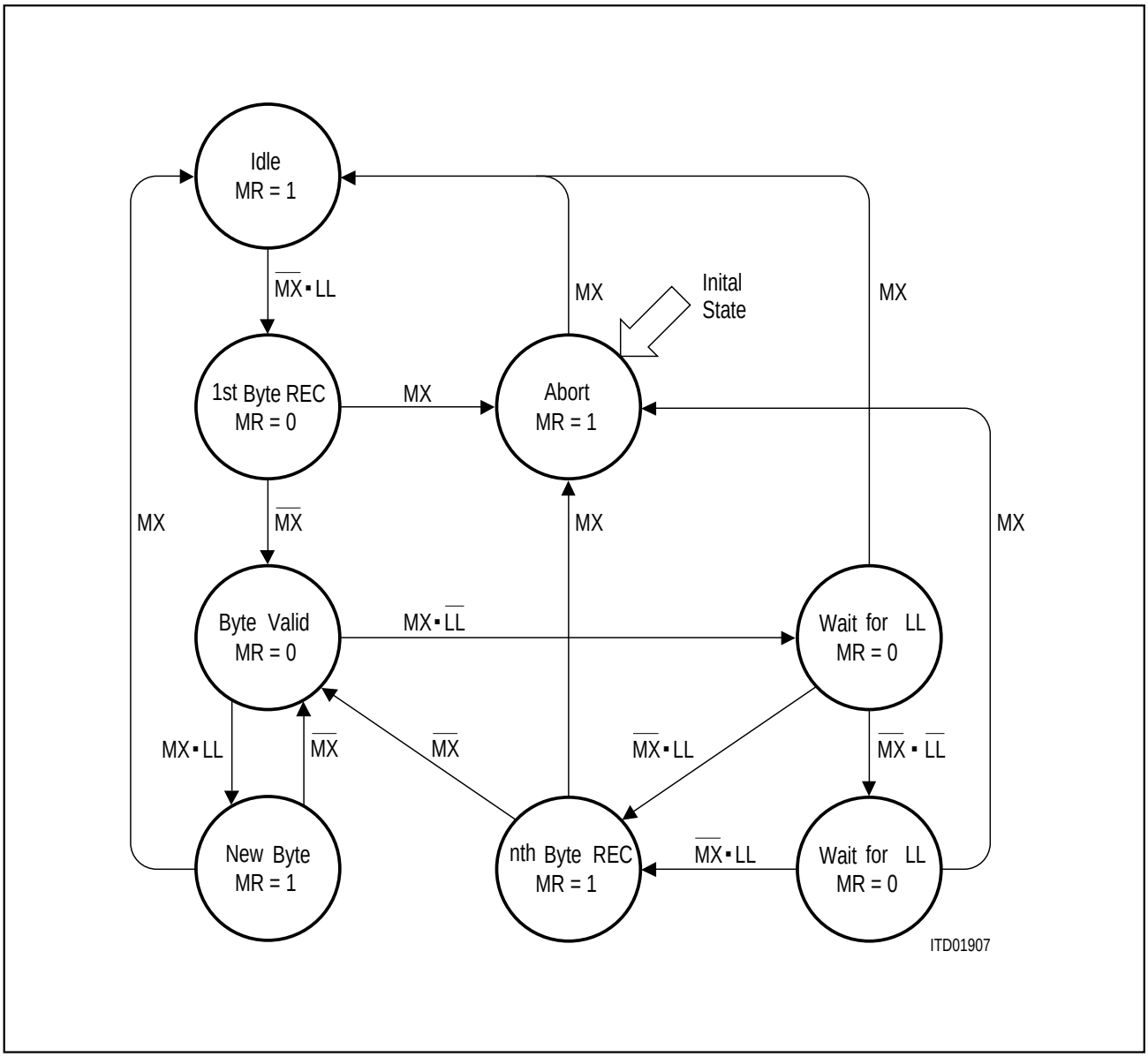


Figure 28
State Diagram of the Monitor Receiver

The MON transmitter has the following features:

- Transparent interface between IOM-2 interface and any device internal block (source) with respect to handshake procedure, i.e. any acknowledge, abort, request for abort is conveyed transparently through the transmitter.

Figure 29 shows the state diagram of the MON transmitter. The following signals are used:

MR: MR-bit received
MX: MX-bit transmitted
LL: Last two bytes were identical
RQT: Request transmission
EOM: End of transmission

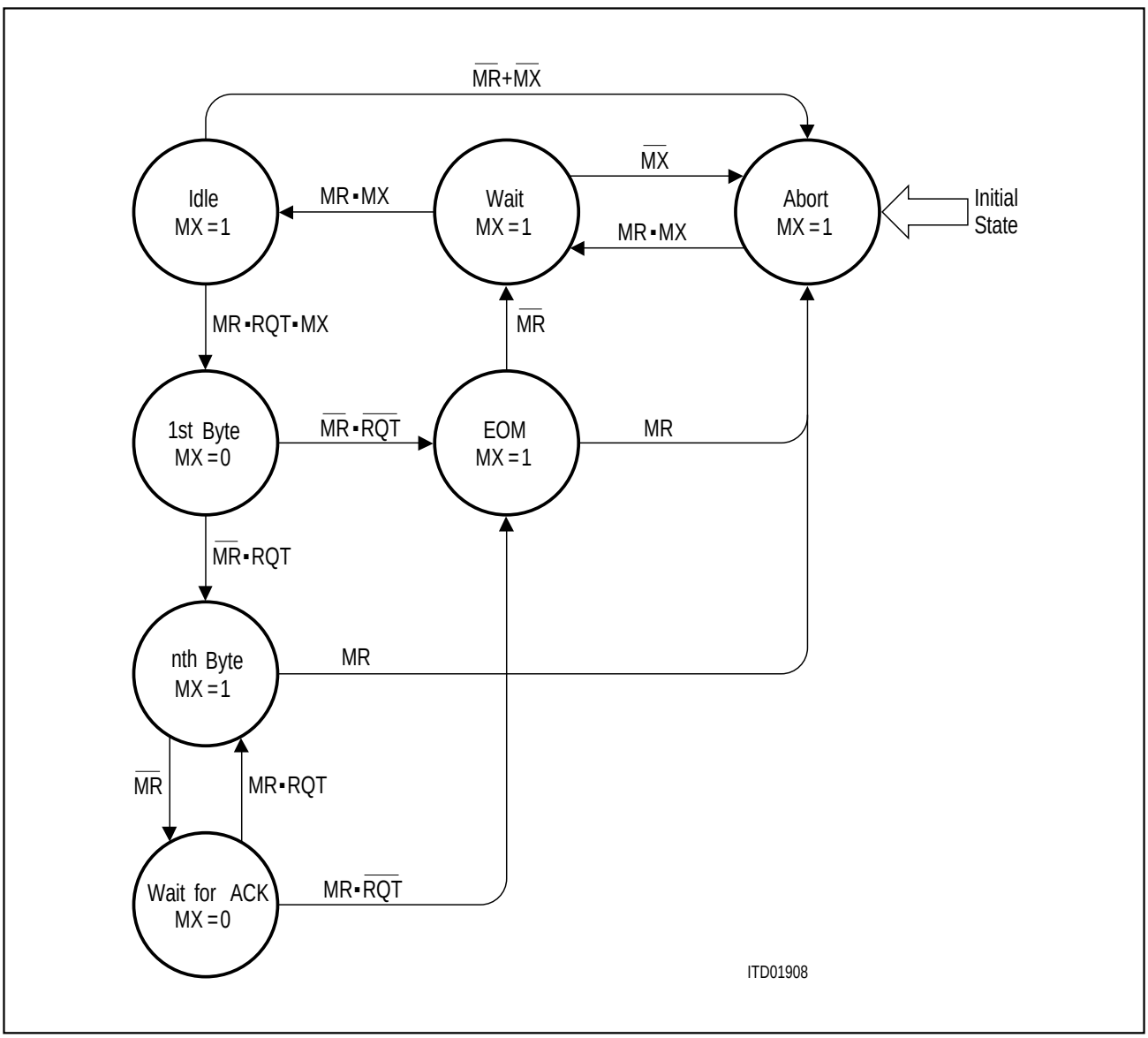


Figure 29
State Diagram of the Monitor Transmitter

3.4.3 Command/Indication Channel 1 (TE Mode)

The C/I-channel bits are represented so that the first bit transmitted/received appears on the left. The data presented to the four peripheral control interface (PCI) pins SA to SD are transparently routed to the C/I IOM-2 channel 1. Pins SA to SD can be configured individually as input or output and the information sent to the pins SA to SD or coming from them will appear respectively in the DD or DU C/I IOM-2 channel 1.

In case a reset has been asserted, the SA to SD pins are programmed as input, however the SA to SD values are not switched to the DU C/I1-channel unless a write command (except NOP) is issued.

The mapping of the peripheral control interface (PCI) pins SA to SD into the six C/I1-channel bits depends on the hardwired AD address (see **section 2.3**) as follows.

AD = 1	7					2	1	0
DD and DU	–	–	SB	SA	SD	SC	MR	MX

AD = 0 (GCR.CAM = 0; two chip mode)								
DD and DU	SD	SC	–	–	–	–	MR	MX

AD = 0 (GCR.CAM = 1; one chip mode)								
DD and DU	SD	SC	SB	SA	–	–	MR	MX

C/I1-Channel (Signaling) Bit Allocation Table

CAM	AD	DD-C/I1						DU-C/I1						PCI-Configuration
		7	6	5	4	3	2	7	6	5	4	3	2	
X	X	X	X	X	X	X	X	H	H	H	H	H	H	after reset
								S	S					
0	0	X	X	X	X	X	X	D	C	H	H	H	H	PCI pins as inputs
		S	S											
0	0	D	C	X	X	X	X	H	H	H	H	H	H	PCI pins as outputs
		S							S					
0	0	D	X	X	X	X	X	H	C	H	H	H	H	PCI pin SC as input PCI pin SD as output
			S					S						
0	0	X	C	X	X	X	X	D	H	H	H	H	H	PCI pin SD as input PCI pin SC as output
										S	S	S	S	
X	1	X	X	X	X	X	X	H	H	B	A	D	C	PCI pins as inputs
				S	S	S	S							
X	1	X	X	B	A	D	C	H	H	H	H	H	H	PCI pins as outputs
					S		S			S		S		
X	1	X	X	X	A	X	C	H	H	B	H	D	H	SB and SD as inputs SA and SC as outputs
				S		S					S		S	
X	1	X	X	B	X	D	X	H	H	H	A	H	C	SA and SC as inputs SB and SD as outputs
								S	S	S	S			
1	0	X	X	X	X	X	X	D	C	B	A	H	H	PCI pins as inputs
		S	S	S	S									
1	0	D	C	B	A	X	X	H	H	H	H	H	H	PCI pins as outputs
		S		S					S		S			
1	0	D	X	B	X	X	X	H	C	H	A	H	H	SA and SC as inputs SB and SD as outputs
			S		S			S		S				
1	0	X	C	X	A	X	X	D	H	B	H	H	H	SB and SD as inputs SA and SC as outputs

X: don’t care
H: passive high

3.5 ARCOFI® Voice/Data Manipulation (VDM)

The ARCOFI offers several possibilities of voice/data manipulation for special applications.

According to the manipulation mode chosen, the byte B1 or B2 (or IC1 or IC2 in the IOM-2 TE mode) can be output via the handset channel and/or the loudspeaker channel.

The following tables give an overview of the different voice/data manipulation modes.

- **PCM-Mode or Normal Mode (DFICR.VDM = 000X):**

DFICR.VDM	AD Pin (IOM®-2) [1]	CMDR.RCM (IOM®-2)	GCR.SLOT (IOM®-2)	Receive Channel	Transmit Channel
0000	0	0	0	–	B1
	0	0	1	–	IC1
	0	1	0	–	B2
	0	1	1	–	IC2
	1	0	0	–	B2
	1	0	1	–	IC2
	1	1	0	–	B1
	1	1	1	–	IC1
0001	0	0	0	B1	B1
	0	0	1	IC1	IC1
	0	1	0	B2	B2
	0	1	1	IC2	IC2
	1	0	0	B2	B2
	1	0	1	IC2	IC2
	1	1	0	B1	B1
	1	1	1	IC1	IC1

[1] This table is given for the IOM-2 two chip mode (GCR.CAM = 0).

- **Linear Mode (DFICR.VDM = 010X):**

This mode exists only in the SDI mode (in the programmed and the following channel) or in the IOM-2 one chip mode (GCR.CAM = 1). The two voice/data channels B1 and B2 (or IC1 and IC2 in the IOM-2 TE mode) are connected to one 16-bit linear channel (2s complement).

DFICR.VDM	AD Pin (IOM®-2)	CMDR.RCM (IOM®-2)	GCR.SLOT (IOM®-2)	Receive Channel	Transmit Channel
0100	–	–	0	–	B1 & B2
	–	–	1	–	IC1 & IC2
0101	–	–	0	B1 & B2	B1 & B2
	–	–	1	IC1 & IC2	IC1 & IC2

B1&B2 (IC1&IC2) means B1 (IC1) byte followed by B2 (IC2) byte (totally 16 bits).

- **Three Party Conferencing Mode (DFICR.VDM = 1000):**

This mode is available only in the SDI mode (in the programmed and the following channel) or in the IOM-2 one chip mode (GCR.CAM = 1).

DFICR.VDM	AD Pin (IOM®-2)	CMDR.RCM (IOM®-2)	GCR.SLOT (IOM®-2)	Receive Channel	Transmit Channel
1000	– –	– –	0 1	B1 + B2 IC1 + IC2	B1, B2 IC1, IC2

B1 + B2 (IC1 + IC2) means the B1 (IC1) and the B2 (IC2) byte are added together (on 8 bits).
B1, B2 (IC1, IC2) means B1 (IC1) and B2 (IC2) byte have the same information.

- **Voice Monitoring Mode (DFICR.VDM = 1100):**

This mode is available only in the SDI mode or in the IOM-2 one chip mode (GCR.CAM = 1). The monitoring chip and the transmission chip must be strapped to a different hardware address (IOM-2: AD/MCLK pin).

The active DU-voice channel of the monitoring chip must be set in the Hi-Z mode (GCR.EVX = 0).

The PCI-port of both chips must be set in the compatible configurations to avoid collision problems in the DU-C/I1 channel.

DFICR.VDM	AD Pin (IOM®-2)	CMDR.RCM (IOM®-2)	GCR.SLOT (IOM®-2)	Receive Channel	Transmit Channel (PZ1)
1100	1/0 1/0 1/0 1/0	0 0 1 1	0 1 0 1	B1D + B1U IC1D + IC1U B2D + B2U IC2D + IC2U	B1 IC1 B2 IC2

Explanations:

–	no signal
B1/B2	voice channels
IC1/IC2	IOM-2 intercommunication channels
B1D/B2D	IOM-2 voice channels (downstream)
B1U/B2U	IOM-2 voice channels (upstream)
IC1D/IC2D	IOM-2 intercommunication channels (downstream)
IC1U/IC2U	IOM-2 intercommunication channels (upstream)

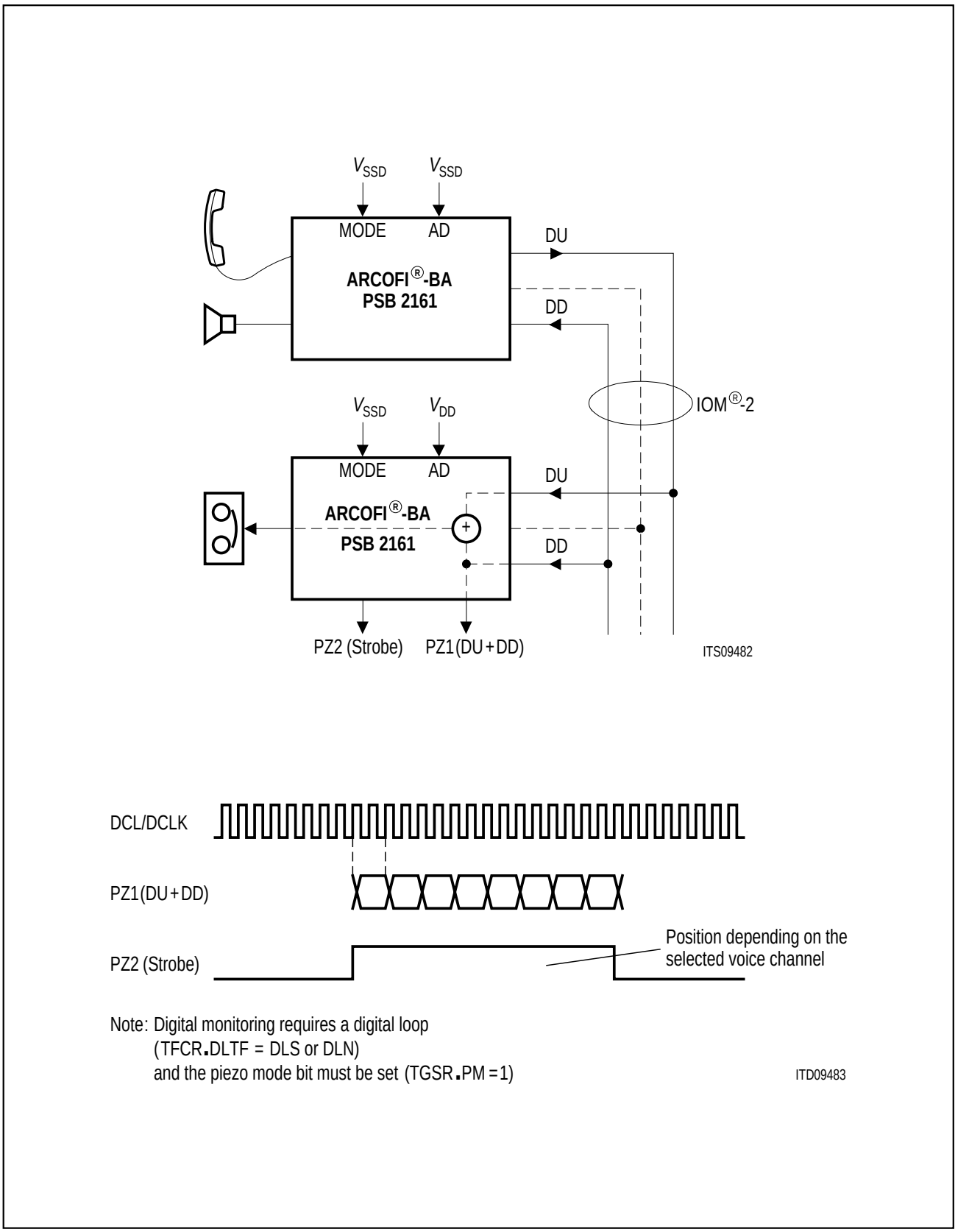


Figure 30
Configuration of the IOM®-2 TE Monitoring Mode

4 Detailed Register Description

The following section describes the various ARCOFI registers and coefficient RAM locations accessible from the terminal equipment microcontroller via the IOM-2 bus or via the serial controller interface (SCI).

A summary of the 13 registers located in the ADI-block is presented below followed by a detailed description of the register content.

Command Register (CMDR)

	7							0
CMDR	R/W	RCM	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

General Configuration Register (GCR)

	7							0
GCR	0	0	0	EVX	SLOT	PU	CAM	LAW

Data Format and Interface Configuration Register (DFICR)

	7							0
DFICR	SD	SC	SB	SA	VDM			

Programmable Filter Configuration Register (PFCR)

	7							0
PFCR	GX	GR	GZ	FX	0	FR	DHPR	DHPX

Tone Generator Configuration Register (TGCR)

	7							0
TGCR	TG	DT	ETF	CG	BT	BM	SM	SQTR

Tone Generator Switch Register (TGSR)

	7							0
TGSR	PM	TRL	0	TRR	DTMF	TRX	0	ERA

AFE Transmit Configuration Register (ATCR)

	7							0
ATCR	MIC				EVREF	0	AIMX	

AFE Receive Configuration Register (ARCR)

	7							0
ARCR	HOC			0	LSC			

Test Function Configuration Register (TFCR)

	7							0
TFCR	0	0	ALTF			DLTF		

SDI Configuration Register (SDICR); only available in SDI mode

	7							0
SDICR	0	0	EPP1	EPP0	DCE	MCLKR		

Time Slot Configuration Register (TSCR); only available in SDI mode

	7							0
TSCR	0	0	TS					

Extended Configuration Register (XCR)

	7							0
XCR	0	0	0	0	DHOP	DHON	DLSP	DLSN

Test Mode Register (TMR)

	7							0
TMR		TM		0	0	0	0	0

4.1 Command Register (CMDR)

Value after reset: BF_H

	7							0
CMDR	R/W	RCM	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

R/W 0: writing to configuration registers or to coefficient RAM
1: reading from configuration registers or from coefficient RAM

RCM **Reverse Channel Mode** (if R/W = 0)
0: receive and transmit in B1 (or IC1 in TE mode)
1: receive and transmit in B2 (or IC2 in TE mode)
For the IOM-2 two chip mode (GCR.CAM = 0), when pin AD is strapped to V_{SS} the above applies. When pin AD is strapped to V_{DD}, RCM operates in the reverse order.

CMDx Address to internal programmable locations

CMD 5	4	3	2	1	0	
0	0	X	X	X	X	code reserved
0	1	X	X	X	X	status operation (SOP)
1	0	X	X	X	X	coefficient operation (COP)
1	1	X	X	X	X	extended operation (XOP)

Coding of Status Operations (SOP):

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	CMD Sequence Description
0	0	0	0	SOP_0	R/W	2	<GCR>
0	0	0	1	SOP_1	R/W	2	<DFICR
0	0	1	0	SOP_2	R/W	2	<PFCR>
0	0	1	1	SOP_3	R/W	2	<TGCR>
0	1	0	0	SOP_4	R/W	2	<TGSR>
0	1	0	1	SOP_5	R/W	2	<ATCR>
0	1	1	0	SOP_6	R/W	2	<ARCR>
0	1	1	1	SOP_7	R/W	2	<TFCR>
1	0	0	0	SOP_8	R/W	2	<SDICR>
1	0	0	1	SOP_9	R/W	2	<TSCR>
1	0	1	0	SOP_A	R/W	2	<XCR>
1	1	0	1	SOP_D	R	2	<IDENT>[1)]
1	1	1	0	SOP_E	R/W	2	<TMR>
1	1	1	1	SOP_F	R/W	9	<TFCR>..<GCR>

[1)] see 3.4.2.1

Coding of Coefficient Operations (COP)

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	CMD Sequence Description	Comments
0	0	0	0	COP_0	R/W	9	<F1> <F1> <G1> <GD1> <T1> <T1> <..> <..>	Tone generator 1
0	0	0	1	COP_1	R/W	9	<F2> <F2> <G2> <GD2> <T2> <T2> <GTR> <GTX>	Tone generator 2 Additional TG gain
0	0	1	0	COP_2	R/W	9	<F3> <F3> <G3> <GD3> <T3> <T3> <FD> <FD>	Tone generator 3 Dual tone
0	0	1	1	COP_3	R/W	5	<K> <A1> <A2> <GE>	frequency
0	1	0	0	COP_4	R/W	5	<TON> <TON> <TOFF> <TOFF>	Tone filter Control generator
0	1	0	1	COP_5	R/W	9	<GX> <GX> <GR> <GR> <..> <..> <..> <..>	Transmit gain Receive gain
0	1	1	0	COP_6	R/W	5	<GZ> <GZ> <..> <..>	Sidetone gain
0	1	1	1	COP_7	R/W	9	<FX1>..<FX8>	
1	0	0	0	COP_8	R/W	9	<FX9>..<FX12> <FR9>..<FR12>	Correction filter FX
1	0	0	1	COP_9	R/W	9	<FR1>..<FR8>	Correction filter FR

Coding of Extended Operations (XOP)

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	Comments
0	0	0	0	XOP_0	W	1	Power-down mode
0	0	0	1	XOP_1	W	1	Power-up mode
1	1	0	1	XOP_D	W	1	DD/DU voice channel swap (toggle function)
1	1	1	0	XOP_E	W	1	Software reset
1	1	1	1	XOP_F	R/W	1	Normal operation (NOP)

4.2 General Configuration Register (GCR)

Value after reset: 00_H

	7							0
GCR	0	0	0	EVX	SLOT	PU	CAM	LAW

EVX **Enable Voice Transmit**
- 0: disable transmit voice data
- 1: enable transmit voice data (if GCR.PU = 0, idle code is transmitted)

SLOT **IOM-2 Slot Select** (IOM-2 TE mode only)
- 0: bearer channels in IOM-channel 0
- 1: bearer channels in IOM-channel 1

PU **Power-Up**
- 0: the ARCOFI is placed in standby mode (power-down); all registers and coefficient RAM contents are saved and all interface functions are available
- 1: the ARCOFI is in a normal operating mode (power-up)

This bit can be directly accessed by the XOP_0/XOP_1 operations.

CAM **Chip Address Mode** (IOM-2 mode only)
- 0: two ARCOFIs are connected to the IOM-2 bus
- 1: only one ARCOFI is connected to the IOM-2 bus

LAW **Coding Law**
- 0: A-Law enabled
- 1: μ-Law enabled

4.3 Data Format and Interface Configuration Register (DFICR)

Value after reset: $F0_H$

	7				0
DFICR	SD	SC	SB	SA	VDM

SD-SA **Signaling I/O** (PCI interface; only available in IOM-2 TE mode)
0: Sx pin programmed as output (x: D, C, B or A)
1: Sx pin programmed as input (x: D, C, B or A)

VDM **Voice Data Manipulation**

Bit 3	2	1	0	Receive Voice Channel	Transmit Voice Channel	Description
0	0	0	0	–	B1	Transmit only
0	0	0	1	B1	B1	Transfer mode
0	1	0	0	–	B1 & B2	16-bit transmit only
0	1	0	1	B1 & B2	B1 & B2	16-bit transfer mode
1	0	0	0	B1 + B2	B1, B2	Conferencing mode
1	1	0	0	B1D + B1U	B1	Monitoring mode

– no signal

Note: In this table above the voice channels indicated are only examples. Other combinations of B1 and B2 (IC1 and IC2 in IOM-2 TE mode) are possible and a complete description is given in section 3.5.

4.4 Programmable Filter Configuration Register (PFCR)

Value after reset: 00_H

	7							0
PFCR	GX	GR	GZ	FX	0	FR	DHPR	DHPX

GX **Transmit Gain**
0: gain set to 0 dB
1: gain coefficients loaded from coefficient RAM (CRAM)

GR **Receive Gain**
0: gain set to 0 dB
1: gain coefficients loaded from CRAM

GZ **Sidetone Gain**
0: gain set to – ∞ dB
1: gain coefficients loaded from CRAM

FX **Transmit Frequency Correction Filter**
0: filter is bypassed
1: filter coefficients loaded from CRAM

FR **Receive Frequency Correction Filter**
0: filter is bypassed
1: filter coefficients loaded from CRAM

DHPR **Disable High-Pass Receive** (50/60 Hz filter)
0: filter enabled
1: filter disabled

DHPX **Disable High-Pass Transmit** (50/60 Hz filter)
0: filter enabled
1: filter disabled

4.5 Tone Generator Configuration Register (TGCR)

Value after reset: 00_H

	7							0
TGCR	TG	DT	ETF	CG	BT	BM	SM	SQTR

TG **Tone Generator**
- 0: tone generator is disabled (if CG = 0)
- 1: tone generator is enabled; frequency and gain coefficients loaded from CRAM; CG has priority over TG

DT **Dual Tone Mode** (DTMF)
- 0: second trapezoid generator is disabled
- 1: second trapezoid generator is enabled; the output signal is added to the S/T signal generator (only if TGSR.DTMF = 0)

ETF **Enable Tone Filter**
- 0: tone filter is by-passed
- 1: tone filter is enabled; filter coefficients loaded from CRAM

CG **Control Generator**
- 0: control generator is disabled
- 1: control generator is enabled; time coefficients loaded from CRAM (tone generator is activated independently of TG-bit setting)

BT **Beat Tone Generator**
- 0: beat tone generator is disabled
- 1: beat tone generator is enabled; time coefficients loaded from CRAM

BM **Beat Mode**
- 0: beat mode is disabled; two tone ring activated when BT-generator is enabled
- 1: beat mode is enabled; three tone ring activated when BT-generator is enabled (only if TGSR.DTMF = 0)

SM **Stop Mode**
- 0: automatic stop mode is disabled
- 1: automatic stop mode is enabled; two and three tone ring gets turned off after the sequence is completed

SQTR **Square/Trapezoid Waveform**
- 0: trapezoid shaped signal is enabled (only if tone ringing via loudspeaker and piezo mode is disabled: TGSR.TRL = 0 & TGSR.PM = 0)
- 1: square-wave signal is enabled

4.6 Tone Generator Switch Register (TGSR)

Value after reset: 00_H

	7							0
TGSR	PM	TRL	0	TRR	DTMF	TRX	0	ERA

PM **Piezo Mode**
- 0: ringing signal is not output to the piezo ring pins
- 1: ringing signal (square) is output to the piezo ring pins PZ1/PZ2

TRL **Tone Ringing via Loudspeaker**
- 0: ringing signal is not output directly to the loudspeaker pins
- 1: ringing signal (square) is output directly to the loudspeaker pins LSP/LSN

TRR **Tone Ringing Receive**
- 0: tone generator for receive direction is disabled
- 1: tone generator for receive direction is enabled

DTMF **DTMF-Generator** (transmit)
- 0: DTMF-generator for transmit direction is disabled
- 1: DTMF-generator for transmit direction is enabled

TRX **Tone Ringing Transmit**
- 0: tone generator for transmit direction is disabled
- 1: tone generator for transmit direction is enabled

ERA **Enhanced Reverse Attenuation**
- 0: standard reverse attenuation in receive direction
- 1: enhanced reverse attenuation in receive direction

4.7 AFE Transmit Configuration Register (ATCR)

Value after reset: 00_H

	7			0
ATCR	MIC	EVREF	0	AIMX

MIC Microphone Control

Bit 7	6	5	4	Selected Mode
0	0	0	0	AMI and PREFI is in **power-down** mode
0	0	0	1	0 dB amplification
0	0	1	0	6 dB amplification
0	0	1	1	12 dB amplification
0	1	0	0	18 dB amplification
0	1	0	1	24 dB amplification
0	1	1	0	30 dB amplification
0	1	1	1	36 dB amplification
1	1	1	1	**bypass** mode, reserved for internal tests

EVREF Enable V_{REF} (2.4-V reference voltage)

0: V_{REF}-buffer is enabled in function of bit GCR.PU (global power-up) and ATCR/ARCR-programming

1: V_{REF}-buffer and internal reference voltage generation are enabled independently of the ARCOFI configuration

AIMX Analog Input Multiplexer

Bit 1	0	Selected Input
0	0	AMI is connected to the pins MIP1/MIN1 (differential input)
0	1	AMI is connected to the pins MIP2/MIN2 (differential input)
1	0	AMI is connected to the pin AXI (single-ended input)
1	1	not used

4.8 AFE Receive Configuration Register (ARCR)

Value after reset: 00_H

	7			0
ARCR	HOC		0	LSC

HOC Handset Output Control

Bit 7	6	5	Selected Mode
0	0	0	AHO is in **power-down** mode
0	0	1	2.5 dB amplification
0	1	0	– 3.5 dB amplification
0	1	1	– 9.5 dB amplification
1	0	0	– 15.5 dB amplification
1	0	1	– 21.5 dB amplification
1	1	1	**bypass** mode, reserved for internal tests

LSC Loudspeaker Output Control

Bit 3	2	1	0	Selected Mode
0	0	0	0	ALS is in **power-down** mode
0	0	0	1	11.5 dB amplification
0	0	1	0	8.5 dB amplification
0	0	1	1	5.5 dB amplification
0	1	0	0	2.5 dB amplification
0	1	0	1	– 0.5 dB amplification
0	1	1	0	– 3.5 dB amplification
0	1	1	1	– 6.5 dB amplification
1	0	0	0	– 9.5 dB amplification
1	0	0	1	– 12.5 dB amplification
1	0	1	0	– 15.5 dB amplification
1	0	1	1	– 18.5 dB amplification
1	1	0	0	– 21.5 dB amplification
1	1	1	1	**bypass** mode, reserved for internal tests

4.9 Test Function Configuration Register (TFCR)

Value after reset: 00_H

	7			0
TFCR	0	0	ALTF	DLTF

ALTF **Analog Loop** and **Test Functions**

Bit 5	4	3	Test Function
0	0	0	NOT: No Test Mode
0	0	1	ALF: Analog Loop via Front End
0	1	0	ALC: Analog Loop via Converter
0	1	1	ALN: Analog Loop via Noise Shaper
1	0	0	ALI: Analog Loop via Interface

DLTF **Digital Loop** and **Test Functions**

Bit 2	1	0	Test Function
0	0	0	NOT: No Test Mode
0	0	1	IDR: Initialize DRAM
0	1	0	DLP: Digital Loop via PCM-Register
0	1	1	DLS: Digital Loop via Signal Processor
1	0	0	DLN: Digital Loop via Noise Shaper

4.10 SDI Configuration Register (SDICR); SDI mode only

Value after reset: 00_H

	7					0
SDICR	0	0	EPP1	EPP0	DCE	MCLKR

EPP0 **Enable Push-Pull** at pin DU/DX (SDI mode only)
0: open drain enabled
1: push-pull enabled

EPP1 **Enable Push-Pull** at pin SDR/SDX (SDI mode only)
0: open drain enabled
1: push-pull enabled

DCE **Double Clock Enable** for DCLK (SDI mode only)
0: single clock rate
1: double clock rate

MCLKR **Master Clock Rate** (synchronized system clock)

Bit 2	1	0	MCLK Clock Rate
0	0	0	512 kHz
0	0	1	1.536 MHz
0	1	0	2.048 MHz
0	1	1	4.096 MHz
1	0	0	16.384 MHz (test mode)

4.11 Time Slot Configuration Register (TSCR); SDI mode only

Value after reset: 00_H

	7							0
TSCR	0	0	TS					

TS Time Slot Selection

Bit 5	4	3	2	1	0	Time Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
		.				.
		.				.
1	1	1	1	1	1	63

4.12 Extended Configuration Register (XCR)

Value after reset: 00_H

	7							0
XCR	0	0	0	0	DHOP	DHON	DLSP	DLSN

DHOP **Disable HOP** Amplifier
0: HOP amplifier normal mode
1: Disable HOP amplifier (power-down, output high impedance)

DHON **Disable HON** Amplifier
0: HON amplifier normal mode
1: Disable HON amplifier (power-down, output high impedance)

DLSP **Disable LSP** Amplifier
0: LSP amplifier normal mode
1: Disable LSP amplifier (power-down, output high impedance)

DLSN **Disable LSN** Amplifier
0: LSN amplifier normal mode
1: Disable LSN amplifier (power-down, output high impedance)

4.13 Test Mode Register (TMR)

Value after reset: 00_H

	7							0
TMR		TM		0	0	0	0	0

TM **Test Mode** (only for internal tests)
000: normal mode

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Ambient temperature under bias	T_A	– 25	80	˚C
Storage temperature	T_{STG}	– 65	125	˚C
Input/output voltage on any pin with respect to ground	V_S	– 0.3	V_{DD} + 0.3	V
Maximum voltage on any pin with respect to ground	V_{max}		7	V

ESD-integrity (according MIL-Std 883D, method 3015.7): 1000 V
exception: The pins #14, #16, #17 and #18 are not protected against voltage stress > 630 V (versus VSSx, x = A, D, P). The output performance prohibits the use of adequate protective structures.

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

DC-Characteristics

V_{DD}/V_{DDP} = 5 V ± 5 %; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 ˚C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input leakage current	I_{IL}	– 1.0		1.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
H-input level (except pins SCLK, MCLK, DCLK)	V_{IH1}	2.0		V_{DD} + 0.3	V	
L-input level (except pins SCLK, MCLK,DCLK)	V_{IL1}	– 0.3		0.8	V	
H-input level (pins SCLK, MCLK, DCLK)	V_{IH2}	0.7 V_{DD}		V_{DD}	V	
L-input level (pins SCLK, MCLK, DCLK)	V_{IL2}	0		0.3V_{DD}	V	
H-output level (except pins PZ1/PZ2)	V_{OH1}	2.4			V	I_O = – 400 µA

DC-Characteristics (cont'd)

V_{DD}/V_{DDP} = 5 V ± 5 %; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
H-output level (pins PZ1/PZ2)	V_{OH2}	V_{DD} – 0.45			V	I_O = – 2 mA
L-output level (except pin DU)	V_{OL1}			0.45	V	I_O = 2 mA
L-output level (pin DU, DD[1])	V_{OL2}			0.45	V	I_O = 7 mA
V_{DD} supply current standby (IOM-2 TE)	I_{DDS1}		300	600	µA	V_{DD} = 5 V; DCL = ON
	I_{DDS2}		10	50	µA	DCL = OFF; reset state
V_{DD} supply current operating (IOM-2 TE) [2]	I_{DDO1}		12	18	mA	V_{DD} = 5 V emergency ringing via ALS (TGSR.TRL = 1)
	I_{DDO2}		13	19	mA	handset mode (ARCR.HOC = 010_B)
Input capacitance	C_I			10	pF	
Output capacitance	C_O			15	pF	

1) If voice channel swap (XOP_D) is enabled

2) Operating power dissipation is measured with all analog outputs open.
All analog inputs are set to VREF.
The digital input signal (pin DD) is set to an idle code.
For the emergency ringing mode, the tone generator is set to 400-Hz single tone (square).
In this mode the loudspeaker amplifier is set to – 3.5 dB (3.2 Vpp)

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

AC-Characteristics

Inputs are driven to 2.4 V for a logical “1” and to 0.45 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and 0.8 V for a logical “0”. The AC-testing input/output waveforms are shown below.

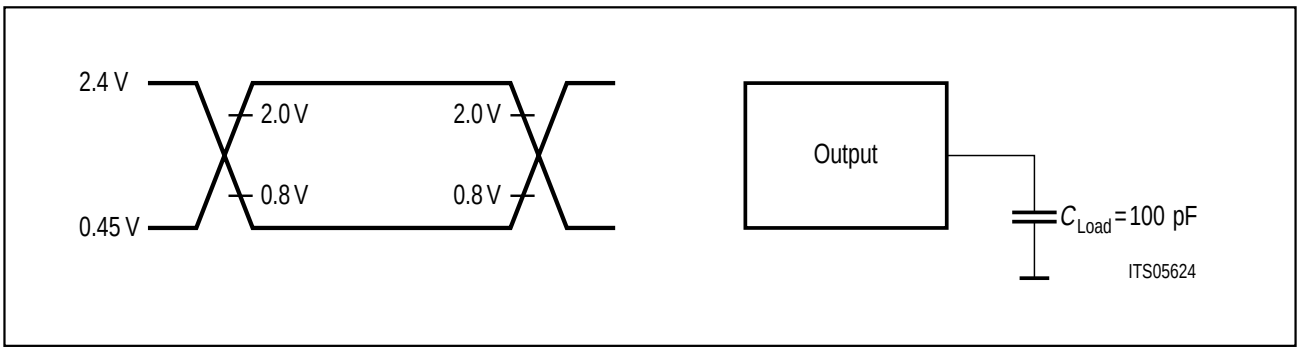


Figure 31
Input/Output Waveforms for AC-Tests

Analog Front End Input Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ	max.		
AMI-input impedance	Z_{AMI}	15			kΩ	300 – 3400 Hz
AMI-input voltage swing	V_{AMI}			38.1	mVpk	36 dB
AMI-gain	G_{AMI}			42	dB	9.55 mV at 1 kHz

Analog Front End Output Characteristics

AHO-output impedance	Z_{AHO}			2	Ω	300 – 3400 Hz
AHO-output voltage swing [1)]	V_{AHO}		3.2		Vpk	Load measured from HOP to HON
AHO-output high voltage [1)]	V_{AHO}		3.2		Vpk	input load – 1 mA @ HOP/HON
AHO-output low voltage [1)]	V_{AHOL}		3.2		Vpk	input load + 1 mA @ HOP/HON
ALS-output impedance	Z_{ALS}			2	Ω	300 – 3400 Hz
ALS-output voltage swing	V_{ALS}		3.2		Vpk	Load measured from LSP to LSN
ALS-output high voltage [1)]	V_{ALSH}		3.08		Vpk	input load – 60 mA @ LSP/LSN
ALS-output low voltage [1)]	V_{ALSL}		3.08		Vpk	input load + 60 mA @ LSP/LSN
V_{REF} output impedance	Z_{VREF}			2	Ω	Load measured from V_{REF} to V_{SSA}
V_{REF} output voltage	V_{VREF}	2.35		2.45	V	input load – 2 mA @ V_{REF}

[1)] The maximum output voltage swing corresponds to the maximum incoming PCM-code (± 127)

Transmission Characteristics

V_{DD}/V_{DDP} = 5 V ± 5 %; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 ˚C

Parameter	Limit Values		Unit	Test Condition
	min.	max.		
Attenuation Distortion @ 0 dBm0	0 – 0.25 – 0.25 – 0.25 – 0.25 0	 0.25 0.45 0.9 	dB dB dB dB dB dB	< 200 Hz 200 – 300 Hz 300 – 2400 Hz 2400 – 3000 Hz 3000 – 3400 Hz > 3400 Hz
Out-of-band signals		 – 35 – 45 – 45 – 65 – 35 – 40	 dB dB dB dB dB dB	receive (TGSR.ERA=0): 4.6 kHz 8.0 kHz receive(TGSR.ERA=1): 4.6 kHz 8.0 kHz transmit: 4.6 kHz 8.0 kHz
Group delay distortion @ 0 dBm0 [1)]		 750 380 130 750	 µs µs µs µs	TGSR.ERA=0 500 – 600 Hz 600 – 1000 Hz 1000 – 2600 Hz 2600 – 2800 Hz
Signal-to-total distortion (method 2, sinewave 1kHz)	35 29 24		dB dB dB	0 to – 30 dBm0 – 40 dBm0 – 45 dBm0
Gain tracking (method 2) @ – 10 dBm0	– 0.3 – 0.6 – 1.6	0.3 0.6 1.6	dB dB dB	3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0
Idle-channel noise		– 75 – 66	dBm0 dBm0	receive (A-Law; Psoph.) transmit (A-Law; Psoph.)
Cross-talk		– 66	dB	Reference: 0 dBm0

Transmission Characteristics (cont'd)

V_{DD}/V_{DDP} = 5 V ± 5 %; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 °C

Parameter	Limit Values		Unit	Test Condition
	min.	max.		
Programmable AFE gain	– 0.5	0.5	dB	step accuracy
	– 1.0	1.0	dB	overall accuracy
Overall programming range (With specified transmission characteristics)				Receive:
	– 21.5	11.5	dB	loudspeaker
	– 21.5	2.5	dB	earpiece
				Transmit:
	0	36	dB	differential inputs
	0	24	dB	single ended input

[1] Delay measurements include delays through the A/D and D/A with all features filters FX, GX, FR and GR disabled.

IOM®-2 Bus Switching Characteristics

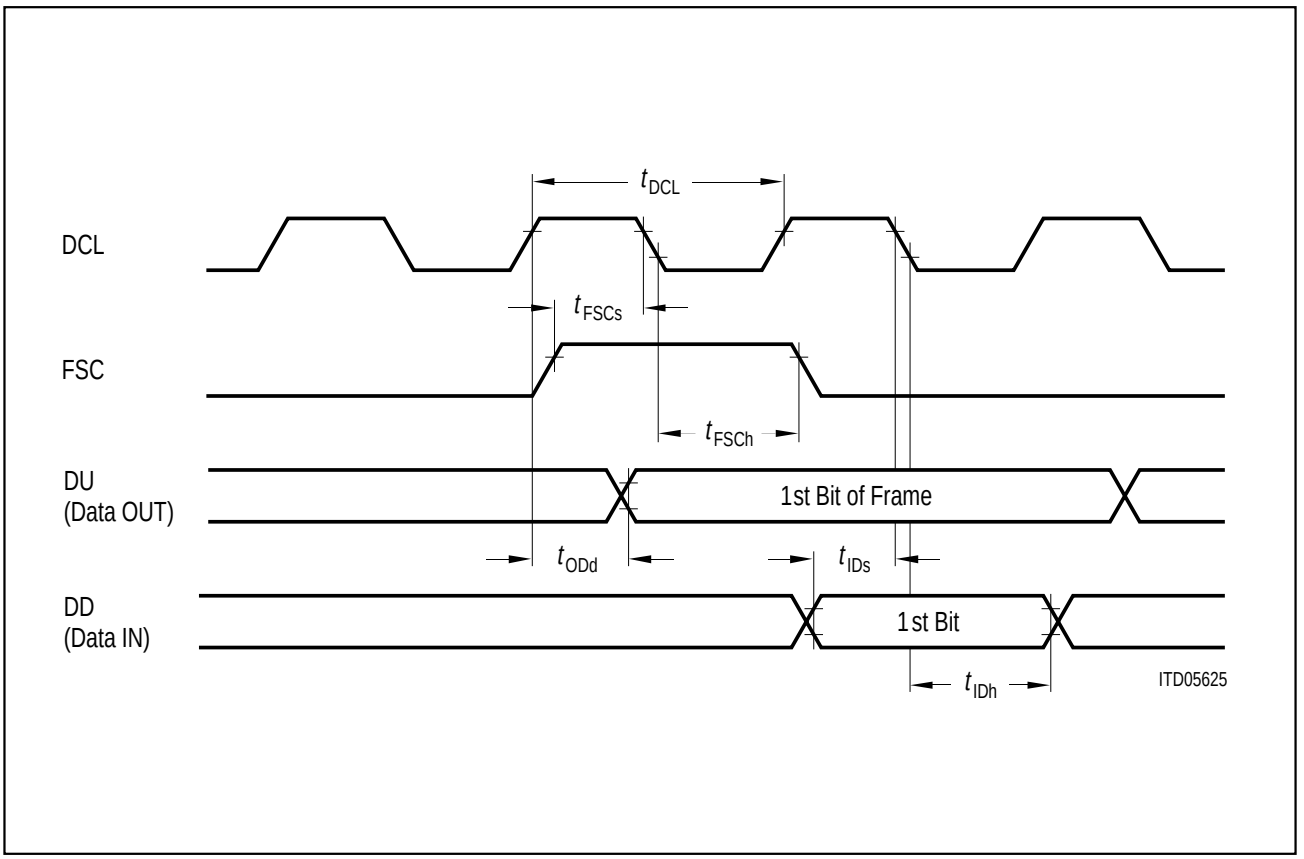


Figure 32
IOM®-2 Bus Timing Diagram

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCL-clock period [1]	t_{DCL}		651		ns
DCL-clock period [2]	t_{DCL}		244		ns
DCL-duty cycle		30	50	70	%
FSC-period	t_{FSC}		125		µs
FSC-setup time	t_{FSCs}	70			ns
FSC-hold time	t_{FSCh}	40			ns
DD-data-in setup time	t_{IDs}	50			ns
DD-data-in hold time	t_{IDh}	50			ns
DU-data-out delay	t_{ODd}			150	ns

1) 768 kbit/s (IOM-2 TE Mode); max. jitter of ±160 ns once in FSC-period.

2) 2048 kbit/s (IOM-2 Non-TE Mode).

PCI-Switching Characteristics (IOM®-2 TE-Mode)

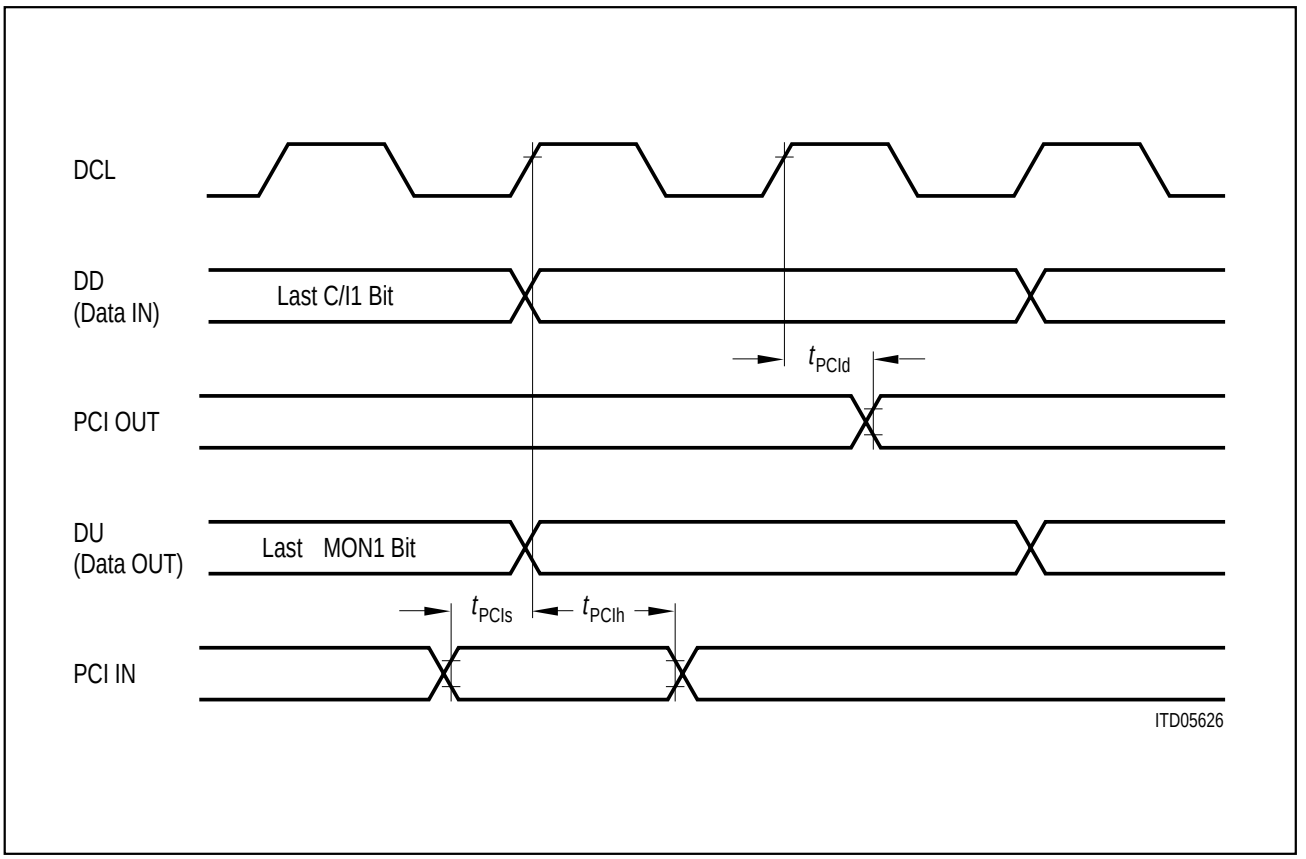


Figure 33
IOM®-2 Bus Timing Diagram (TE-Mode)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PCI-data-out delay	t_{PCId}		350	ns
PCI-data-in setup time	t_{PCIs}	50		ns
PCI-data-in hold time	t_{PCIh}	100		ns

SCI-Switching Characteristics

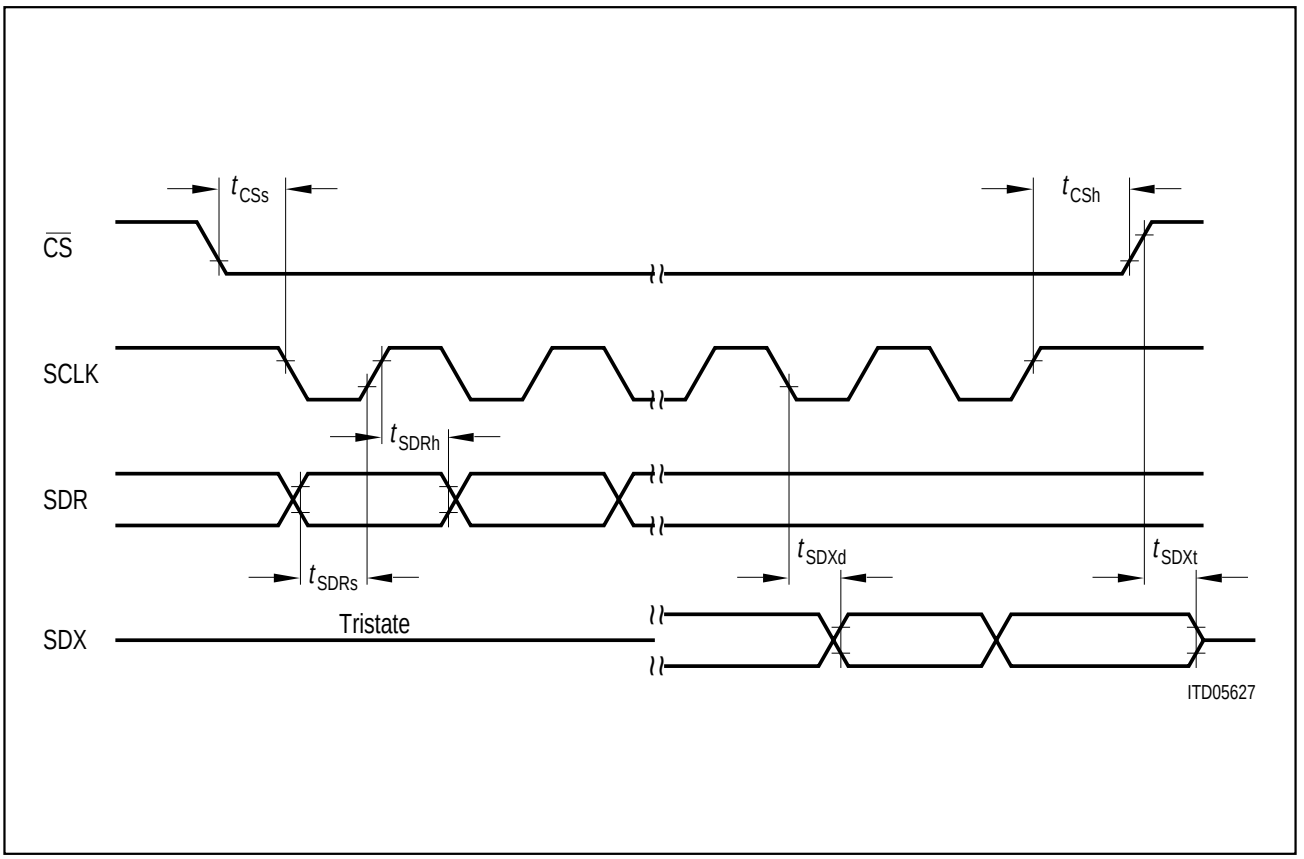


Figure 34
SCI-Switching Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
SCLK-frequency	f_{SCLK}		2048	kHz
Chip Select setup time	t_{CSs}	0		ns
Chip Select hold time	t_{CSh}	0		ns
SDR-setup time	t_{SDRs}	50		ns
SDR-hold time	t_{SDRh}	50		ns
SDX-data-out delay	t_{SDXd}		150	ns
SDX $\overline{CS}$ high to tristate	t_{SDXt}		30	ns

SDI-Switching Characteristics

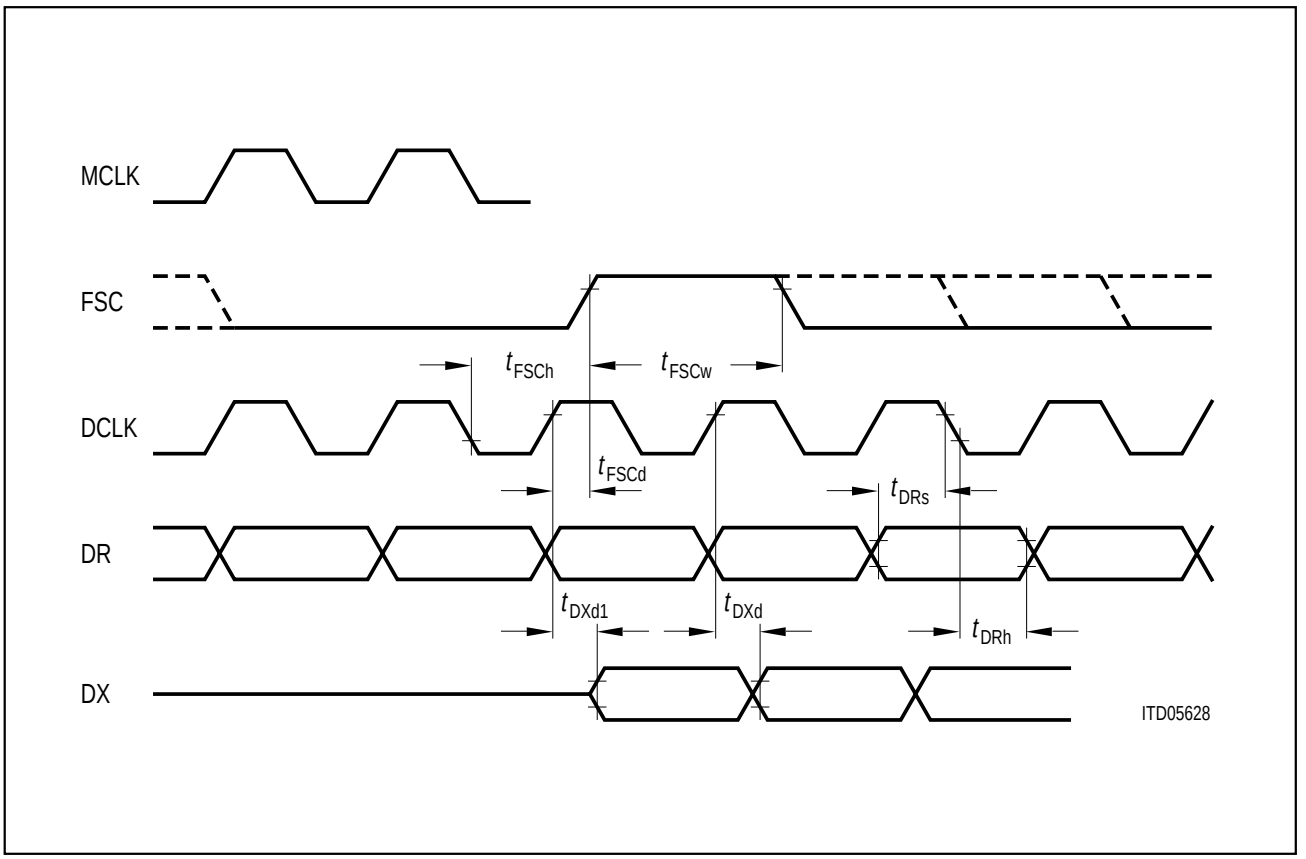
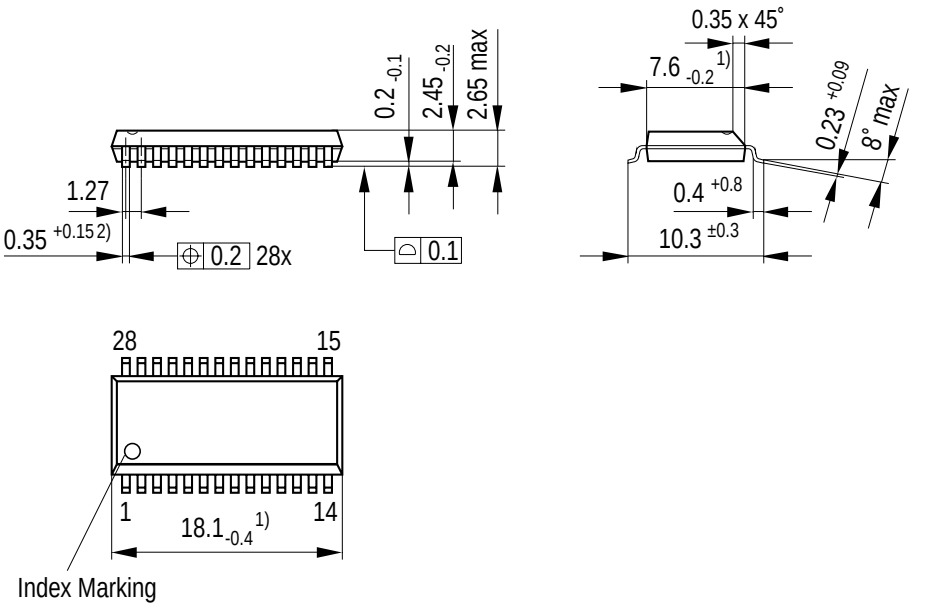


Figure 35
SDI-Switching Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
MCLK-frequency	f_{MCLK}	512	4096	kHz
DCLK-frequency	f_{DCLK}	64	4096	kHz
FSC-pulse width	t_{FSCw}	40		ns
FSC-hold time from DCLK low	t_{FSCh}	30		ns
FSC-delay time	t_{FSCd}		30	ns
DR-setup time	t_{DRs}	50		ns
DR-hold time	t_{DRh}	50		ns
DX-data-out delay (t_{FSCd} < 0 ns)	t_{DXd1}		80	ns
DX-data-out delay ($t_{FSCd} \geq 0$ ns)	t_{DXd1}		80 + t_{FSCd}	ns
DX-data-out delay	t_{DXd}		80	ns

6 Package Outlines

P-DSO-28-1
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusions of 0.15 max rer side
2) Does not include dambar protrusion of 0.05 max per side

GPS05123

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”
SMD = Surface Mounted Device

Dimensions in mm

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ICs for Communications

Audio Ringing Codec Filter
ARCOFI®-BA

PSB 2161

Layout and Wiring Recommendations

Application Note 06.96

PSB 2161 Revision History: Current Version: 1996-06-01		
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Table of Contents **Page**

7 Application Note – Layout and Wiring Recommendations

7.1 Introduction

The ARCOFI-BA PSB 2161 is a high performance codec filter device with high gain analog amplifiers. To obtain the full performance of the device, some care in designing the analog circuitry and the printed circuit board has to be taken. This application note gives some hints and wants to provide understanding of the parameters that influence the performance.

With “performance”, especially the following effects are meant:

- Signal to noise ratio, especially in transmit direction (analog to digital)
- Idle channel noise (the noise that is present when there is no signal applied)
- Spurious oscillations
- Sensitivity to any kind of interfering signals (noise on power supply, RF interference, induced voltages etc.)

The ARCOFI-BA contains high performance A/D and D/A converters with more than 16 bit resolution in order to allow the different signal processing steps without degradation of the signals themselves. On one silicon the PSB 2161 integrates a high gain, analog preamplifier, the oversampling converters as well as an digital signal processor. Besides the ARCOFI-BA is used in an digital environment that typically causes noise on the power supply and produces many kinds of interfering signals. For all these reasons, careful grounding, decoupling, and shielding is the key to get best system performance.

Note: The circuits given in this application note are for general guidance and do not claim to satisfy all user specific requirements. Especially for EMC reasons additional components may be required.

7.2 Layout Considerations

Decoupling at Power Supply Pins

The PSB 2161 has three ground pins and two pins for connecting the positive supply voltage. Internally all the ground pins and all the power supply pins are connected. From **table 1** it can be seen, what parts of the ARCOFI-BA are supplied from what pins. It is important, that each pair of pins given in one row of **table 1** is decoupled with a pair of capacitors in parallel. One capacitor has to be a 47 nF … 100 nF ceramic one, for the second one a tantalum type with 1 µF … 10 µF is recommended.

Table 1
Power Supply Pins of the PSB 2161

Pin for V_{SS}	Pin for V_{DD} (+ 5 V)	Supply for
1 (V_{SSD})	21 (V_{DD})	Digital signal processor and digital interface
15 (V_{SSP})	13 (V_{DDP})	Analog output amplifier AHO, ALS
20 (V_{SSA})	21 (V_{DD})	Analog preamplifiers and switches

Note, that pin 21 (V_{DD}) is used for both, the supply of the DSP and the supply of the analog part of the ARCOFI-BA except the power amplifiers AHO and ALS.

Blocking the Reference Voltage

The reference voltage pin V_{REF} of the PSB 2161 has to be blocked with a capacitor of at least 100nF to the analog ground. Therefore this capacitor is required between pin 19 (V_{REF}) and 20 (V_{SSA}). It has to be placed close to these pins.

Grounding

A second aspect in designing a good PCB layout is a well defined ground connection. This concerns the three ground pins of the ARCOFI-BA (pin 1, 15, 20). These three ground pins have to be connected to each other either directly via a big ground plane underneath the PSB 2161 or via separate wires that lead to a central ground point of the system. In the latter case care must be taken that the three single ground wires carry only the current for the ARCOFI-BA itself.

The ground connection of e.g. low-level microphone signals should be made directly to the pin V_{SSA} which serves as ground for the microphone preamplifier.

In general, any kind of ground loop must be avoided since this would be an antenna for RF noise. Note also the position of the decoupling capacitor for the reference voltage between pin 19 and 20 in **figure 38b**. It should be placed close to pin 19 and 20.

7.3 Connecting the Analog Front End

7.3.1 Outputs for Earpiece and Loudspeaker

The analog handset output amplifier AHO delivers a symmetrical signal at the pins HOP and HON. Any load with an impedance higher than 200 Ω can be connected directly (see **figure 36a**). However, if the load shows a strong capacitive behavior like a piezo-ceramic earpiece, it is better to use series resistors as shown in **figure 36b** to avoid spurious oscillations. This is also an typical example for a circuitry as it is used in a real application. The resistors have to be placed close to the output pins.

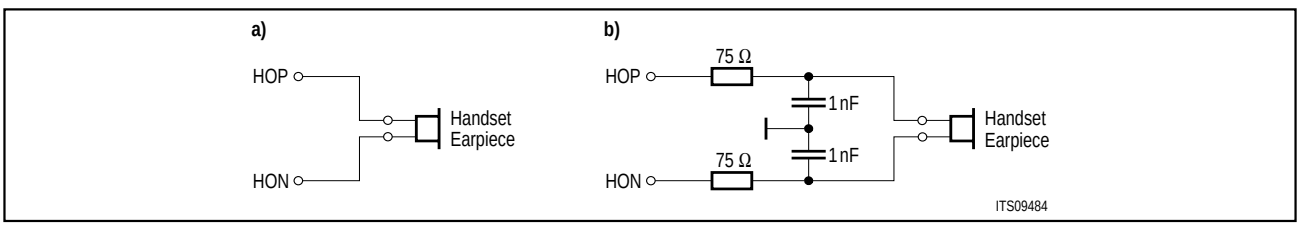

Figure 36
The Analog Handset Output

It is possible to use the outputs HOP and HON as single ended outputs with reference to ground; the load must be greater than 100 Ω and only half of the amplitude swing is available.

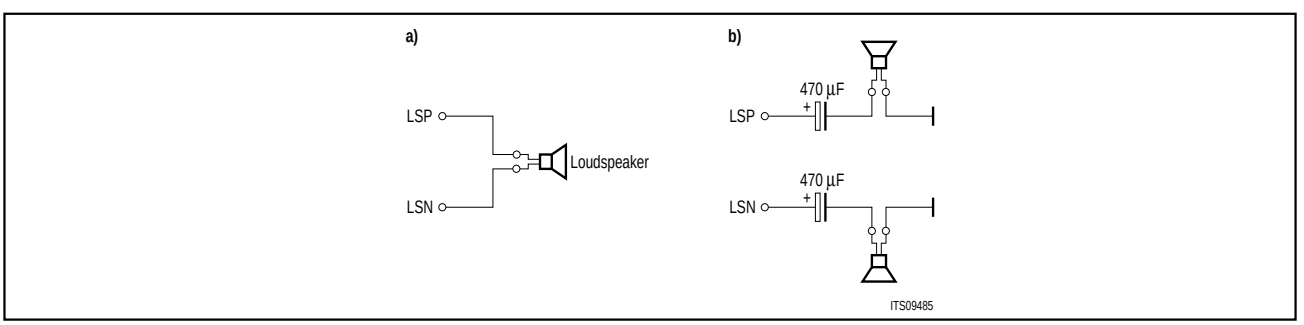

Figure 37
The Analog Loudspeaker Output

The main difference between the earpiece output and the loudspeaker output is the driver capability. The load between the pins LSP and LSN may be as low as 50 Ω in order to drive a speaker. A dynamic speaker can be connected directly to these pins (see **figure 37a**). An arrangement for an unsymmetrical connection with two speakers shows **figure 37b**. The load can be 25 Ω but should be decoupled to avoid DC currents through the speakers. With the register bits **XCR.DLSP** and **XCR.DLSN** each output pin can be switched into a high impedance state therefore the speakers can be switched on and off independently. The same applies for the earpiece output with HOP and HON. This feature offers a variety of applications. For example, if one speaker in **figure 37b** is left out, the output pin becomes a switchable line level output. For example, this output could control an external speaker box.

7.3.2 Differential Microphone Inputs

The ARCOFI-BA offers five pins as microphone inputs. The two differential inputs MIN1/MIP1 and MIN2/MIP2 are equivalent in terms of performance and circuitry. The single ended input MI3 offers a slightly reduced performance due to its unsymmetrical structure. All inputs can be used to interface directly with all kinds of microphones or serve as a high level input. Unused microphone inputs can be left open or tied to V_{REF}.

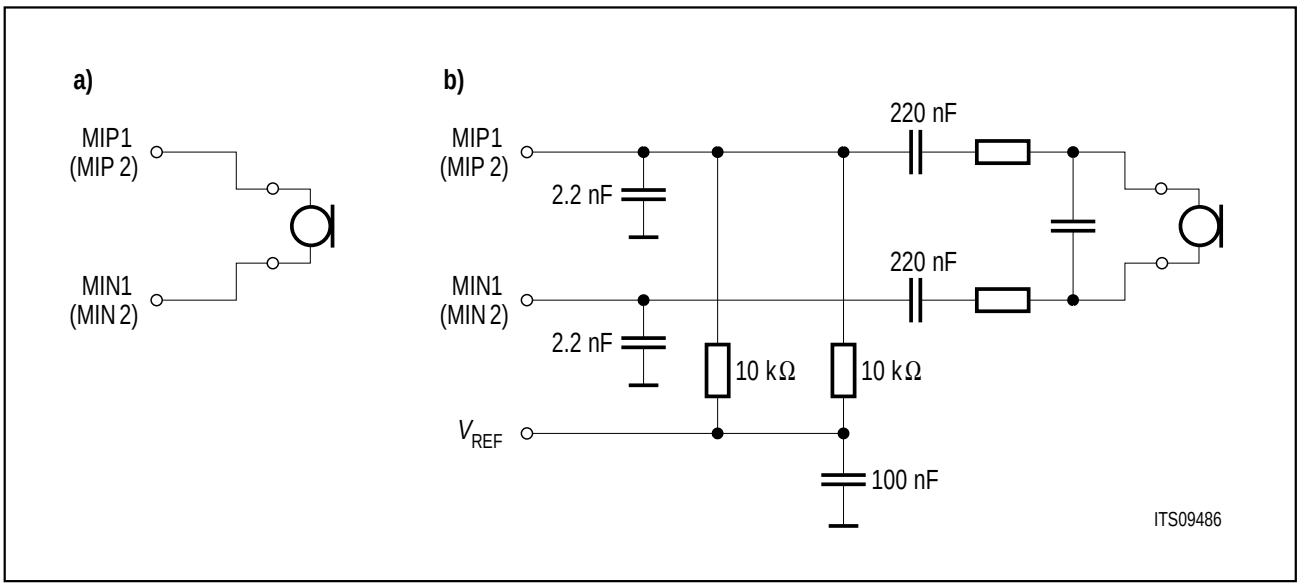

Figure 38
Interfacing Symmetrical Microphones

A symmetric signal source that has no reference to ground can simply be connected to one of the differential inputs. Basically, no additional components are required (**figure 38a**). The microphone can be a dynamic, magnetic, or piezoelectric one. Usually an arrangement similar to the one shown in **figure 38b** will be used in order to get well defined impedances and a EMC/ESD protection. The component values depend on the type of microphone used.

The microphone inputs are biased internally with V_{REF} and require no external biasing. However, a DC path can be helpful in order to avoid any static charging of the input pins while they are unused (not active). Therefore the two 10 kΩ resistors in **figure 38b** are introduced. The input impedance at the single pins MIN, MIP, MI3 is higher than 15 kΩ.

Electret Microphones

Today, electret microphones are widely used in telecommunications devices. These microphones usually contain an active amplifier or a FET to achieve a low output impedance and therefore require some DC biasing.

The DC current to bias the electret microphone can be taken from the positive supply voltage of the ARCOFI-BA (+ 5 V) or the reference voltage V_{REF} can be used for this purpose (2.4 V). The schematic in **figure 39** depicts the first possibility.

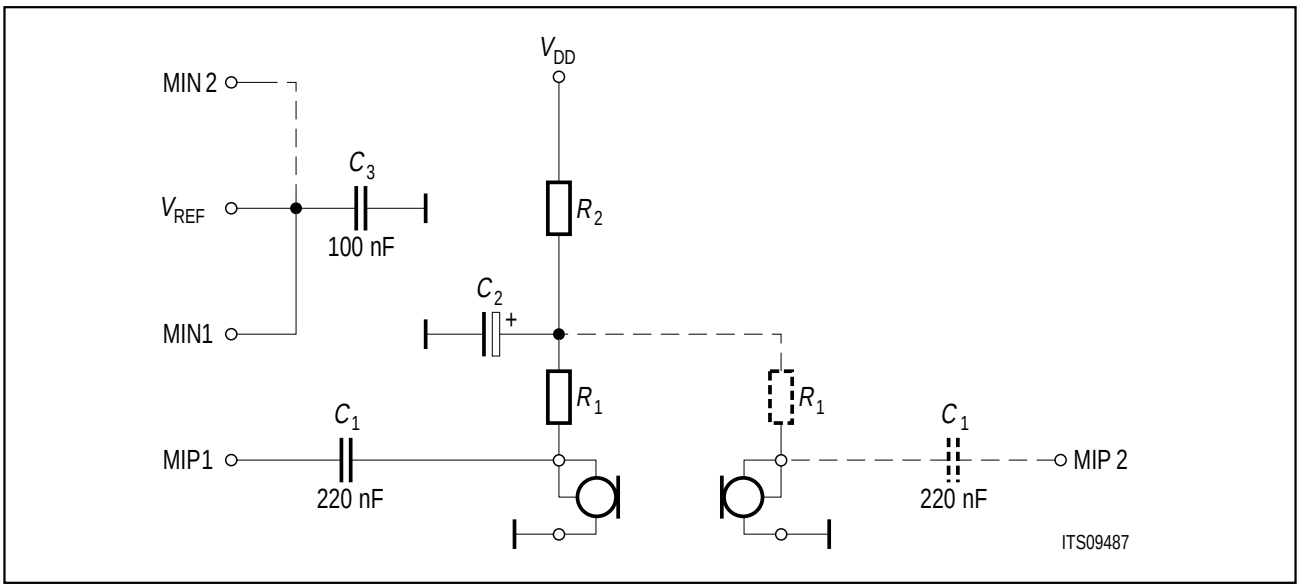

Figure 39
Interfacing Electret Microphones with Bias from V_{DD}

One input pin (MIN1) of the differential input is tied to V_{REF}. This creates a single ended configuration which must be AC coupled with C1 to the signal source, consisting of the electret microphone. R1 and R2 are used to bias the microphone. The RC combination R2/C2 filters out power supply ripple. R1 has the value recommended by the microphone manufacturer and is usually in the range of 1 kΩ … 4 kΩ.

The dashed line in **figure 39** illustrates how to connect a second microphone to the other differential input of the ARCOFI-BA without spending the complete bias network again.

The second possibility to bias electret microphones is shown in **figure 40**. The DC current is taken directly from the V_{REF} pin of the ARCOFI-BA. No RC network to filter out power noise is necessary because the reference voltage is clean and stable. Only in case of high gains in the analog microphone amplifier (AMI more than 30 dB) the overall performance can be improved, if the reference voltage is filtered. For this purpose, a R/C combination (1 kΩ/10 µF) between the V_{REF} pin and the resistors R1 in **figure 40** can be inserted. An application incorporating this RC element shows **figure 41**.

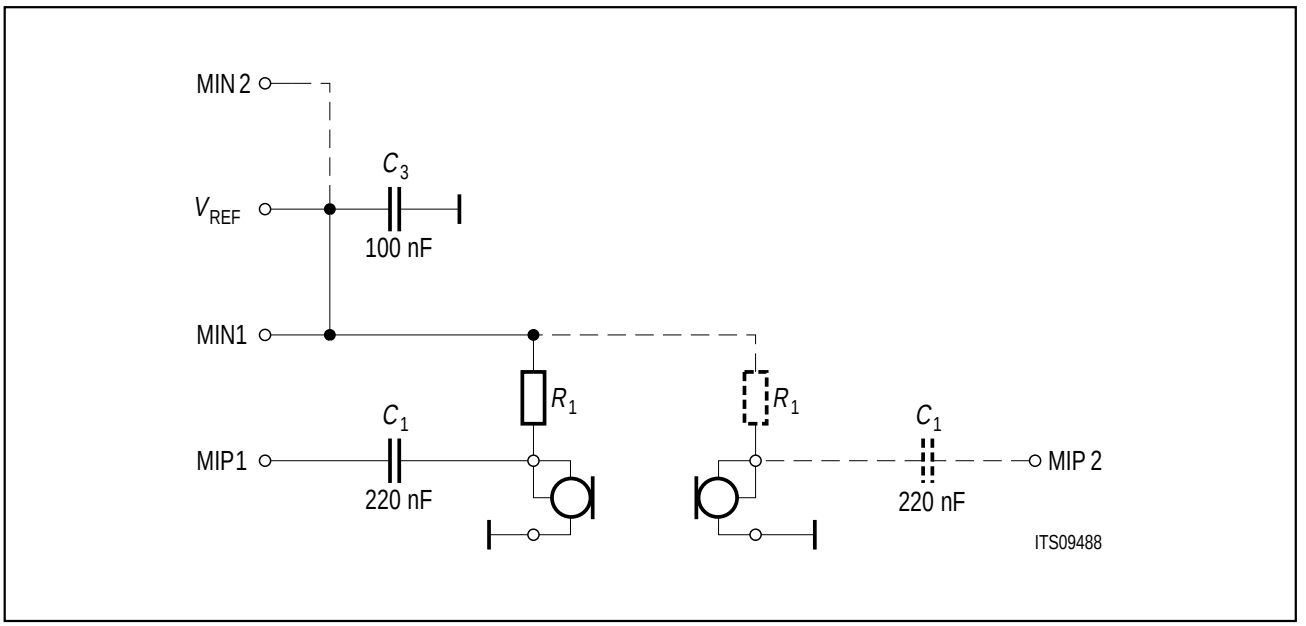

Figure 40
Interfacing Electret Microphones with Bias from V_{REF}

The solutions for connecting microphones shown in **figure 39** and **40** contain a minimum of components to explain the principle. A solution that comes closer to a real application can be seen in **figure 41**. The microphone is biased from the V_{REF} pin.

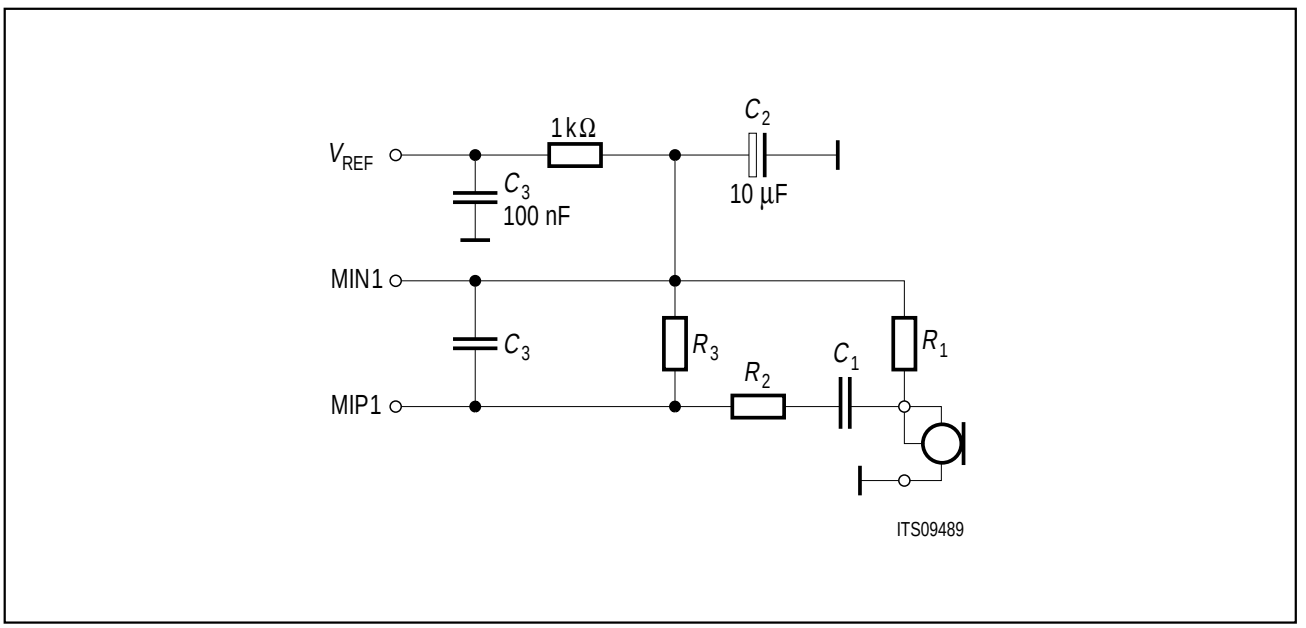

Figure 41
Example For a Typical Application

With the help of R3/C3 a well defined input impedance is achieved. If R2 is inserted, a high frequency cut-off can be realized. The 1 k/10 µF combination is used to filter the reference voltage (improved idle channel noise with AMI > 30 dB).

Especially if an electret microphone is connected via a longer cable or if high noise immunity is desired, the circuity from **figure 42** is suitable. The microphone is not directly connected to ground but with two feeding resistors R_F.

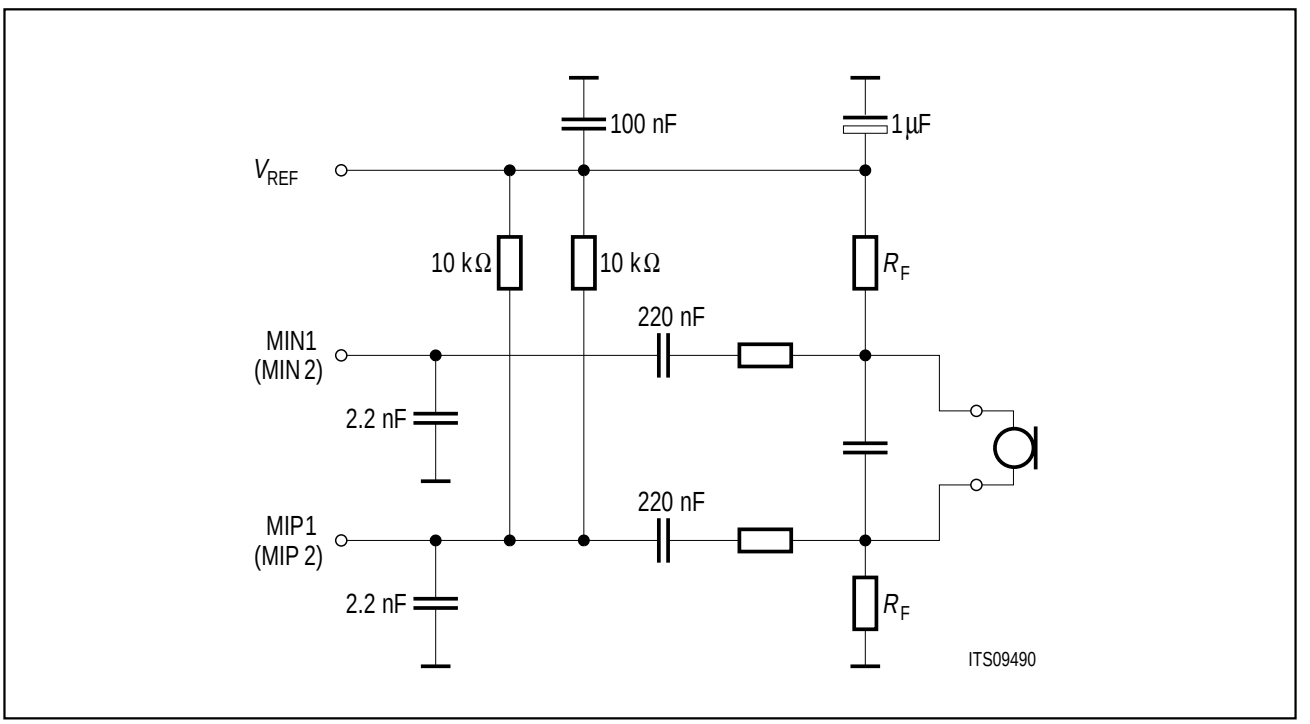

Figure 42
Symmetrical Biasing of an Electret Microphone

7.3.3 The Single Ended Input MI3

The single ended input MI3 behaves like one of the differential input pins, in case of one input of the differential inputs is tied to V_{REF}. Therefore the application examples in **figure 43** introduces no new ideas. An electret microphone can be biased from V_{DD} (**figure 43a**) or from the V_{REF} pin (**figure 43b**). Any symmetric signal source with no reference to ground should be connected between the MI3 pin and the V_{REF} pin (**figure 43c**). Often MI3 is used as a additional input e.g. for separate microphones with their own preamplifiers. Such high-level signal sources could be connected to MI3 as shown in **figure 43d**.

In general, if only two inputs are required, it is advisable to use MIN1/MIP1 and MIN2/MIP2 for this purpose. They exhibit a slightly better performance because of their differential nature. When the input source is referred to ground, the gain for the input MI3 should not exceed 24 dB.

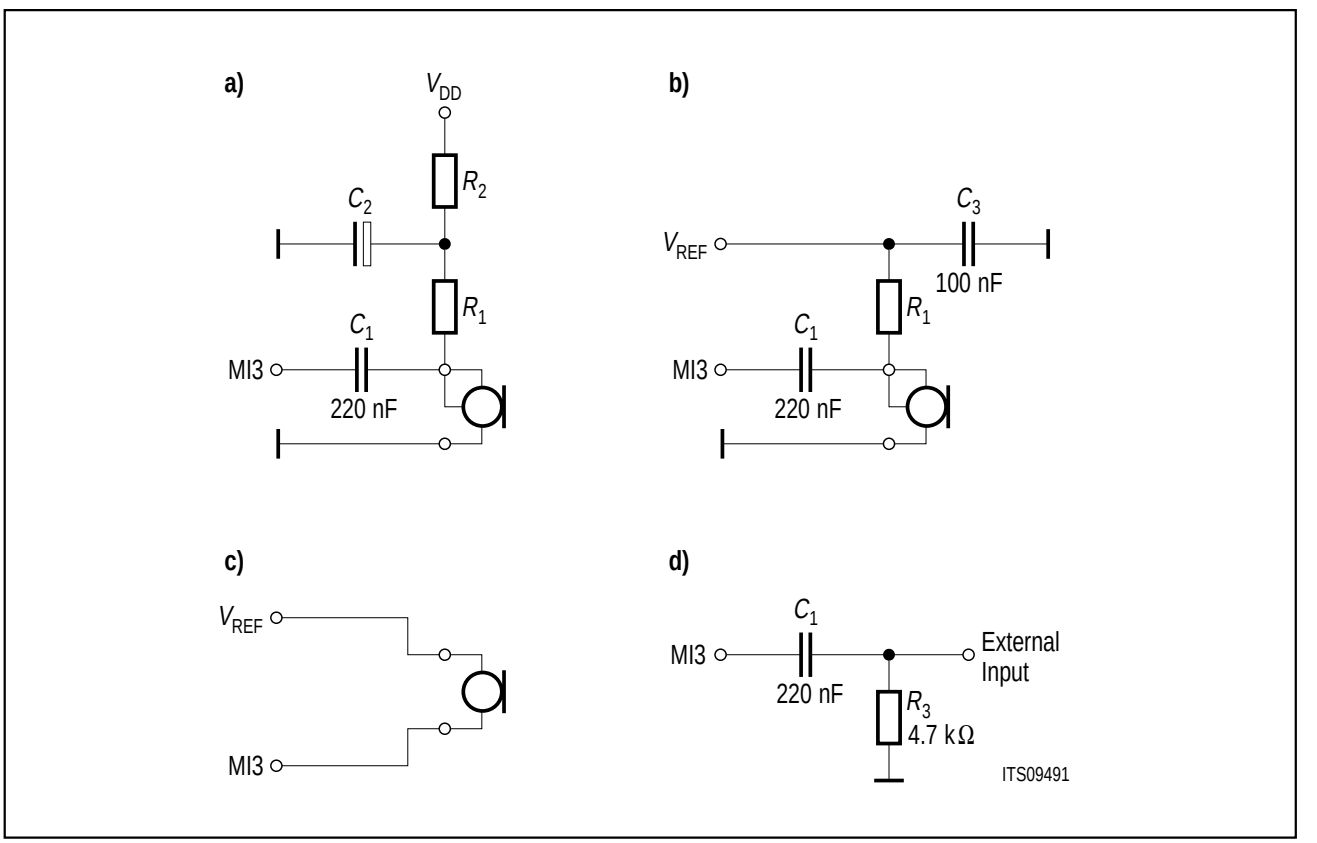

Figure 43
Using the Single Ended Input MI3

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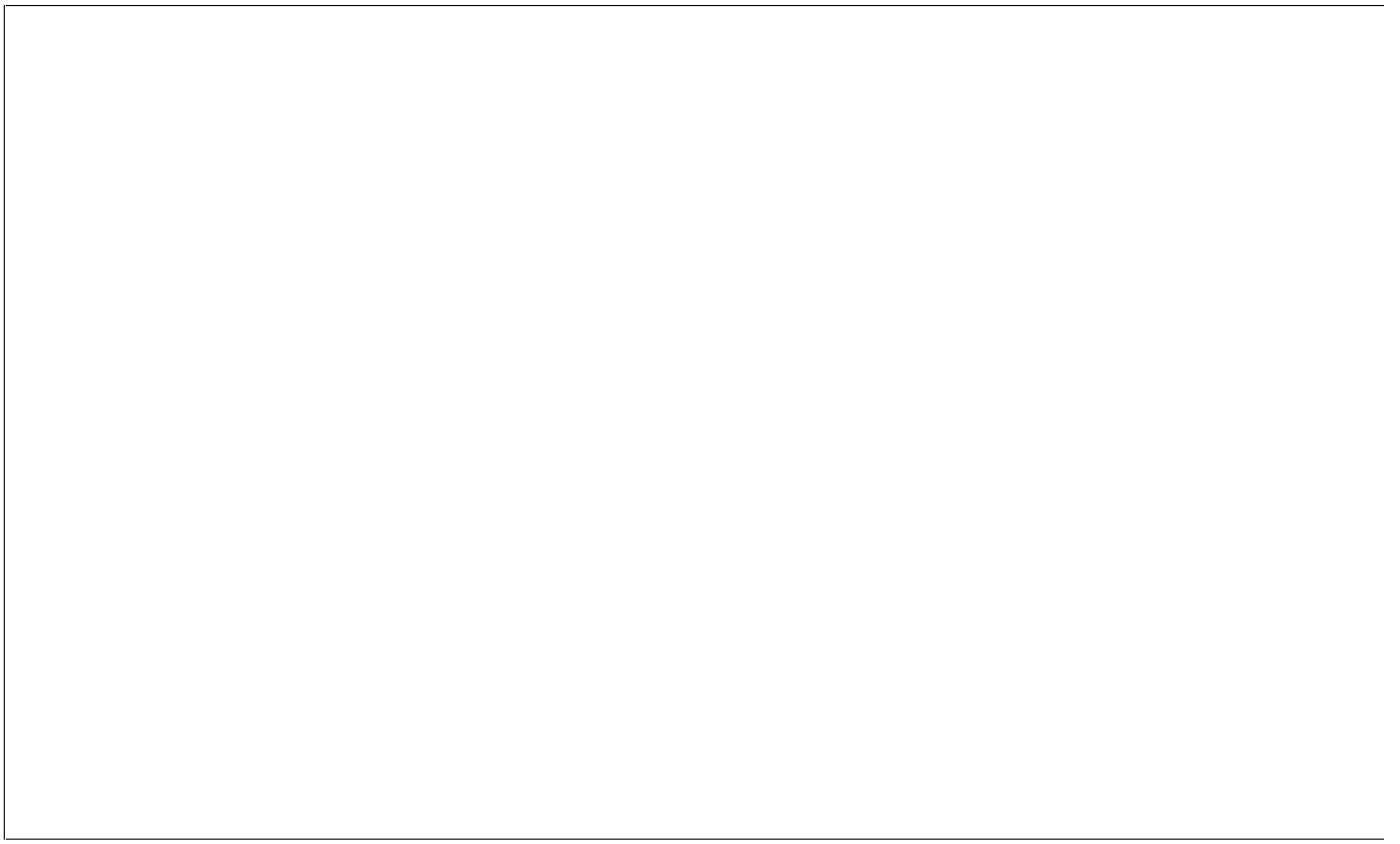

ICs for Communications

ARCOFI® Telephone Board

SIPB 5132-SP Version 2.0

Board Description 05.96

SIPB 5132-SP Revision History:		Current Version: 1996-05-01
Previous Version:		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

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8 ARCOFI® Telephone Board SIPB 5132-SP – Board Description

8.1 Introduction

The ARCOFI Telephone Board SIPB 5132-SP is an evaluation board for the ARCOFI-SP PSB 2163 and the ARCOFI-BA PSB 2161. In conjunction with an acoustic box (optional) and a handset it can be used as a simple IOM-2 telephone. Handset and handsfree operation are fully supported but no keypad for entering dialling information is available. For evaluation and measurement purposes all analog in- and outputs pins of the PSB 2161/PSB 2163 are directly accessible. Customer specific analog circuitry can easily be connected. The SIPB 5132-SP board can be configured for IOM-2 TE or NON-TE mode (1.536 MHz or 4.096 MHz data clock).

Upon delivery the board is equipped with a PSB 2163 in a DIP-28 package. Since the PSB 2163 is compatible with the PSB 2161 all applications for the PSB 2161 can be evaluated with the PSB 2163 as well. The only difference between the two chips is the lack of speakerphone support with the PSB 2161. If desired, a PSB 2161 can be soldered to the DSO-28 footprint inside the DIP-28 socket.

8.2 Hardware Configuration

8.2.1 Floor Plan and DIP Switches

Figure 44 shows a floor plan with all connectors and the different jumpers. Please refer also to the schematic of the board on SICOFI-2.

The ARCOFI-SP offers a test mode which indicates the internal speakerphone states (“transmit”, “receive”, and “idle”) with the help of LEDs connected to the piezo ringer output pins. On the SIPB 5132-SP board these pins are switched to a piezo ringer or to a pair of LEDs with J1 and J2.

Power supply (+ 5 V) can be taken directly from the IOM-2 connector or from a separate connector ST2. This can be selected by J3.

The complete circuitry for the analog front end is connected through the jumpers ST5. Therefore each analog in-/output pin of the ARCOFI is accessible at ST5 if the corresponding jumper is removed; please refer to the schematic for details.

The reset pin of the ARCOFI is active high. On the board a pull-up resistor is connected to the reset pin. The reset switch S2 is normally closed and requires the reset line at the IOM-2 connector to be held low by the connected hardware. If a customer specific hardware is used together with the SIPB 5132-SP board it must be ensured that during normal operation this reset line has a low level.

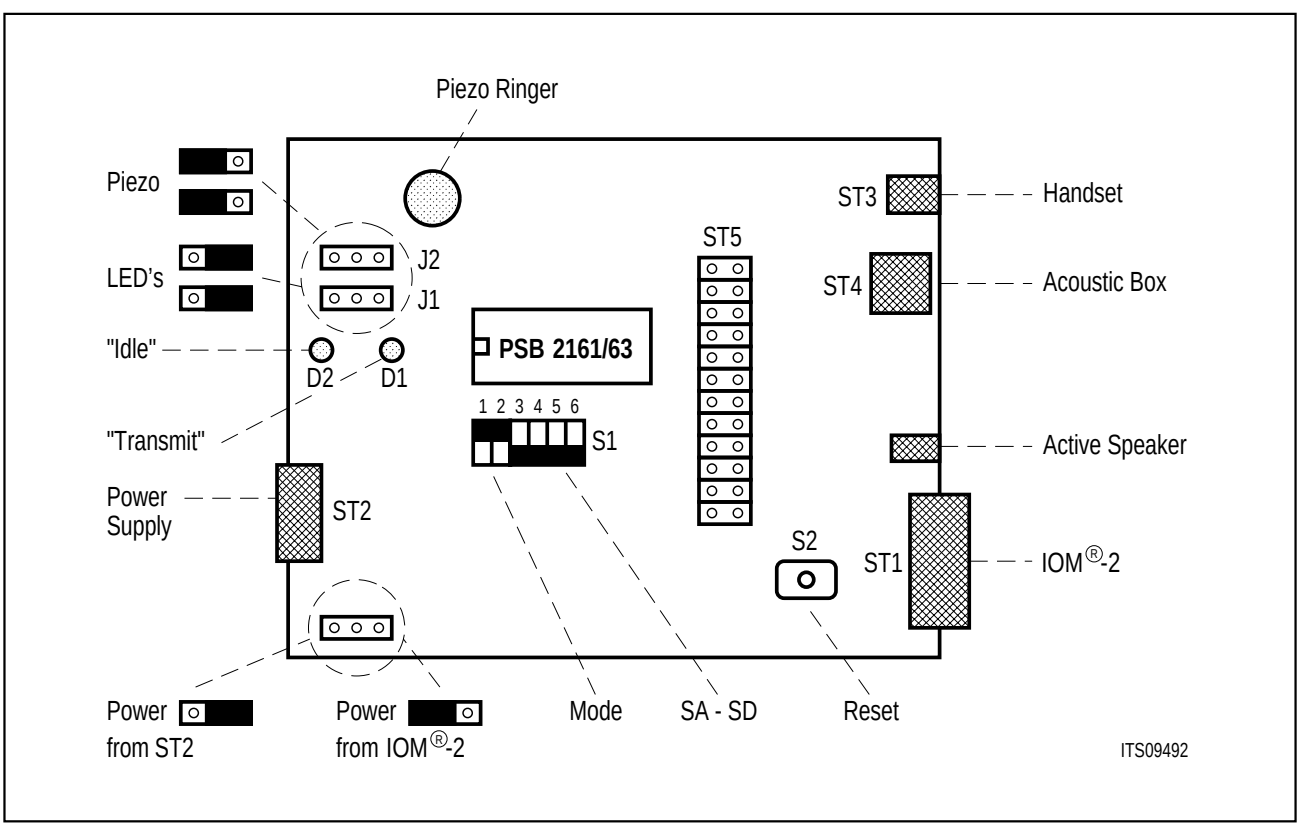

Figure 44
Floor Plan with all Connectors

The switches 1 and 2 of DIP-switch S1 are used to select the address and the interface mode of the ARCOFI. The other four switches are applying high or low-level signals to the pins SA, SB, SC, and SD of the ARCOFI. They can therefore be used to test the PCI interface (general I/O interface) if the ARCOFI is in IOM-2-TE mode or to select the active IOM channel if the IOM-2-NON-TE mode is used (refer to ARCOFI User's Manual, e.g. PSB 2163, User's Manual 06.96, page 65).

Table 2
Mode and Address setting with DIP Switch 1 and 2

Switch	ON	OFF
S1, Switch 1	IOM-2 TE (1.536 MHz)	IOM-2 NON-TE (4.096 MHz)
S1, Switch 2	A-Chip (AD = 0)	B-Chip (AD = 1)

Table 3
Purpose of Switch 3 to 6

Switch	ON	OFF
S1, Switch 3	Low-level at pin SA	High-level at pin SA
S1, Switch 4	Low-level at pin SB	High-level at pin SB
S1, Switch 5	Low-level at pin SC	High-level at pin SC
S1, Switch 6	Low-level at pin SD	High-level at pin SD

8.2.2 Connectors

Connector ST1

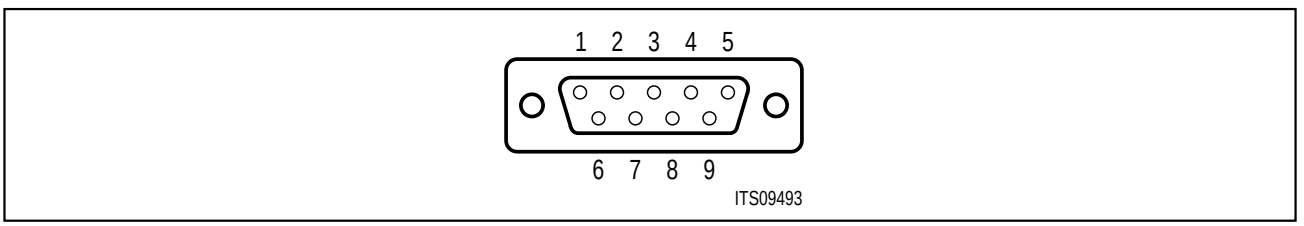

Figure 45
IOM® Connector

Pin	Use	Signal
1	I	V+
2	I	GND
3	NC	–
4	O	DD
5	NC	–
6	I	DCL
7	I	FSC
8	I	DU
9	I	Reset

Connector ST2

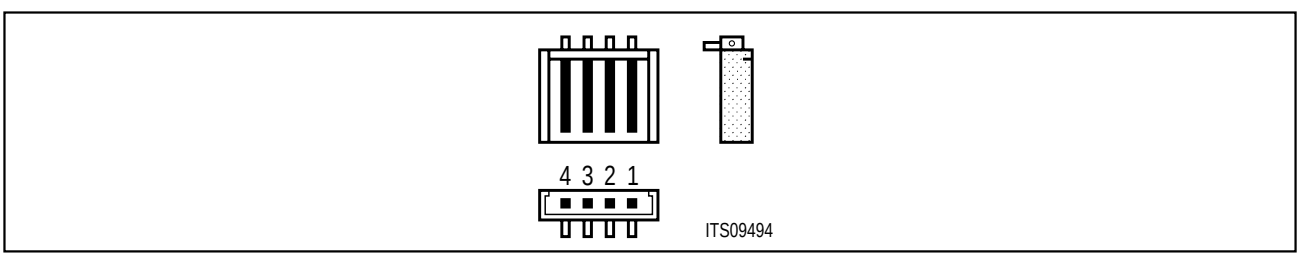

Figure 46
External Power Supply

Pin	Use	Signal
1	I	V+
2	I	GND
3	I	GND
4	NC	–

Connector ST3

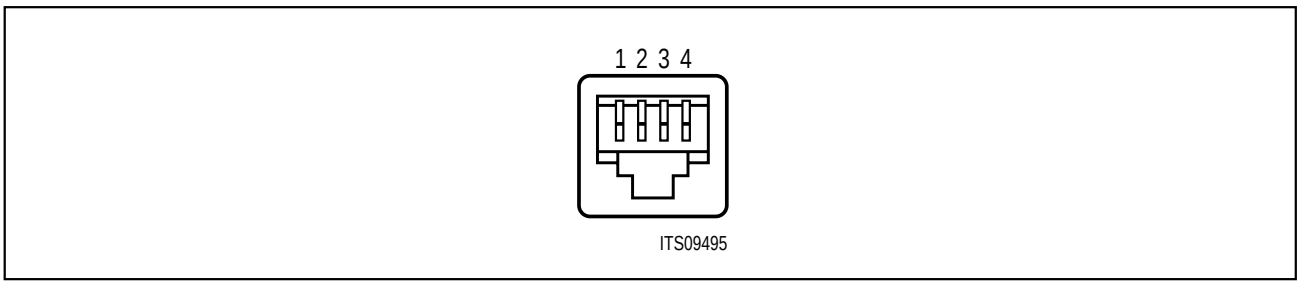

Figure 47
Handset Connector

Pin	Use	Signal
1	I	MIP2
2	O	HOP
3	O	HON
4	I	GNA

Connector ST4

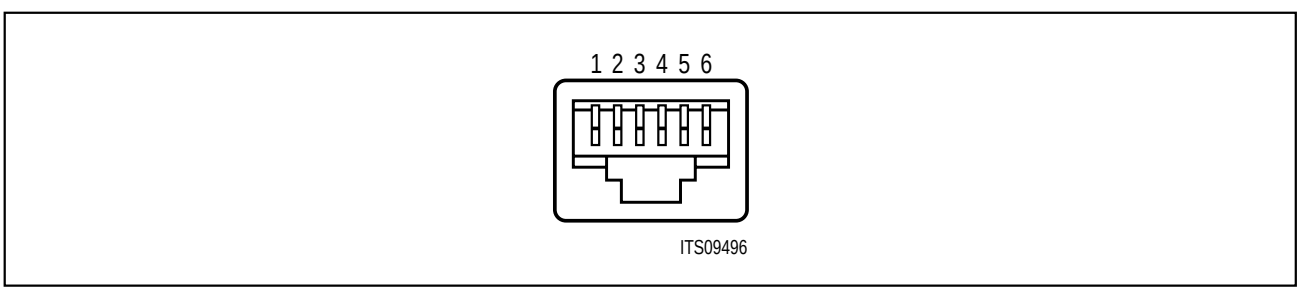

Figure 48
Speakerphone Connector

Pin	Use	Signal
1	-	NC
2	I	MIP1
3	O	LSN
4	O	LSP
5	I	GNA
6	-	NC

8.3 Hardware Environment

Figure 49 shows a typical example for a hardware setup based on the SIPB 5000 mainboard with the ISAC-S (TE) or the ISAC-P (TE) as a transceiver chip. The ARCOFI telephone board SIPB 5132-SP is connected via a flat-band cable to the IOM-2 connector that leads to the Audio Interface Module SIPB 5130. The interface mode used is the IOM-2-TE mode. Programming can be performed with the ARCOS software package or the SIPB menu-software which comes with the SIPB 5000 board. If two of the terminals in **figure 49** are linked via a Mini-Switch SIPB 8100 a complete ISDN voice connection can be simulated (without D-channel protocol).

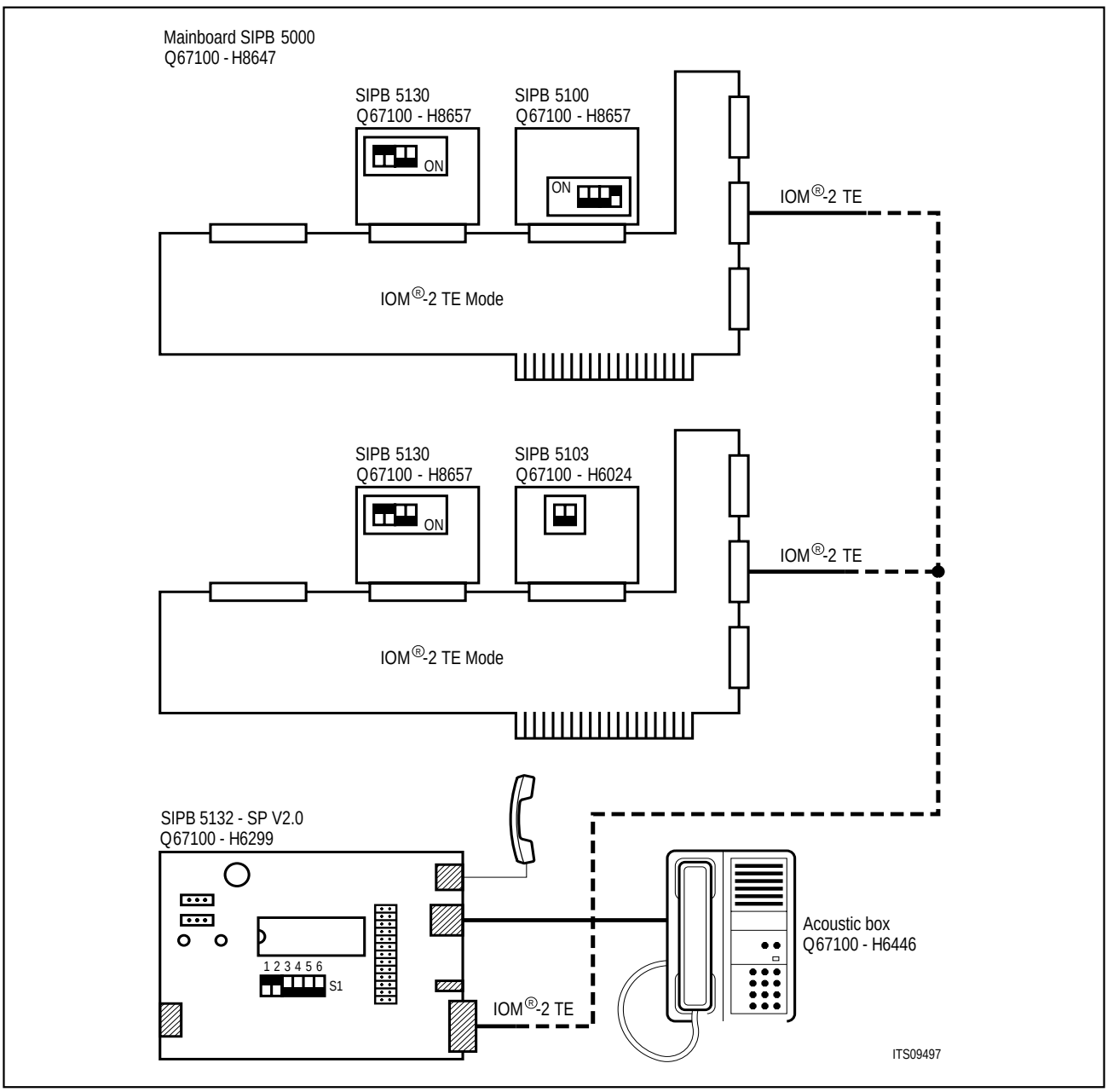

Figure 49
Terminal Configuration with SIPB 5000 Mainboard

For the IOM-2 NON-TE mode the configuration in **figure 50** can be used. Again programming can be done either with the ARCOS software or the menu software. The PCM4 adapter is optional. A more flexible setup for PCM4 measurements can be made with the PERCOFI-Board STUT 2000.

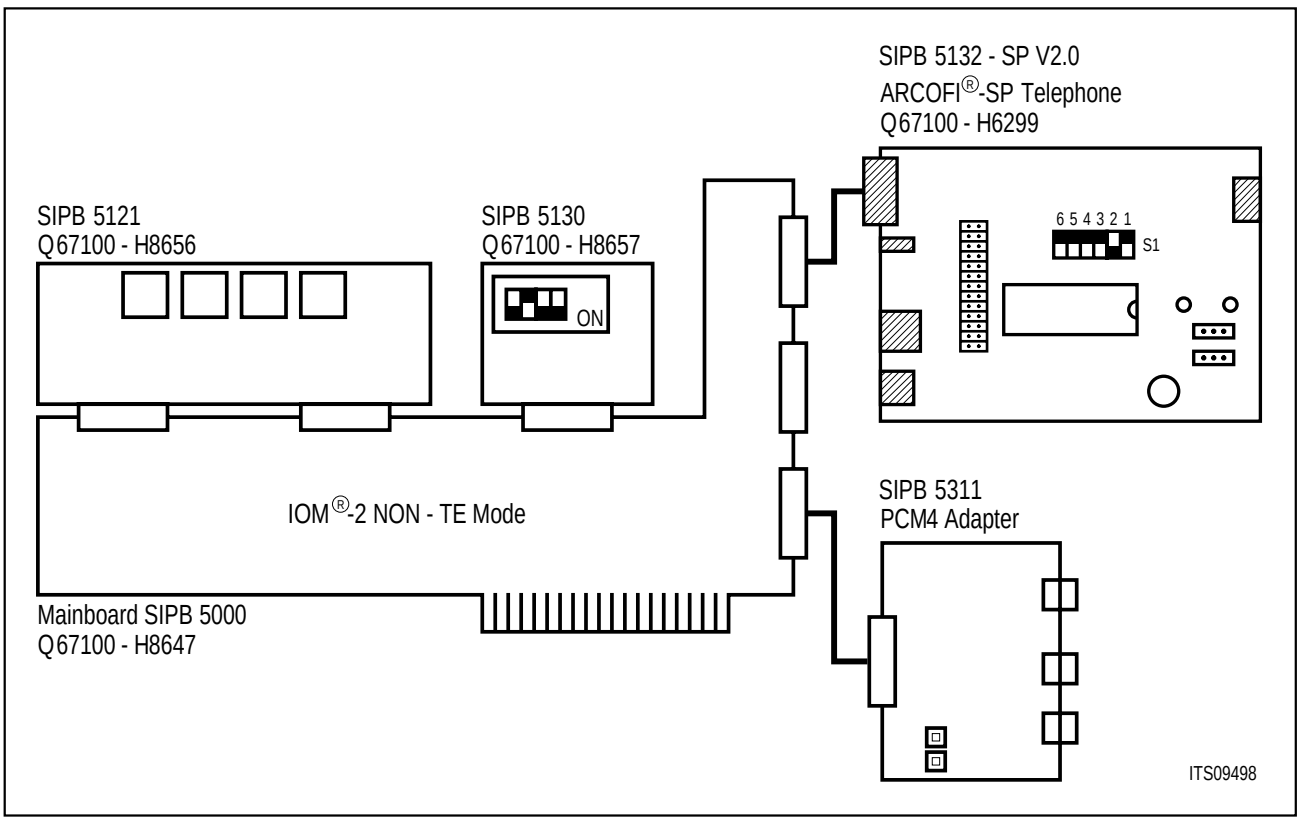

Figure 50
Setup for NON-TE Mode

8.4 Trackfiles

8.4.1 Trackfile for IOM®-2 TE Mode

The following trackfile can be used with the setup shown in **figure 49**. It is written for the PSB 2163 but can be used with the PSB 2161 as well.

```
C ************************************
C ************************************
C *                                  *
C * Trackfile  HS_S0.TE              *
C *                                  *
C *  PROGRAMMING THE ARCOFI-SP       *
C *           PSB 2163               *
C *    IOM2 in HANDSET MODE          *
C *       and additionally           *
C *  ACTIVATING THE S0 - INTERFACE   *
C *                                  *
C * !! COSY /2 MUST BE RUN BEFORE !! *
C *                                  *
C ************************************
C ************************************
C
C ------------------------------------
C ISAC-S in IOM2 mode
C ------------------------------------
W /S02TE/ISAC_S/SERIAL/ADF2 80
W /S02TE/ISAC_S/SERIAL/SPCR 80
R /S02TE/ISAC_S/HDLC/STAR 4A
R /S02TE/ISAC_S/HDLC/STAR 4A
R /S02TE/ISAC_S/HDLC/STAR 4A
C ------------------------------------
C Activation of the S0 - interface
C ------------------------------------
W /S02TE/ISAC_S/SERIAL/CIX0 60
R /S02TE/ISAC_S/SERIAL/CIR0 30
R /S02TE/ISAC_S/SERIAL/CIR0 30
W /S02TE/ISAC_S/SERIAL/SPCR 05
R /S02TE/ISAC_S/SERIAL/SPCR 05
C ------------------------------------
C IOM2 - Identification of ARCOFI-SP
C ------------------------------------
W /S02TE/ISAC_S/SERIAL/MOCR A0
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 A0
W /S02TE/ISAC_S/SERIAL/MOCR B0
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 00
R /S02TE/ISAC_S/SERIAL/MOSR A0
R /S02TE/ISAC_S/SERIAL/MOR1 A0
W /S02TE/ISAC_S/SERIAL/MOCR E0
R /S02TE/ISAC_S/SERIAL/MOSR 80
R /S02TE/ISAC_S/SERIAL/MOR1 84
R /S02TE/ISAC_S/SERIAL/MOSR 40
W /S02TE/ISAC_S/SERIAL/MOCR A0
R /S02TE/ISAC_S/SERIAL/MOSR 00
C ------------------------------------
C Programming the ARCOFI-SP
```

```
C in HANDSET mode
C ----------------------------------
R /S02TE/ISAC_S/SERIAL/MOSR 00
W /S02TE/ISAC_S/SERIAL/MOX1 A1
W /S02TE/ISAC_S/SERIAL/MOCR B0
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 1F
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 00
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 60
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 41
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 00
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 00
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 20
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 F1
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 12
R /S02TE/ISAC_S/SERIAL/MOSR 20
C ----------------------------------
C COP_6: GZ=-15dB
C ----------------------------------
W /S02TE/ISAC_S/SERIAL/MOX1 26
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 99
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 32
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOCR A0
R /S02TE/ISAC_S/SERIAL/MOSR 00
C ----------------------------------
C Powering up the ARCOFI-SP
C ----------------------------------
R /S02TE/ISAC_S/SERIAL/MOSR 00
W /S02TE/ISAC_S/SERIAL/MOX1 A1
W /S02TE/ISAC_S/SERIAL/MOCR B0
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 31
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOCR A0
R /S02TE/ISAC_S/SERIAL/MOSR 00
C ----------------------------------
C Read Out SOP_F 00, 60, 41, 00
C                00, 20, F1, 16
C ----------------------------------
W /S02TE/ISAC_S/SERIAL/MOCR A0
R /S02TE/ISAC_S/SERIAL/MOSR 00
W /S02TE/ISAC_S/SERIAL/MOX1 A1
W /S02TE/ISAC_S/SERIAL/MOCR B0
R /S02TE/ISAC_S/SERIAL/MOSR 20
W /S02TE/ISAC_S/SERIAL/MOX1 9F
R /S02TE/ISAC_S/SERIAL/MOSR A0
R /S02TE/ISAC_S/SERIAL/MOR1 A1
W /S02TE/ISAC_S/SERIAL/MOCR E0
```

```
R /S02TE/ISAC_S/SERIAL/MOSR 80
R /S02TE/ISAC_S/SERIAL/MOR1 00
R /S02TE/ISAC_S/SERIAL/MOSR 80
R /S02TE/ISAC_S/SERIAL/MOR1 60
R /S02TE/ISAC_S/SERIAL/MOSR 80
R /S02TE/ISAC_S/SERIAL/MOR1 41
R /S02TE/ISAC_S/SERIAL/MOSR 80
R /S02TE/ISAC_S/SERIAL/MOR1 00
R /S02TE/ISAC_S/SERIAL/MOSR 80
R /S02TE/ISAC_S/SERIAL/MOR1 00
R /S02TE/ISAC_S/SERIAL/MOSR 80
R /S02TE/ISAC_S/SERIAL/MOR1 20
R /S02TE/ISAC_S/SERIAL/MOSR 80
R /S02TE/ISAC_S/SERIAL/MOR1 F1
R /S02TE/ISAC_S/SERIAL/MOSR 80
R /S02TE/ISAC_S/SERIAL/MOR1 16
R /S02TE/ISAC_S/SERIAL/MOSR 40
W /S02TE/ISAC_S/SERIAL/MOCR A0
R /S02TE/ISAC_S/SERIAL/MOSR 00
C
C ************************************
C ************************************
C *                                  *
C *         End of Trackfile         *
C *                                  *
C ************************************
C ************************************
```

8.4.2 Trackfiles for IOM®-2 NON-TE Mode

The trackfiles in this chapter can be used with the hardware shown in **figure 50**. Before the ARCOFI can be accessed the EPIC on the Linecard Module has to be initialized first. This is the task of the first trackfile LC_1.IOM. This trackfile was originally written for the SICOFI 2 chip but can be used with the ARCOFIs as well.

```
C ***********************************
C              LC_1.IOM
C ***********************************
C
C application: initialization of the
C              line card module
C              for a SICOFI2
C              measurement tool
C setup: line card module sipb 5121
C
C iom2 channel assignement:
C * ch0: analog subscriber (sicofi2)
C * ch1: analog subscriber (sicofi2)
C * ch2: analog subscriber (sicofi2)
C * ch3: analog subscriber (sicofi2)
C * ch4: analog subscriber (sicofi2)
C * ch5: analog subscriber (sicofi2)
C * ch6: analog subscriber (sicofi2)
C * ch7: analog subscriber (sicofi2)
C
C interface characteristics:
C pcm interface: 2 hws with 32 ts each
C cfi interface: 4 hws with 32 ts each
C                (4 iom2 interfaces)
C
C configuration of the lc module:
C config register bits:
C id,cks/tc2/tc1/tc0/dch/dma/cts/res
C * clock mode 6 (xtal 4096khz)
C * reset of on board devices
W /LINECA/CONFIG/CONFIG/CONFIG 61
W /LINECA/CONFIG/CONFIG/CONFIG 60
C
C configuration of the pcm interface:
C * pcm mode 0
W /LINECA/EPIC/PCMCFI/PMOD 20
W /LINECA/EPIC/PCMCFI/PCSR 11
W /LINECA/EPIC/PCMCFI/POFD F1
W /LINECA/EPIC/PCMCFI/POFU 19
C
C configuration of the cfi interface:
C * cfi mode 0, clock source: pcl/pfs
C * pfs evaluated with falling edge
C * prescaler = 1
W /LINECA/EPIC/PCMCFI/CMD1 20
C * fsc output: fc mode 6
C * dcl output: double rate
C * xmit rising, rec falling edge
W /LINECA/EPIC/PCMCFI/CMD2 D0
C * cfi bit number is 256
W /LINECA/EPIC/PCMCFI/CBNR FF
```

```
C * pfs marks cfi ts31,bit1
W /LINECA/EPIC/PCMCFI/CTAR 02
C * no shift between xmit and rec
W /LINECA/EPIC/PCMCFI/CBSR 00
C * subchannel position:64kbps=bits7.0
C                       32kbps=bits7.4
C                       16kbps=bits7.6
W /LINECA/EPIC/PCMCFI/CSCR 00
C
C initialization of cm ctrl field:
C * cm reset mode
W /LINECA/EPIC/MARSCR/OMDR 00
C * ff is copied to all positions of
C * the cm ctrl field
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MACR 70
C
C cfi configuration for iom2:
C * cm init mode
W /LINECA/EPIC/MARSCR/OMDR 80
C
C cfi timeslots  2 and  3 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts  2 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 08
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts  3 downstream:
W /LINECA/EPIC/MARSCR/MAAR 09
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts  2 upstream:
W /LINECA/EPIC/MARSCR/MAAR 88
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts  3 upstream:
W /LINECA/EPIC/MARSCR/MAAR 89
W /LINECA/EPIC/MARSCR/MACR 7A
C
C cfi timeslots  6 and  7 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts  6 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 18
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts  7 downstream:
W /LINECA/EPIC/MARSCR/MAAR 19
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts  6 upstream:
W /LINECA/EPIC/MARSCR/MAAR 98
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts  7 upstream:
W /LINECA/EPIC/MARSCR/MAAR 99
W /LINECA/EPIC/MARSCR/MACR 7A
C
C cfi timeslots 10 and 11 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts 10 downstream:
```

```
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 28
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 11 downstream:
W /LINECA/EPIC/MARSCR/MAAR 29
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 10 upstream:
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 11 upstream:
W /LINECA/EPIC/MARSCR/MAAR A9
W /LINECA/EPIC/MARSCR/MACR 7A
C cfi timeslots 14 and 15 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts 14 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 38
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 15 downstream:
W /LINECA/EPIC/MARSCR/MAAR 39
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 14 upstream:
W /LINECA/EPIC/MARSCR/MAAR B8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 15 upstream:
W /LINECA/EPIC/MARSCR/MAAR B9
W /LINECA/EPIC/MARSCR/MACR 7A
C cfi timeslots 18 and 19 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts 18 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 48
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 19 downstream:
W /LINECA/EPIC/MARSCR/MAAR 49
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 18 upstream:
W /LINECA/EPIC/MARSCR/MAAR C8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 19 upstream:
W /LINECA/EPIC/MARSCR/MAAR C9
W /LINECA/EPIC/MARSCR/MACR 7A
C cfi timeslots 22 and 23 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts 22 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 58
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 23 downstream:
W /LINECA/EPIC/MARSCR/MAAR 59
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 22 upstream:
W /LINECA/EPIC/MARSCR/MAAR D8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 23 upstream:
W /LINECA/EPIC/MARSCR/MAAR D9
```

```
W /LINECA/EPIC/MARSCR/MACR 7A
C cfi timeslots 26 and 27 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts 26 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 68
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 27 downstream:
W /LINECA/EPIC/MARSCR/MAAR 69
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 26 upstream:
W /LINECA/EPIC/MARSCR/MAAR E8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 27 upstream:
W /LINECA/EPIC/MARSCR/MAAR E9
W /LINECA/EPIC/MARSCR/MACR 7A
C cfi timeslots 30 and 31 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts 30 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 78
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 31 downstream:
W /LINECA/EPIC/MARSCR/MAAR 79
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 30 upstream:
W /LINECA/EPIC/MARSCR/MAAR F8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 31 upstream:
W /LINECA/EPIC/MARSCR/MAAR F9
W /LINECA/EPIC/MARSCR/MACR 7A
C * pcm status is
R /LINECA/EPIC/MARSCR/STAR 05
C * not synchronized (pss=0)
C
C setting epic to normal mode
W /LINECA/EPIC/MARSCR/OMDR C0
R /LINECA/EPIC/MARSCR/ISTA 08
R /LINECA/EPIC/MARSCR/STAR 25
C pcm status: synchronized (pss=1)
C
C initialization of the pcm tristate
C field, all ch. to high impedance
W /LINECA/EPIC/MARSCR/MADR 00
W /LINECA/EPIC/MARSCR/MACR 68
C
C activation epic:
C * normal mode, pcm and cfi active
C * cfi output drivers push-pull
C * mf ch. handshake protocol enabled
W /LINECA/EPIC/MARSCR/OMDR E6
C
C reset cififo:
W /LINECA/EPIC/MARSCR/CMDR 10
C
C
C the line card is now ready for use
```

```
C the SICOFI2 and do measurements
C with the PCM4 from Wandel and
C Goltermann
C ***********************************
C
C Now you can run your trackfile with
C the filter coefficients
C
C ***********************************
C
C end of trackfile
C
```

After initializing the EPIC on the LineCard module the file HS_LC.TE can be used to set the ARCOFI in handset mode.

```
C*******************************
C*******************************
C
C  Track File HS_LC.TE
C
C  Programming the ARCOFI-SP
C  PSB 2163 via IOM-2 NON-TE
C  in Handset Mode
C
C  Trackfile LC_1.IOM has to
C  be run before !
C
C  Configuration:
C  -------------
C  LineCard     SIPB 5121
C  Audio Module SIPB 5130
C               DIP-Switch 1 ON
C                          2 ON
C                          3 OFF
C                          4 ON
C
C*******************************
C*******************************
C
C-------------------------------
C Connecting the LineCard to the
C Audio Interface Module
C-------------------------------
C
W /LINECA/CONFIG/CONFIG/CONFIG E0
C
C-------------------------------
C Selecting the timeslot
C (depends on the pins SB,SC,SD)
C Here: slot 7 (all pins to VCC)
C
C MFSAR = 04  => slot 0
C MFSAR = 0C  => slot 1
C MFSAR = 14  => slot 2
C MFSAR = 1C  => slot 3
C MFSAR = 24  => slot 4
```

```
C MFSAR = 2C  => slot 5
C MFSAR = 34  => slot 6
C MFSAR = 3C  => slot 7
C--------------------------------
C
W /LINECA/EPIC/MCHSTR/MFSAR 3C
C
C--------------------------------
C ARCOFI-SP Identification
C--------------------------------
C
W /LINECA/EPIC/MCHSTR/CMDR 01
W /LINECA/EPIC/MCHSTR/MFFIFO A0
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
R /LINECA/EPIC/MCHSTR/STAR 26
R /LINECA/EPIC/MCHSTR/MFFIFO A0
R /LINECA/EPIC/MCHSTR/STAR 26
R /LINECA/EPIC/MCHSTR/MFFIFO 84
W /LINECA/EPIC/MCHSTR/CMDR 01
C
C--------------------------------
C COP_6: GZ=-15dB
C--------------------------------
C
W /LINECA/EPIC/MCHSTR/MFFIFO A1
W /LINECA/EPIC/MCHSTR/MFFIFO 26
W /LINECA/EPIC/MCHSTR/MFFIFO 99
W /LINECA/EPIC/MCHSTR/MFFIFO 32
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/CMDR 04
W /LINECA/EPIC/MCHSTR/CMDR 01
C
C--------------------------------
C SOP_F: Handset Mode
C--------------------------------
C
W /LINECA/EPIC/MCHSTR/MFFIFO A1
W /LINECA/EPIC/MCHSTR/MFFIFO 1F
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 60
W /LINECA/EPIC/MCHSTR/MFFIFO 41
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 20
W /LINECA/EPIC/MCHSTR/MFFIFO F1
W /LINECA/EPIC/MCHSTR/MFFIFO 16
W /LINECA/EPIC/MCHSTR/CMDR 04
W /LINECA/EPIC/MCHSTR/CMDR 01
C********************************
C********************************
C*                              *
C* End of Track File            *
C*                              *
C********************************
C********************************
```

The following trackfile can be used as a basis for PCM4 measurements. It must be completed by the desired programming for the ARCOFI itself. The Trackfile LC_1.IOM has to be executed first.

```
C*******************************
C*******************************
C
C  Track File LC_PCM4.TE
C
C  Preparing the ARCOFI-SP
C  PSB 2163 for PCM4 measurements
C
C  Trackfile LC_1.IOM has to
C  be run before !
C
C  Configuration:
C  -------------
C  LineCard     SIPB 5121
C  Audio Module SIPB 5130
C               DIP-Switch 1 ON
C                          2 ON
C                          3 OFF
C                          4 ON
C  PCM4 Adaptor SIPB 5311
C               Jumper open
C
C*******************************
C*******************************
C
C--------------------------------
C Connecting the LineCard to the
C Audio Interface Module
C--------------------------------
C
W /LINECA/CONFIG/CONFIG/CONFIG E0
C
C--------------------------------
C Selecting the timeslot
C (depends on the pins SB,SC,SD)
C Here: slot 7 (all pins to VCC)
C--------------------------------
C
W /LINECA/EPIC/MCHSTR/MFSAR 3C
C
C--------------------------------
C B-channel switching for the
C PCM4 Adaptor
C B1 -> TS1
C B2 -> TS2
C--------------------------------
C
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 81
W /LINECA/EPIC/MARSCR/MACR 60
C
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 88
```

```
W /LINECA/EPIC/MARSCR/MACR 60
C
W /LINECA/EPIC/MARSCR/MADR 81
W /LINECA/EPIC/MARSCR/MAAR F0
W /LINECA/EPIC/MARSCR/MACR 71
C
W /LINECA/EPIC/MARSCR/MADR 01
W /LINECA/EPIC/MARSCR/MAAR 70
W /LINECA/EPIC/MARSCR/MACR 71
C
W /LINECA/EPIC/MARSCR/MADR 88
W /LINECA/EPIC/MARSCR/MAAR F1
W /LINECA/EPIC/MARSCR/MACR 71
C
W /LINECA/EPIC/MARSCR/MADR 08
W /LINECA/EPIC/MARSCR/MAAR 71
W /LINECA/EPIC/MARSCR/MACR 71
C
C--------------------------------
C ARCOFI-SP Identification
C--------------------------------
C
W /LINECA/EPIC/MCHSTR/CMDR 01
W /LINECA/EPIC/MCHSTR/MFFIFO A0
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
R /LINECA/EPIC/MCHSTR/STAR 26
R /LINECA/EPIC/MCHSTR/MFFIFO A0
R /LINECA/EPIC/MCHSTR/STAR 26
R /LINECA/EPIC/MCHSTR/MFFIFO 84
W /LINECA/EPIC/MCHSTR/CMDR 01
C
C--------------------------------
C Insert now the desired
C programming sequence for the
C PSB 2163
C--------------------------------
C
C********************************
C********************************
C*                              *
C* End of Track File            *
C*                              *
C********************************
C********************************
```

8.5 Circuit Diagram

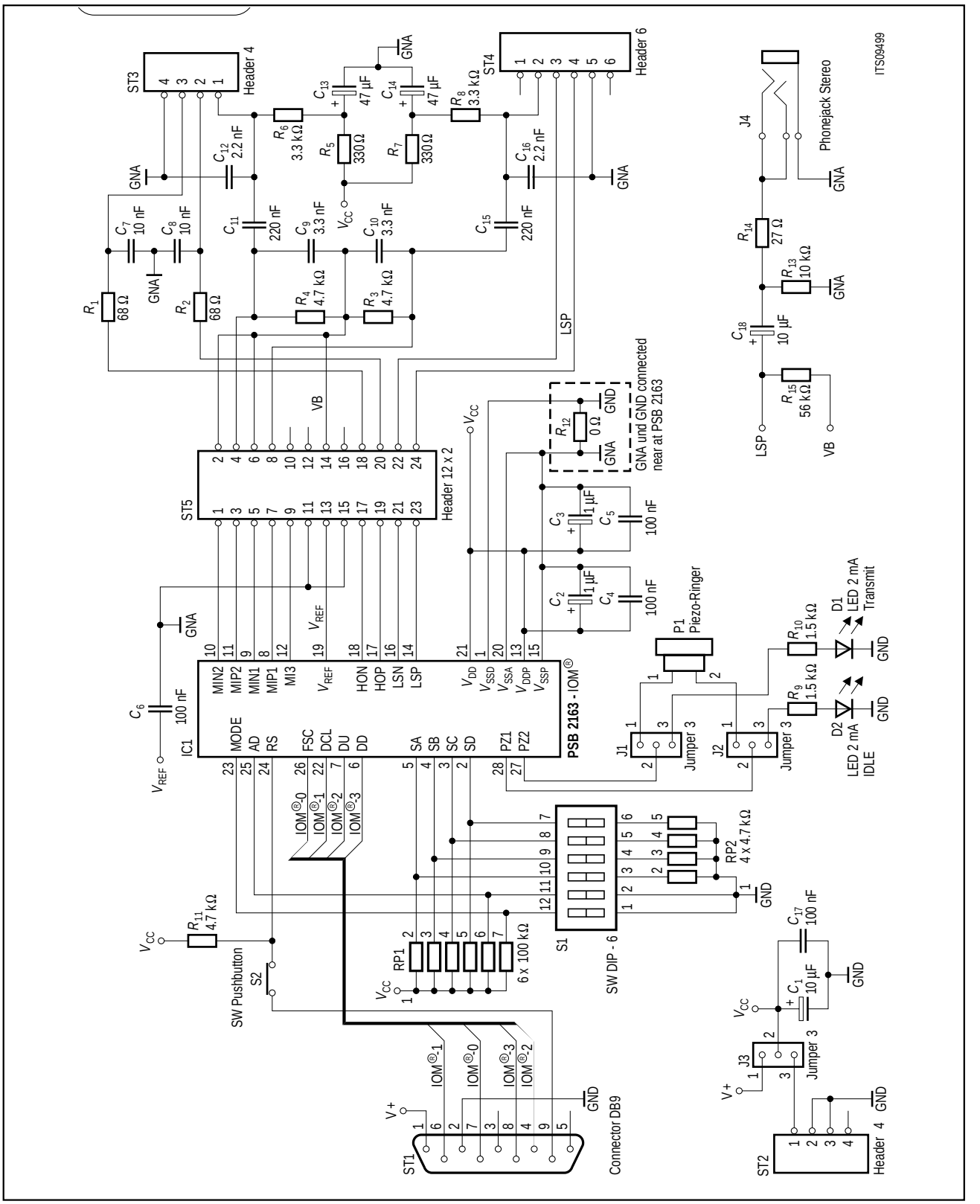

Figure 51
ARCOFI®-SP Telephone Board

SIEMENS

ICs for Communications

ARCOFI®-SP Coefficients Software ARCOS-SP PLUS

SIPO 2163

User's Manual 06.96

SIPO 2163 Revision History:		Current Version: 1996-06-01
Previous Version:		03.95
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
		ARCOS-SP PLUS V1.1 supports now PSB2161
		no demo version
		typical hardware setups show SIPB5132-SP V2.0 instead of V1.0

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9 ARCOFI® Coefficients Software SIPO 2163 – User's Manual

9.1 Introduction

9.1.1 The ARCOFI®-SP PSB 2163

The PSB 2163 provides the subscriber with an optimized Audio, Ringing, Codec, Filter processor solution for a digital telephone. The ARCOFI-SP fulfils all the necessary requirements for a full-featured digital telephone including handsfree operation. The ARCOFI-SP performs all coding, decoding and filtering according to ITU-T and ETSI standards. The outstanding advantage of the PSB 2163 is the high performance speakerphone implementation with the "stronger-wins algorithm" that allows almost a full duplex conversation.

Due to the completely digital concept of the circuit no external components are required. The various filters and processing steps of the voice channel including the speakerphone, the signalling, and the tone generation can be adapted to meet the different operating conditions by means of software. Also adapting different acoustical transducers to the ARCOFI-SP is accomplished simply by programming registers and coefficients.

Therefore evaluating the features and the high performance of the PSB 2163 is an easy thing if some software is available to program the chip. An important task of the ARCOS-SP PLUS software is to offer an quick and easy way for evaluation.

9.1.2 The ARCOFI®-BA PSB 2161

The PSB 2161 is a pin-compatible, downstrapped version of the PSB 2163. The only difference between the two chips is the lack of speakerphone support with the PSB 2161. In fact, the SP-bit in the general configuration register of the PSB 2161 is not available. All other register and CRAM locations have the same meaning as with the PSB 2163 so that both devices are software compatible. The identification code of the PSB 2161 is different too. Therefore it is possible to distinguish between the PSB 2161 and PSB 2163 by software means.

9.1.3 The ARCOS-SP PLUS Software

The ARCOS-SP PLUS program has been designed to generate all the required coefficients and to program the ARCOFI-SP and the ARCOFI-BA in a real environment. Besides the software offers an easy way to get familiar with the internal structure of the ARCOFI-SP and ARCOFI-BA because all functional blocks are displayed in a graphic form with many possibilities of interaction (switches, parameters, registers that can be clicked upon). Throughout this software description the term "ARCOFI" refers to both, the ARCOFI-SP and the ARCOFI-BA.

Features of the ARCOS-SP PLUS Software

ARCOS-SP PLUS supports the calculation and programming of

- coefficients for the ARCOFI-SP digital speakerphone
- coefficients for the three ARCOFI tone generation registers
- coefficients for the ARCOFI DTMF tone generator registers
- coefficients for both ARCOFI programmable gain registers GX and GR
- coefficients for the GZ side tone gain register
- coefficients for the FX and FR correction filter registers;
  adaptive software calculates coefficients to fit a target frequency response

ARCOS-SP PLUS supports also the configuration registers and offers an user-friendly dialogue mode allowing full programming of the ARCOFI configuration registers and the coefficient RAM (CRAM).

Other features simplify working with the ARCOFI:

- access to different kinds of hardware (see **chapter 9.4** for details)
- NOTE and EXECUTE (a kind of keyboard macro)
- READ ARCOFI and WRITE ARCOFI
- support of transmission measurements using the Wandel&Goltermann PCM-4 measuring instrument

It is highly recommended to have an User's Manual at hand when working with the ARCOS-SP PLUS software. It is recommended to use the manual as a reference when working with the ARCOS-SP PLUS software. On the other hand, not all coefficients are documented in detail in the User's Manual of the PSB 2163 and PSB 2161 so the ARCOS-SP PLUS software allow easy determination of all coefficients.

9.1.4 System Requirements

An IBM or compatible Personal Computer (AT or better) is required. The computer should have at least 500 kByte of free conventional DOS memory. DOS version 3.2 or newer is required. The usage of a mouse as an input device is recommended and offers access to all features of the user area. A mouse driver must be installed before calling the ARCOS-SP PLUS software.

For hardware access the SIEMENS ISDN PC Board (SIPB) system is required. The SIPB family consists of a mainboard (SIPB 5000) and a wide variety of modules to realize different applications. The following equipment is needed:

- a Mainboard SIPB 5000
- any Layer-1 module SIPB 511x
- any Layer-2 module SIPB 512x
- an Audio Interface Module SIPB 5130, EPROM version 2.0 or newer
- as well as one of the following modules containing the ARCOFI:
- an ARCOFI-SP Telephone SIPB 5132-SP V1.0 or V2.0
- an ARCOFI-SP Evaluation Board SIPB 5133-SP

The ARCOS-SP PLUS software not only supports the SIPB 5000 system, but also some evaluation boards that have serial interfaces. These are:

- SIPB 8051 ISDN Telephone and Terminal Adapter Development Board V1.0 or V2.0,
- SISI 2197 SmartLink Board,
- STUT 2000 PERCOFI-Board.

The setups for the different kinds of hardware are described in **chapter 9.4**.

9.1.5 Installation and Activation of ARCOS-SP PLUS

Installation

The following simple procedure is recommended for the installation of ARCOS-SP PLUS on a hard-disc:

Create ARCOS-SP directory: md c:\ARCOS_SP

Change to ARCOS-SP directory: cd ARCOS_SP

Copy ARCOS-SP files: copy a:*.* c:\ARCOS_SP*.*

At least the following files should have been copied:

- ARC63.EXE, the main program
- ARC63.TAB, data file
- RS232.INI, initialization file for the serial interface
- MSHERC.COM (hercules driver; only necessary if the system is equipped with a Hercules monochrome graphics card)

The program MSHERC.COM loads a Hercules driver resident in the RAM. When using a Hercules graphics card, this program must be called before starting ARCOS-SP PLUS.

The file ARC63.INI is generated by ARCOS-SP itself, it is not delivered with the program.

Starting ARCOS-SP PLUS

Enter the following DOS command to start ARCOS-SP:

ARC63 [File[.xxx]]

[File[.xxx]] is an optional initialization file. The initialization file contains information about the last hardware settings and the options chosen (see **chapter 9.4**). As default, the file ARC63.INI is used as initialization file.

Please note, that the ARCOS-SP PLUS software must be started with a special option when using external hardware which is controlled via the serial interface (command line switch /V; this is described in **chapter 9.4.3**).

After having started ARCOS-SP PLUS the following is carried out:

- loading the initialization file,
- loading the data file (ARC63.TAB),
- showing the ARCOS-SP PLUS main menu and the SIEMENS label (once a day),
- after a mouse click or carriage return the SIEMENS label will disappear.

The next step to be done is either to disable any hardware access or to initialize the hardware.

9.2 Using ARCOS-SP PLUS

9.2.1 Introduction

When working with ARCOS-SP PLUS the screen is divided into four main areas (please compare with **figure 52**):

- row 1 is reserved for the menu line
- rows 2 to 23 are for the User Area
- row 24 contains the command line
- row 25 is the status line.

All items that can be activated via the menu line are described in **chapter 9.2.2**. The user area is controlled with a mouse and allows to program the whole ARCOFI (**chapter 9.2.3**). Everything that can be done with the mouse in the user area can also be done via the command line using the keyboard. The syntax for the command line can be found in **chapter 9.2.4**.

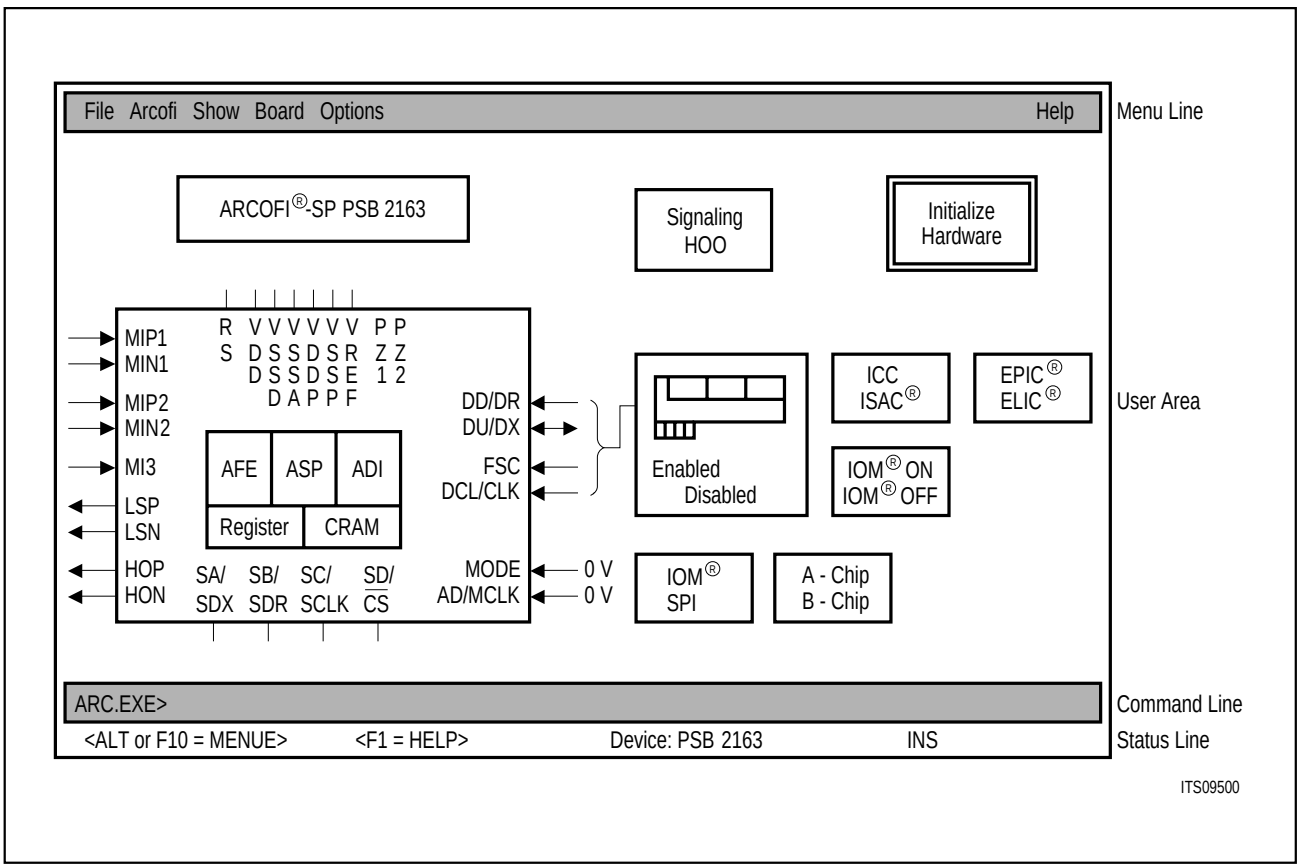


Figure 52
ARCOS-SP PLUS Screen

9.2.2 The Menu Line

9.2.2.1 Using the Menu Line

The menu items can always be activated by pressing either the F10-key or the ALT-key in combination with the highlightened letter of the menu item (e.g. "ALT+O" for the options menu). Of course, clicking with the left mouse button is also possible. The subsequent paragraphs describe each menu item.

9.2.2.2 Pull-Down Menu "File"

"Load"

The name of the file to be loaded has to be entered in the input field or can be selected in the file list. The command to load a file will be aborted if an incorrect, non-existent file name is entered. Both kinds of files: *.ARC and *.ARB are loadable (refer to the next paragraph). This menu item is used to restore a previously saved set of coefficients.

The load command can also be activated by pressing "Ctrl+L".

"Save"

The complete programming of the ARCOFI as well as the state of the ARCOS-SP PLUS software can be saved in a file.

When saving, a file name and format is asked for. There are two different formats supported by ARCOS-SP PLUS. They are an ARCOS-SP PLUS specific binary file format and a text format. If no extension is given, the entered name will automatically receive the following one:

sequence of commands: *.ARC (text format)

state of ARCOS-SP PLUS: *.ARB (binary format)

Afterwards the filename is checked for validity. If the file name is not correct, an error message appears and the save command is aborted.

The binary format is used to store the device status. Since the format is device specific it is not readable by the user. Being in binary format, the information exchange between the hard-disc and the ARCOS-SP PLUS software is speeded up.

The text format takes more time to program a sequence since this format has to be translated to the binary format via the ARCOS command interpreter before it is sent to the ARCOFI. The user, however, can read this format, which facilitates programming the ARCOFI. For documentation purposes the contents of an *.ARC file can be used in standard word-processing software. It can even be altered with an ASCII-Editor and then again be loaded with the LOAD command.

The save command can also be activated by pressing "Ctrl+S".

"Execute"

A file name is asked for and then checked for validity. Any file which was previously recorded with the "Note" function, may be read and executed. If the file name is invalid or non-existent, an error message is shown and the execute command is aborted.

"Note"

It is possible to record all activities between the ARCOFI and ARCOS-SP PLUS. The feature "Note" can be turned on or off to record all actions in a pre-named file.

To implement "Note" the user has to activate the pull-down menu. When "Note" is active, the menu command will have a check mark to the left of it. Once active, one has to name the file and give an appropriate extension to it. The file extension depends on what one wants to record, either a sequence of commands or just a line input.

- extension *.ARC : ARCOFI sequence of commands: only ARCOFI programming
- extension *.ARS : ARCOS-SP PLUS commands; a record of every key stroke or mouse activity

The *.ARS file consists of a list of all commands that the user has entered via the ARCOS-SP PLUS dialogue mode to program the ARCOFI. It is possible to read the *.ARC file and review what was programmed. The *.ARS commands, however, are written in an ARCOS-SP PLUS specific program language to program the ARCOFI. This feature allows to run a test pattern several times without looking at the file, thereby saving time.

"DOS Shell"

"DOS Shell" is provided for calling the operating system. It is possible to toggle back and forth between ARCOS-SP PLUS and the DOS command level. The following actions are carried out:

- the screen in ARCOS-SP PLUS is completely stored as it is,
- the DOS operating system is called,
- when returning to ARCOS-SP PLUS, the screen reappears just the way it was left before.

"Exit"

To leave the ARCOS-SP PLUS program, use the "Exit" command or just type a "Q" in the command line.

9.2.2.3 Pull-Down Menu "ARCOFI"

"READ ARCOFI"

The command READ ARCOFI reads the complete device. If the coefficients of the ARCOS-SP PLUS software are not identical to the coefficients in the ARCOFI, the current window as well as the status line are corrected.

This command can also be activated by pressing "Ctrl+R".

"WRITE ARCOFI"

With the WRITE ARCOFI function the ARCOS-SP PLUS software coefficients which are displayed on the screen are written to the ARCOFI. In general, this is always done automatically by the software, but the WRITE ARCOFI command allows to write all coefficients at once a second time.

This command can also be activated by pressing "Ctrl+W".

9.2.2.4 Pull-Down Menu "Show"

This feature enables the user to switch between various windows in the user area to show the device parameters that are read from the chip and to manipulate them. The following windows can be displayed (refer to **chapter 9.2.3**):

- CRAM (Coefficient RAM)
- Register
- ARCOFI
  - AFE (Analog Front End)
  - ADI (ARCOFI Digital Interface)
  - ASP (ARCOFI Signal Processor)
    - Tone-Generator
    - DTMF-Generator
    - Speakerphone (PSB 2163 only)
      - SD-Transmit (Speech Detector)
      - SD-Receive (Speech Detector)
      - SC-Acoustic (Speech Comparator for the acoustic echo)
      - SC-Line (Speech Comparator for the line echo)

9.2.2.5 Pull-Down Menu "Board"

This menu serves for changing the configuration of the Mainboard, setting the signalling channel and choosing the ARCOFI device (interface mode and chip address).

"A-Chip/B-Chip"

These two menu items can only be selected when the IOM2-mode is activated. In this case switching between two devices via software is possible. If the serial interface mode was selected (SPI Serial Programming Interface; SCI/SDI) this feature is not available.

"Signalling"

This menu listing allows to set the bits in the C/I channel 1. Please note, that this menu item is only available in the IOM-2 TE mode of the ARCOFI-SP. The setting of the bit CAM in the GCR-register influences the bit positions in the signalling window (refer e.g. to the PSB 2162 User's Manual, **chapter 3.4.3**).

9.2.2.6 Pull-down Menu "Options"

A variety of options exists with the ARCOS-SP PLUS software. It is possible to set the colors, the sensitivity of the mouse, the beeper (ON/OFF), the tone frequency of the error beep, the double borders for the menu (ON/OFF) and the shadow effect (for the windows).

9.2.3 The User Area

Working with the User Area

The user area is the portion of the screen between row 2 and 23 (see **figure 9.2.2**). In this area different background items can be displayed and manipulated with the mouse. The screen contents of the user area can be chosen either with the menu item "Show" from the main menu or simply by clicking at different boxes inside the user area with the left mouse button.

Being in the user area of ARCOS-SP PLUS, only a click with the left button of the mouse will activate the different fields.

A field can have three different states:

- ON: the border and contents of the field are highlighted
- OFF: the border and contents of the field are dimly displayed
- ERROR: the border and contents of the field are displayed in red

The left and right mouse buttons have different meanings. The **left mouse button** is used to program a field or used to zoom into another window. A double click with the left button turns a field ON/OFF and at the same time programs the corresponding bit in the configuration register. The **right mouse button** is used to read a field and to show the coefficients in hexadecimal code, i.e. as they have to be written into the ARCOFI.

Initializing the Hardware

Before it is possible to work with the user area either the external hardware must be initialized (click at the field "Initialize Hardware", compare with **figure 9.2.2**) or it must be disabled (field "Disabled"). With a disabled hardware the ARCOS-SP PLUS software can be used to evaluate ARCOFI coefficients without influencing any external hardware containing the ARCOFI. If the hardware is successfully initialized, any programming action will also concern the ARCOFI.

The hardware is initialized as soon as the initialization field in the ARCOFI-SP window is clicked upon or when the ARCOFI is accessed. Access takes place either with a "Read" command or with a "Load" command. In this case the hardware will be programmed completely with the ARCOS-SP PLUS conditions displayed on the screen.

The status line contains information about the kind of ARCOFI that has been detected (PSB 2161 or PSB 2163) and if external hardware is connected via the serial interface any activity at this interface is indicated as well ("RS232 active").

In **chapter 9.4** a description of the different setups depending on the external hardware can be found.

Changing Registers and Coefficients in the User Area

Functions or switches can be activated simply by clicking upon the desired, double framed fields. This is equivalent to the bit combinations in the registers as they can be found in the register window. For example the sidetone gain stage GZ can be activated by setting the GZ bit in the register window or simply with a double click at the GZ box in the user area. Another example is the DTMF bit. This bit can be activated with a single click on the DTMF switch in the user area.

A coefficient like the sidetone gain coefficient required for GZ can be programmed with a single click at the GZ box in the user area. As a result, a pop-up window appears which offers all possible values. Should the desired value not be shown, one can scroll through the list by clicking upon the small up and down arrows located at the top of the frame surrounding the coefficient values. It is also possible to type in the desired value. The program automatically chooses the closest value available. If the value of the coefficient is unknown, then two question marks will be shown. The entered coefficient must carry the same unit as the main header of the window.

These explanations apply to all bits and coefficients. In general, the user area is self-explanatory and can also be used to become familiar with the architecture of the ARCOFI. However, the generation of coefficients for the FX- and FR-filters is a bit more difficult to understand and will be explained separately in **chapter 9.3**.

The Register Window and the CRAM Window

For experienced users, the two windows "Register" and "CRAM" offer the possibility to change almost every bit or coefficient of the ARCOFI with the help of only two different screen masks. Everything that can be done in the other windows of the user area can be done with the register and CRAM window instead. Using the right mouse button in the register and CRAM window shows the complete programming sequence that is required for the actual setting of the ARCOFI.

Clicking upon register bits makes them toggle or a pop-up window appears. CRAM coefficients can also be altered by clicking upon them. A double click at one of the coefficients causes ARCOS-SP PLUS to switch to the corresponding window in the user area. For example a double click at the parameter ATT in the CRAM window activates the speakerphone window (PSB 2163 only).

9.2.4 The Command Line

Introduction

It is highly recommended to use a mouse to work with the ARCOS-SP PLUS software, but it is also possible to enter all inputs via the keyboard. All commands have to be entered in the command line (see **figure 52**).

This chapter gives a complete description of all inputs that can be done in the command line. Of course the speakerphone commands take only effect with the PSB 2163. The command line is not case sensitive. The F3 key can be used to recall the last command.

ARCOS-SP PLUS Commands

Show	**ASP** | **Reg**[ister] | **ARCOFI** | **AFE** | **ADI** | **CRAM** | **Tone**[generator]| **DTMF**[generator] | **Spe**[akerphone] | **SDT**[ransmit] | **SDR**[eceive]
W[rite]	**ARCOFI**
R[ead]	**ARCOFI**
Board	{ **A**[-][Chip] | **B**[-][Chip]} | {**B1** | **B2**} | **Sig**[nalling] [<Hex><Hex>] | **En**[abled] | **Dis**[abled] | **Init**[ialise]}
Load	<Filename>
Save	<Filename>
Note	<Filename>
Exec[ute]	<Filename>
Delay	<Time>
DOS	
Exit	
Q[uit]	

Commands for Setting Coefficients

<Command>	**<Coefficient>**	**[<Coefficients Set>]**
DTMF	<Float><Float>[<Float><Float>]	F3, G3, [FD, GD3]
F[T]	<Float> <Float>[<Float>]	F1, F2, [F3]
FS	<Float> <Float>[<Float>]	F1S, F2S, [F3S]
G	<Float> <Float>[<Float>]	G1, G2, [G3]
GD	<Float> <Float>[<Float>]	GD1, GD2, [GD3]
T	<Float> <Float>[<Float>]	T1, T2, [T3]
FX	<**OptimMode**> <Files> <**OptimSpeed**>	
FR	<**OptimMode**> <Files> <**OptimSpeed**>	

Coefficients

GX	**| GR**	**| GZ**		
TOn	**| TOff**			
F1[T]	**| F2[T]**	**| F3[T]**		
F1S	**| F2S**	**| F3S**	**| FD**	
G1	**| G2**	**| G3**		
GD1	**| GD2**	**| GD3**		
T1	**| T2**	**| T3**		
A1	**| A2**	**| K**	**| GE**	
GAE	**| GLE**	**| ATT**	**| ETAE**	**| ETLE**
TW	**| DS**	**| SW**		
GDSAE	**| PDSAE**	**| GDNAE**	**| PDNAE**	
GDSLE	**| PDSLE**	**| GDNLE**	**| PDNLE**	
LIM	**| OFFX**	**| OFFR**		
LP2LX	**| LP2LR**	**| LP1X**	**| LP1R**	
PDSX	**| PDNX**	**| PDSR**	**| PDNR**	
LP2SX	**| LP2NX**	**| LP2SR**	**| LP2NR**	
LGAX	**| LGAR**			
COMX	**| AGX**	**| TMHX**	**| TMLX**	**| NOISX**
COMR	**| AGR**	**| TMHR**	**| TMLR**	**| NOISR | AAR**

Extended Commands

Po[wer] Down

Po[wer] Up

Re[set]

Configuration Setting Commands

S[et]	<CRBit>	[0 | 1 | I | II | ALw | uLw | in | out | SQ | TR]
C[lr]	<CRBit>	
S[et]	VDM <Hex>	
C[lr]	VDM	
S[et]	**MIC|AMI**	[down | by [-pass]| 0 | 6 | 12 | 18 | 24 | 30 | 36 | 42]
C[lr]	**MIC|AMI**	

S[et]	**AIMX**|**AIN**[-MUX]	[MIP1[|MIN1]|MIP2[|MIN2]|MI3]
C[lr]	**AIMX**|**AIN**[-MUX]	
S[et]	**HOC**|**AHO**	[down | by [-pass] | 2.5 | -3.5 | -9.5 | -15.5 | -21.5]
C[lr]	**HOC**|**AHO**	
S[et]	**LSC**|**ALS**	[down | by [-pass] | 11.5 | 8.5 | 5.5 | 2.5 | -0.5 | -3.5 | -6.5 | -9.5 | -12.5 | -12.5 | -15.5 | -18.5 | -21.5]
C[lr]	**LSC**|**ALS**	
S[et]	**DLTF**	[NOT | IDR | DLP | DLS | DLN]
C[lr]	**DLTF**	
S[et]	**Tone**[generator]	
C[lr]	**Tone**[generator]	
S[et]	**Spe**[akerphone]	
C[lr]	**Spe**[akerphone]	
S[et]	**AGCX**	
C[lr]	**AGCX**	
S[et]	**AGCR**	
C[lr]	**AGCR**	
S[et]	**Comp**|**Exp**|**VDM**	
C[lr]	**Comp**|**Exp**|**VDM**	
S[et]	**{ GCR | DFICR | PFCR | TGCR | TGSR | ATCR | ARCR | TFCR | SDICR | XCR } <Hex><Hex>**	
C[lr]	**GCR | DFICR | PFCR | TGCR | TGSR | ATCR | ARCR | TFCR | SDICR | XCR**	

Low-Level Setting Commands

W[rite] [**0**|**1**]	<WCommands>
R[ead]	<RWCommands>

Print Commands

P[rint]	DTMF | CRAM | AFE | ADI |Tone[generator]| Spe[akerphone]| AG[CX] | AG[CR] | Reg[ister] | GX | GR | GZ | Exp[&VDM] | Comp
P[rint]**FX**	Freq[uency]|Res[ult]|<OptimMode> <Files> <OptimSpeed>

Command Parameters

<**CRBit**> SP | AGCX | AGCR | EVX | SLOT | PU | CAM | ESIG | LAW | SD | SC | SB | SA | VDM3 | VDM2 | VDM1 | VDM0 | GX | GR | GZ | FX | FR |DHPR | DHPX | TG | DT | ETF | CG | BT | BM | SM | SQTR | PM | TRL | TRR | DTMF | TRX | MIC3 | MIC2 | MIC1 | MIC0 | EVREF | AIMX1 | AIMX0 | HOC2 | HOC1 HOC0 | CME | LSC3 | LSC2 | LSC1 | LSC0 | DHS | EPZST | ALTF2 | ALTF1 | ALTF0 | DLTF2 | DLTF1 | DLTF0 | EPP | DCE | MCLKR2 | MCLKR1 | MCLKR0 | PGCR | PGCX | RAAR | OBS | DHOP | DHON | DLSP | DLSN

<**RWCommands**> SOP_0 | SOP_1 | SOP_2 | SOP_3 | SOP_4 | SOP_5 | SOP_6 | SOP_7 | SOP_8 | SOP_A | SOP_D | SOP_F | COP_0 | COP_1 | COP_2 | COP_3 | COP_4 | COP_5 | COP_6 | COP_7 | COP_8 | COP_9 | COP_A | COP_B | COP_C | COP_D | COP_E | COP_F

<**WCommands**> XOP_0 | XOP_1 | XOP_D | XOP_E | XOP_F

<**Files**> <Filename> [<Filename> [<Filename> [<Filename>]]]

<**Filename**> Filename with extension

<**OptimMode**> F[lat] | T[arget] | L[imited]

<**OptimSpeed**> /F[ast]| /M[iddle]| /B[est]

<**Float**> Standard Real Number

<**Time**> <Float>

<**Hex**> 0 ... F

9.3 Generating the Correction Filter Coefficients

9.3.1 Filter Implementation and Theory of Calculation

Two high performance frequency correction filters FX and FR are implemented in the ARCOFI, allowing an optimum adaption to different types of transducers or compensating the frequency response of the telephone plastics itself. Specifications of different countries can be fulfilled by means of a simple software change.

One filter consists of two equalizers with variable gain, factor of quality, and center frequency followed by a high-/low-pass filter. The filters can only attenuate the signal, they behave like passive filters. The FX or FR filter is adjusted with the help of twelve coefficients which are calculated by the ARCOS-SP PLUS software.

It is obvious, that there are different ways to configure the two equalizers and the high-/ low-pass filter to achieve one and the same frequency response. Therefore always more than one coefficient set is capable of fulfilling the desired response.

The basic idea for calculating the coefficients is, that two frequency responses are given. One represents the desired over-all frequency response (target function), the other one is the frequency response, that the hardware actually offers (input function). While the first one is usually a flat frequency response, the latter one can be measured or estimated. ARCOS-SP PLUS then calculates the filter coefficients (filter function) in a way, that the filter function plus the input function results in the target function. If for example the hardware transmits high frequencies only attenuated, it exhibits a kind of low-pass function (input function). If a flat frequency response is desired (target function) ARCOS-SP PLUS would calculate the coefficients in a way, that the FX or FR filter shows a high-pass behavior in order to compensate the input function.

Furthermore, it is not only possible to give a desired target function but also an upper and lower limit for the target function can be given.

The algorithm used for generating the filter coefficients is based on a stochastic method, similar to the law of cooling: i.e. at the beginning of the process, the parameters (here the filter coefficients) may be within a large range. This range progressively is reduced such that the parameters converge. Up to and including the 8th calculation step the quality of the approximation is defined by the mean square of the difference between the target function and the addition of the filter functions of FX or FR and the input function. Thus the discrepancy between the two curves is calculated for each sampling frequency, then it is squared, added and finally divided by the number of the sampling frequency points.

From the 9^{th} calculation step the quality of the approximation is defined by the greatest absolute difference. The algorithm shows the value of the absolute minimum and the quality of the coefficient set which is presently considered as the best solution.

In order to calculate the discrepancy properly, each amplitude curve is normalized. Before the algorithm starts, each amplitude curve is shifted such that it has an amplitude

value of 0 dB at one sampling frequency point. The reference frequency is the sampling frequency which is equal to or closest to 1000 Hz.

Note: Because the algorithm is based on a random process, different runs of the program, starting from the same input function, can give different results. It is recommended to make several runs and to take the best result (see also page 157).

9.3.2 Calculation of Coefficients

The coefficients for the FX transmit and FR receive path correction filters can be calculated either with the ARCOS-SP PLUS or with the ARCOS-SP program. Both programs generate filter coefficients and graphically display the filter transfer functions (amplitude transfer function in dB, group delay response in µs). The graphic output is only possible if the system is equipped with an EGA, VGA, CGA, or a Hercules graphics card. The transfer function can also be stored in tabular form in two separate files, one for the amplitude response (*.AMP) and one for the group delay response (*.GDY).

After clicking at the FX or FR filter box in the ASP window (ARCOFI signal processor) an dialogue box appears that offers the choice between three basic optimization modes. For each mode the optimization speed must be chosen as either “fast”, “middle” or “best”. Once the optimization mode, the selected speed of optimization and the required file names have been entered, the calculation starts.

Optimization Speed

The optimization process might require long computing time in some difficult cases, in particular a "best" fit with over 100 frequency points might take hours to be completed when using a slow PC without co-processor. It has been found that between 20 to 30 sampling points usually give a satisfactory result while keeping the calculation time reasonably short.

Optimization Mode “Flat Target Function”

For a flat frequency response, the algorithm approximates the inverted function of the input function. The input function must be declared in an input file. The file has to be entered with the filename and the extension. An example for an input file shows **table 4**.

For the FR filter a second input function can be entered (e.g. one for the handset earpiece, the second for the loudspeaker). The calculation points of this second input function are interpolated and subsequently averaged. Hereby ARCOS-SP PLUS will eliminate automatically the frequency areas which are not common in both input functions (ranges at lower and upper frequencies).

When the coefficients have been calculated, the inverse curve of the input function is displayed if a graphics screen is available. On the same graph the filter functions of FX

or FR are displayed. Both curves are shifted such that they have the same amplitude value at the reference frequency.

After having quit (using pressing carriage return or the key "Q") the discrepancy between the two curves is displayed. The graphics mode can be left by quitting a second time.

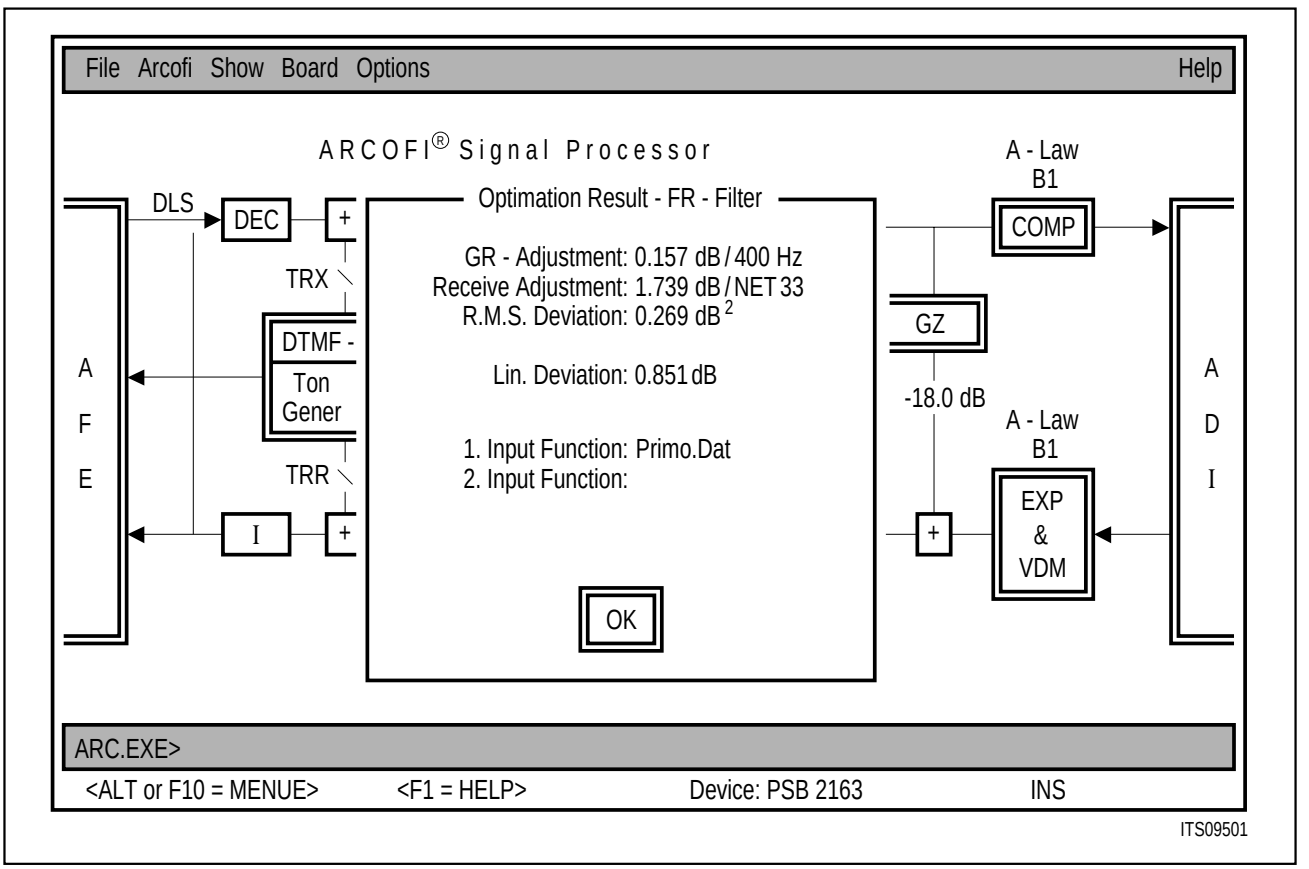


Figure 53
Screen after Calculating Filter Coefficients

The optimization result is displayed in a separate window after successful completion (see **figure 53** for an example). Here the values GR- or GX-Adjustment, r.m.s. deviation and linear deviation are displayed as well as the relevant input files. Because the FX/FR filters can be regarded as passive filters, the additional loss caused by the filter must be compensated. ARCOS-SP PLUS displays different values that represent this additional loss and are also a measure for the quality of the optimization:

- "lin. deviation" is the minimum filter loss
- "Receive Adjustment" ("Transmit Adjustment") is the filter loss weighted according to CCITT and ETSI NET33
- "GR-Adjustment" ("GX-Adjustment") is the weighted filter loss over the complete frequency range of 4 kHz
- "r.m.s. deviation" is the mean square of the difference between the filter function and the desired response

Figure 54 illustrates the meaning of these values.

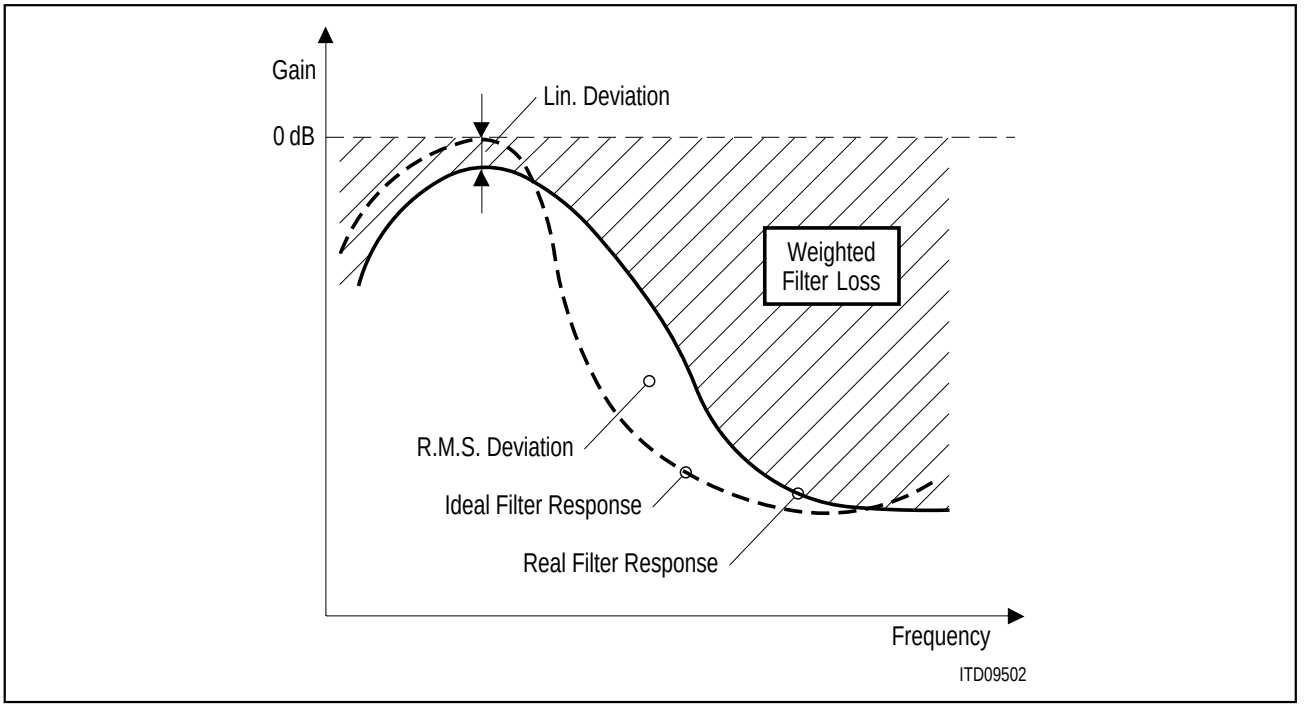


Figure 54
Illustration of Filter Loss and Deviation

Especially the "linear deviation" is a measure for the quality of the coefficient set. The lower this value, the better the approximation is. Several runs of the program can result in different values for the linear deviation because of the random starting parameters the algorithm uses. In general, it should be possible to reach a value of less than 3 dB for the "lin. deviation".

Optimization Mode "Target Function"

The algorithm tries to compensate the input function in such a way that the addition of this input function and of the filter functions of FX or FR is as close as possible to the target function. The target function must be given in a file.

Before starting the algorithm, the sampling frequency points of the target function are adjusted to the sampling frequency points of the input function. ARCOS-SP PLUS checks if each sampling frequency point of the input function has a corresponding sampling frequency point in the target file. If a sampling frequency point is not found in the file, then the amplitude value of this sampling frequency point is interpolated by making a linear approximation from the two points closest to the desired sampling frequency point. Thus the algorithm can work with two curves not having the same sampling frequency points.

If a sampling frequency point is higher than the highest point or lower than the lowest point of the target function then the algorithm considers that the frequency response can have any value at this point. These calculation sampling points are not recognized and therefore do not influence the calculation.

After the calculation of the coefficients the input functions and filter functions of FX or FR are added and the result is graphically displayed. In the same graph the target function is also shown. Both curves are shifted such that they have the same amplitude value at the reference frequency.

After quitting the discrepancy, i.e. the difference between the two curves, is graphically shown. When quitting again one leaves the graphics mode. Finally the results as described for the "flat frequency response" are displayed.

Optimization Mode "Limited by an Upper and Lower Curve"

The algorithm tries to compensate the input function such that the addition of this input function and of the filter functions of FX or FR is as close as possible to the middle of the upper and the lower limiting curves (which is then the target function). Before starting the algorithm, the target function as well as the weighting factors are calculated.

First, the sampling frequency points of the upper limit and lower limit are adjusted to the ones of the input function. Then the algorithm checks whether each sampling frequency point of the input function has a corresponding sampling frequency point in the upper and lower function. If a sampling frequency point is not found in the upper and lower curves, then the amplitude value for this sampling frequency point is interpolated by making a linear approximation from the two points closest to the desired sampling frequency point. Finally for each frequency point the mean of the upper and the lower limit is calculated. These mean values describe the target function.

If a sampling frequency point is higher than the highest point or lower than the lowest point of the upper and lower limiting curve, then the algorithm considers that the frequency response can have any value at this point. These calculation samples would not be recognized.

The ratio of the longest and shortest distance between the upper and the lower limiting curves (for one frequency) defines the size of a weighting factor. The shorter the distance between the limiting curves, the better the correction, the larger the weighting factor. The weighting factor is taken into consideration when calculating the greatest absolute difference as well as the mean of the square of the difference.

After the calculation of the coefficients, the input function and the filter functions of FX or FR are added and the result is graphically displayed. In the same graph the upper and lower limits are also shown. The curves are shifted in such a way, that the input function and the target function have the same amplitude value at the reference frequency.

Finally the mean square of the difference and the other values described above, are displayed.

File Format

A maximum of up to 100 frequency/amplitude points can be used by the approximation algorithm. The frequency points must be in progressing order between 1 Hz and 3999 Hz. The amplitude values should be limited to a maximum of |20| dB although this is not required for the fitting algorithm.

The software expects one pair of values (frequency and level) in one line, both values separated by one or more blanks and/or tab-stops. The first value must be the frequency, the second one the level. Units are Hz and dB; they are not part of the file. Numbers can be integer or real (e.g. 3 or -3.1 are allowed). **Table 4** shows an example for an input file.

Table 4
Example for an Input File; First Column: Frequency (Hz); Second Column: Level (dB)

300	– 1
700	– 1
800	– 0.5
1000	0
1050	0.1
1200	0.5
1250	0.75
1300	1
1350	1.25
1400	1.5
1450	1.75
1500	2
1700	3.75
1750	4.25
1900	5.5
2250	6.9
2550	7.45
3000	8
3250	6.75
3350	6.25

9.3.3 Reading the FX and FR Filters

A click with the right mouse button (or the input `Print FX` or `Print FR`) at the command line) invokes the read window for the filters. This window is a blend between an input and an output window. There are three fields which can be clicked upon and one entry field to enter a file name. If one clicks upon the field "Frequency Response", then the frequency and phase response of the filter are shown in a graphical format. If one chooses the field "Optimization", the three values of the last calculation and the file name are shown (optimization result window). With a click on the "Check Optimization" field, the same window is displayed that appears after programming the filters (see **figure 53**), but the coefficients are not recalculated, instead the result of the optimization is taken. If it is desired that the frequency response is saved in a separate file, the file name has to be entered in this window.

9.3.4 Examples for the Usage of the FX/FR Filters

9.3.5 Adapting the FX Filters to a Target Frequency Response

The use of the FX filter to match a required mask template will be highlighted in the following example.

According to the European Telecommunications Standards Institute (ETSI) standard, the sending sensitivity and frequency response from the mouth reference point (MRP) to the digital interface shall be within a mask template given in **table 5**.

Table 5
Mask Template according to ETSI

Frequency (Hz)	Upper Limit (dB)	Lower Limit (dB)
100	– 12	
200	0	
300	0	– 12
1000	0	– 6
2000	4	– 6
3000	4	– 6
3400	4	– 9
3999	0	

The sampling points (in units of Hz and dB) of the upper and the lower limits are written into a text file with the help of an editor. The first column contains the frequency values in Hz, the second column contains amplitude values in dB (refer also to **table 4**). The units themselves are not inputs, they are generated by ARCOS-SP PLUS.

The names chosen for the files in this example are UPPER.LIM and LOWER.LIM.

Table 6
Listing of Boundary Curves (in Hz and dB)

Upper Curve		Lower Curve	
		300	– 12
1000	0	1000	– 6
2000	4	3000	– 6
3400	4	3400	– 9

The frequency response of the microphone can be measured. The sampling points are also input into a text file. For example it is assumed, that the appropriate file is PRIMO.DAT as shown in **table 4**. Because frequencies under 300 Hz and above 3400 Hz are blocked by the ARCOFI filters, only the sampling points in the range 300 Hz – 3400 Hz should be entered in the file. In order to obtain a good approximation, at least 20 points between 300 Hz and 3400 Hz should be selected. However, not more than 100 points should be entered.

After having entered the measurement points, the program ARCOS-SP PLUS is called. When in the ASP-Window, a click with the left mouse button upon the FX field opens a display where the input files, the optimization mode and the optimization speed have to be selected. For this example the optimization mode "limited by an upper and a lower curve" must be chosen. The input function is the file called PRIMO.DAT, the upper and lower curves are given with the files UPPER.DAT and LOWER.DAT. A click upon the "OK" field starts the calculation.

At the end of the approximation process the frequency response of the microphone (input function) and that of the FX correction filter (filter function) are added and the sum is displayed together with the two limiting curves. Notice that the curves are shifted. The value of the amplitude at the reference frequency (1000 Hz in the example) is 0 dB. The two limiting curves are shifted such that the mean value of the limiting curves at the reference frequency is 0 dB.

As already described, the linear deviation of the filter function is a indication of the quality of the coefficient set. The calculation in this example should be done several times until a set of coefficients is found, that results in a deviation of less than 2 dB.

9.3.5.1 Using the "Execute" Feature to Calculate Coefficients

The process of starting the filter calculation several times and checking the results after each calculation can be eased by using the "Execute" function of ARCOS-SP PLUS. With the help of an appropriate *.ARS file, the software calculates as many sets of coefficients as desired and allows to check the optimization result afterwards.

To understand the contents of the *.ARS file it is necessary to remember the command line syntax of ARCOS-SP PLUS, as far as it is required for the FX/FR filters:

FX <OptimMode> <Files> <OptimSpeed>

FR <OptimMode> <Files> <OptimSpeed>

<OptimMode> : **F**[lat] | **T**[arget] | **L**[imited]

<OptimSpeed> : **/F**[ast] | **/M**[iddle] | **/B**[est]

<Files> : <DATFile> [<DATFile> [<LIMFile> [<LIMFile>]]]

<DATFile> : Filename containing an input function

<LIMFile> : Filename containing an upper/lower limit

A simple example illustrates the use of the "Execute" function. It is assumed that the FX filter should compensate the frequency response given with a file called PRIMO.DAT. The desired response is "flat" and the optimization mode is "best". The following steps have to be performed:

- With the help of an ASCII editor a file with the extension *.ARS has to be prepared, that contains two lines of text for each set of coefficients to be calculated; one line tells the ARCOS-SP PLUS software to do the calculation, the second line is used to save the result in an *.ARC file; **figure 55** shows the contents of such an *.ARS file, it is called CALC.ARS; the combination of "FX...SAVE" must be repeated as many times as sets of coefficients are to be calculated.
- In a second step an *.ARS file has to be prepared to check the previously stored *.ARC files; see **figure 56** for an example, here the file is called CHECK.ARS.
- Now the ARCOS-SP PLUS software is started and the menu item FILE, EXECUTE is chosen; the name of the first *.ARS file is given (e.g. CALC.ARS) and the calculation starts; depending on the optimization speed and the number of coefficient sets, this can take quite a long time but the calculation is performed automatically and needs no interaction from the keyboard.

- when the calculation is completed, the previously saved *.ARC files can be loaded separately by using the "Load" command, or the second *.ARS file (CHECK.ARS) is used to load all the files one after the other and to inspect especially the "lin. deviation"; the best approximation is taken as a final result then.

```
FX          Flat primo.dat      /B
SAVE        result01.ARC
FX          Flat primo.dat      /B
SAVE        result02.ARC
FX          Flat primo.dat      /B
SAVE        result03.ARC
```

Figure 55
Contents of the File CALC.ARS (calculation for 3 sets of coefficients shown)

```
LOAD result01.ARC
Print FX Result
LOAD result02.ARC
Print FX Result
LOAD result03.ARC
Print FX Result
```

Figure 56
Contents of the File CHECK.ARS

9.4 Hardware Setup for Use with ARCOS-SP PLUS

9.4.1 Introduction

The ARCOFI is able to work in three different interface modes:

- IOM-2 TE interface (1.536 MHz)
- IOM-2 NON-TE interface (4.096 MHz)
- Serial control / serial data interface (SCI/SDI)

The ARCOS-SP PLUS supports each of these three interface modes in conjunction with appropriate hardware. This chapter describes the different hardware setups. First the ARCOFI has to be connected to the particular hardware which must be configured correctly. Then the ARCOS-SP PLUS software is called and informed about the hardware configuration. With a click at the "Initialize Hardware" box the hardware is checked and initialized for the use with ARCOS-SP PLUS. The ARCOFI itself can be located either on the SIPB 5133-SP evaluation board, on a SIPB 5132-SP telephone, or on a dedicated board like the SIPB 8051 telephone board. Also custom specific boards with an IOM-2 interface are suitable.

In the "Show ARCOFI" window in the user area of ARCOS-SP PLUS, the following modes can be set if the hardware support is enabled (compare with **figure 52**):

- either the **ICC/ISAC** as a layer 1/2 device, or the **EPIC/ELIC**
- either **IOM** interface mode, or **SPI** interface mode (SCI/SDI interface)
- either **A**-Chip or **B**-Chip (only possible in IOM2 interface mode)

These settings must correspond to the hardware that is connected to the PC on which the ARCOS-SP PLUS software runs.

9.4.2 Using the SIPB 5000 System

The ARCOS-SP PLUS software requires a specific SIPB 5000 hardware environment. The firmware EPROM version 1.1 or newer must be installed on the SIPB 5000 mainboard. Three standard configurations are described in the next paragraphs. More detailed information can be found in the technical description of the SIPB 5000 system.

Please note, that if the ICC-B is used as a layer 2 device, EPROM version 2.2 or newer is required for the SIPB 5000 mainboard.

IOM®-2 TE Interface with an ISAC-X

A common setup uses the SIPB 5100 (ISAC-S Module) or the SIPB 5103 (ISAC-P Module) as layer 1/2 module. The ARCOFI is connected via a SIPB 5130 (Audio Module). **Figure 57** shows the general setup either with an ISAC-S or with an ISAC-P Module. The ARCOFI is located on a SIPB 5132-SP telephone, but instead of the telephone any hardware which offers an IOM-2 interface can be connected.

For the use with ARCOS-SP PLUS the fields **ICC/ISAC** as well as **IOM** must be activated.

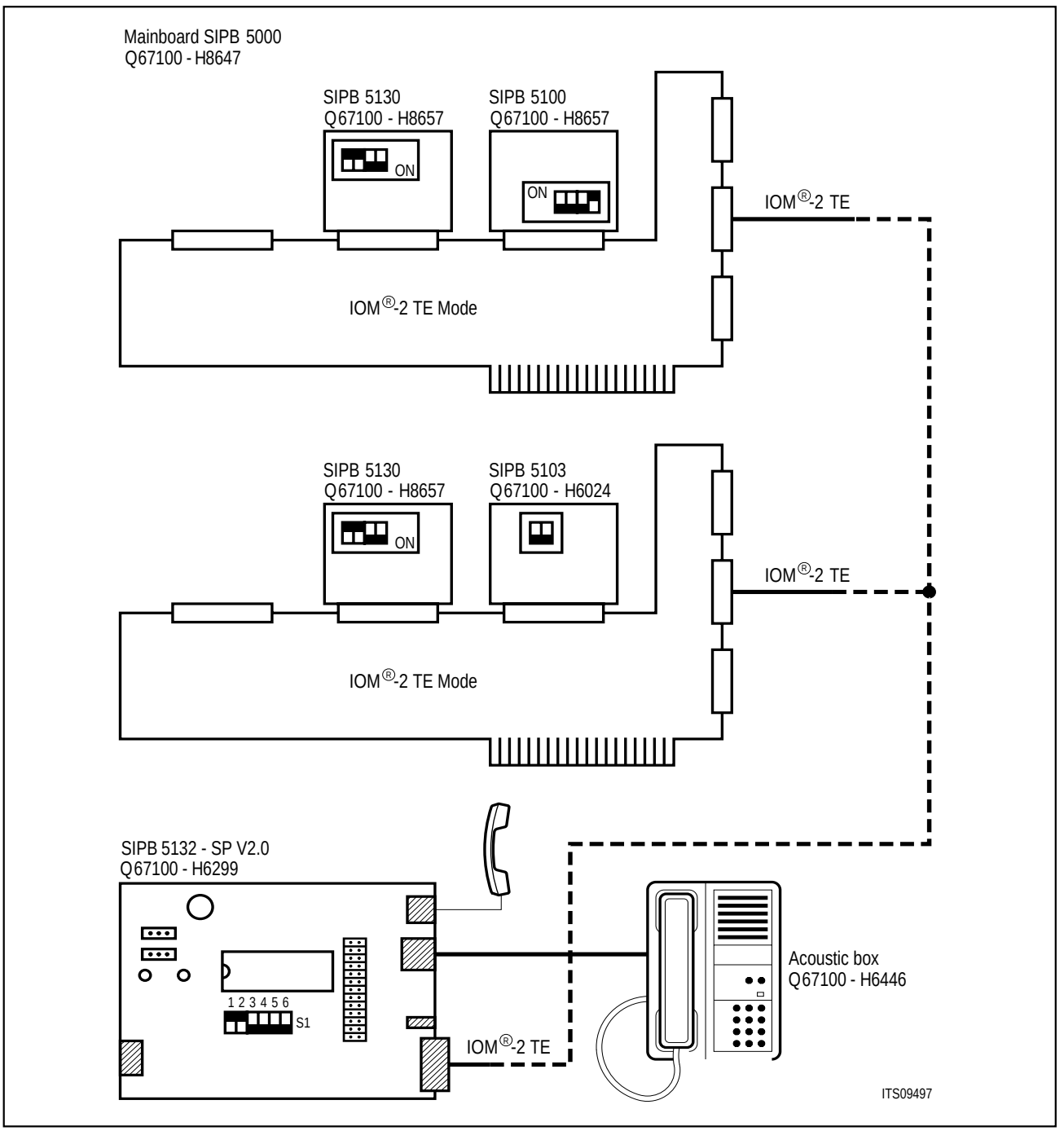


Figure 57
Setup for IOM®-2 TE Mode with the ISAC-X in TE-Mode

The ISAC-X runs in TE-mode and the B channels are switched to the S_0 bus or the U_{P0} bus respectively. Therefore the setup in **figure 57** can be connected to an NT simulator consisting of another SIPB 5000 mainboard with another ISAC-X in LT-S mode and a voice connection can be established.

IOM®-2 NON-TE Interface with an EPIC®/ELIC®

The 4.096 MHz IOM-2 NON-TE interface can also be used if a Linecard-Module SIPB 5121 is connected to the SIPB5000 mainboard. Optionally, this configuration offers the possibility to do measurements with the PCM4 measuring instrument from Wandel&Goltermann which has to be connected with the help of an PCM4 adapter SIPB 5311. **Figure 58** shows the setup with the ARCOFI placed on the SIPB 5133-SP ARCOFI-SP evaluation board. Due to the relatively high clock frequencies it is necessary to keep the cable length between the mainboard and the evaluation board (or any other hardware platform containing the ARCOFI-SP) as short as possible. This also applies to the cable between mainboard and PCM4 adapter.

Table 7
Timeslot Assignment for Measurements with the PCM4

Timeslot PCM4	IOM-2 Channel
TS1	B1
TS2	B2

Since the IOM-2 NON-TE interface offers eight channels, it is important to know that the ARCOS-SP PLUS software supports channel 7 (the last one) and therefore the ARCOFI must be pin-strapped to this channels. This can easily be done by setting the DIP-switches on the ARCOFI-SP telephone board V2.0 accordingly. For measurements with the PCM4 measurement device the B1 and B2 channel are switched to timeslot 1 and 2 (**table 7**).

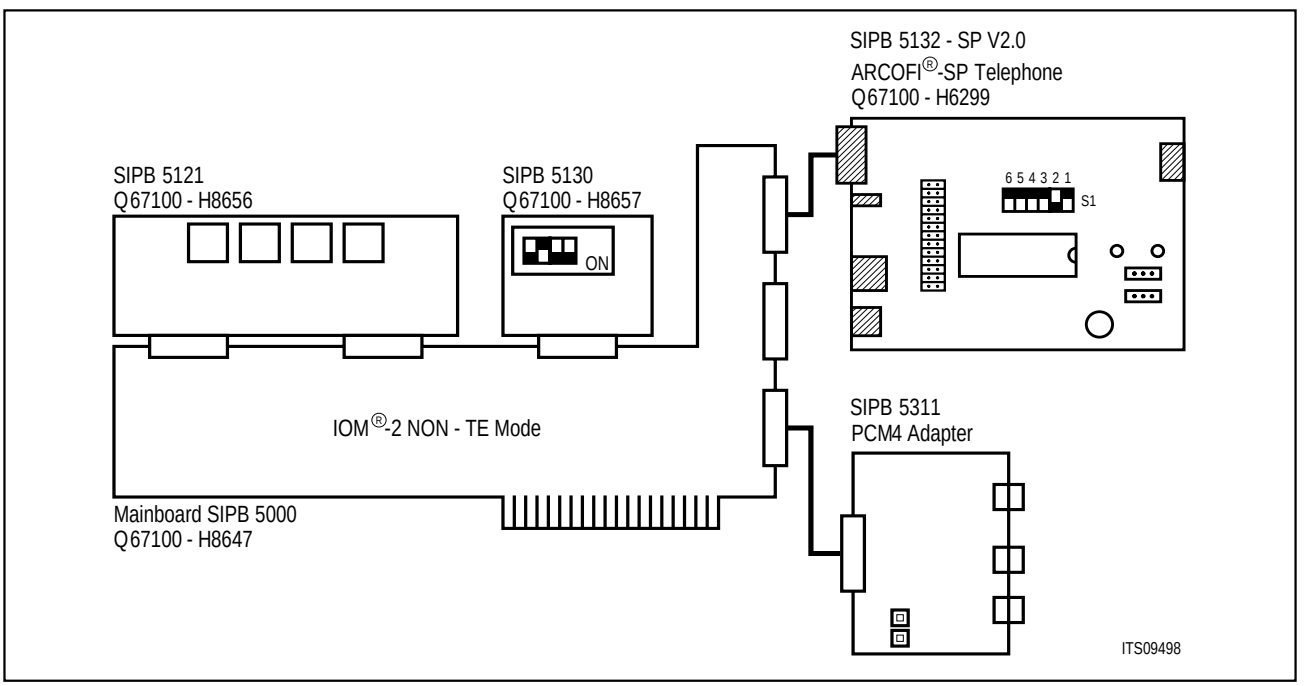


Figure 58
Setup for IOM®-2 NON-TE Mode with the Linecard Module

9.4.3 Other Hardware Tools

The ARCOS-SP PLUS software is able to communicate with different evaluation boards via the serial interface port of the PC. The following boards are supported:

- PERCOFI-Board STUT 2000; the ARCOFI is programmed with the help of an EPIC in IOM-2 TE mode
- Smart Link Kit SISI1097; the SCI/SDI interface of the ARCOFI is used
- ISDN Telephone Board SIPB8051; the ARCOFI is programmed by an ISAC-X in IOM-2 TE mode

In order to enable the software to communicate with the boards, a special firmware version is required for the evaluation boards. This firmware must be loaded to the target hardware before the ARCOS-SP PLUS software is started. **Table 8** shows the names of the HEX-files with the special firmware versions and the names of the batch files used to download the HEX-files. The download itself is performed by the utility SIMPLV24.EXE which is called from the batch files.

Table 8
Hardware to be Connected to the Serial Interface

Hardware Platform	Required Firmware	Batch File for Download	Required RS232 Cable
PERCOFI-Board STUT 2000	PERCOFI.HEX	LPERCOFI.BAT	null-modem
Smart Link Kit SISI1097	SMART.HEX	LSMART.BAT	serial 1:1
ISDN Telephone Board SIPB 8051	SIPB 51.HEX	LSIPB.BAT	null-modem

Table 9
Configuration to be made in the User Area of ARCOS-SP PLUS

Hardware Platform	Hardware Switches in the User Area	
PERCOFI-Board STUT 2000	EPIC/ELIC	IOM
Smart Link Kit SISI1097		SPI
ISDN Telephone Board SIPB8051	ICC/ISAC	IOM

Therefore the procedure for starting ARCOS-SP PLUS for the use with one of the hardware platforms given in **table 8** is the following:

- Connect the hardware with an appropriate cable to the PC (the cable is delivered together with the hardware).
- Make sure that the correct serial port is chosen (default: COM1, see paragraph "choosing the COM port" for more information).

- Make sure that the hardware is in "loader mode" (see board documentation; switching between "loader mode" and "program" is performed with the reset button on the board).
- Download the firmware (batch file according to **table 8**)
- Make sure, that the board is switched to "program mode"; this is done automatically after the download, except for the Smart Link Kit where the reset button must be pressed once (the loader LED on the SmartLink board has to be inactive then)
- Start ARCOS-SP PLUS in the serial interface mode; this is done by adding the switch /V to the command line input; the syntax is:
  `ARC [IniFile[.xxx]] /V`
  When started with this option, the ARCOS-SP PLUS software ignores any SIPB 5000 based hardware and scans the serial port for the presence of one of the boards from **table 8** instead.
- After quitting the hardware message ("board xxx found at the serial port") the usual window appears in the user area; in this window the hardware switches must be set according to **table 9** before the "initialize hardware" field has to be activated

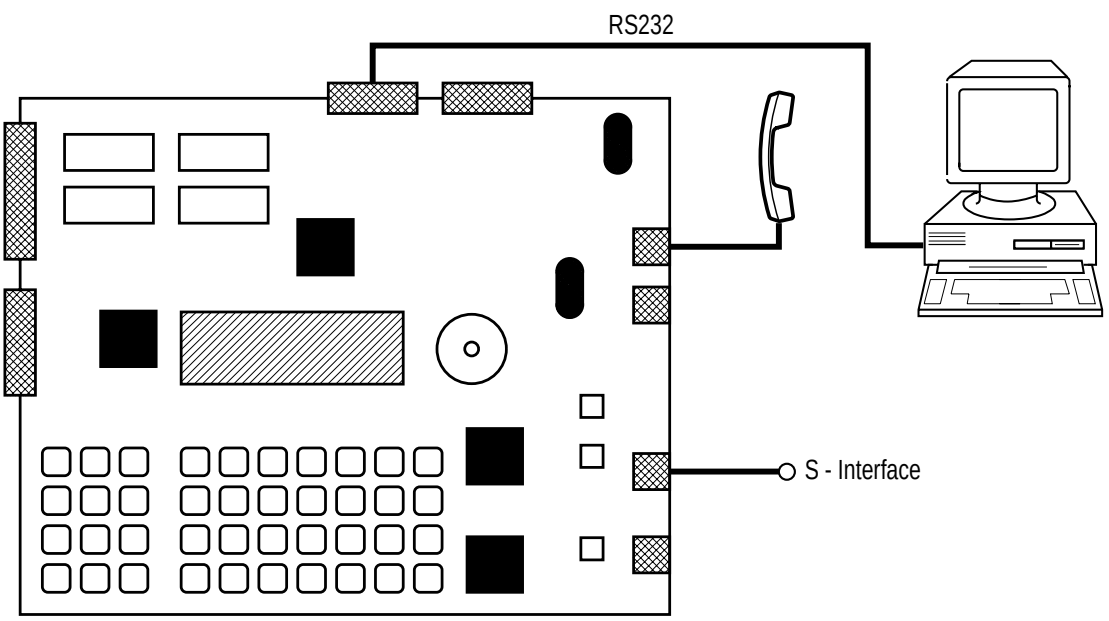


Figure 59
Setup for the SIPB 8051 Telephone Board

The **figures 59, 60, and 61** show the setup for the different kinds of hardware. With the SIPB8051 Board the B channels are switched to the S interface as well as with the Smart Link Kit the B channels are transferred over the U interface. Therefore in conjunction with an NT-simulator, a voice connection can be established.

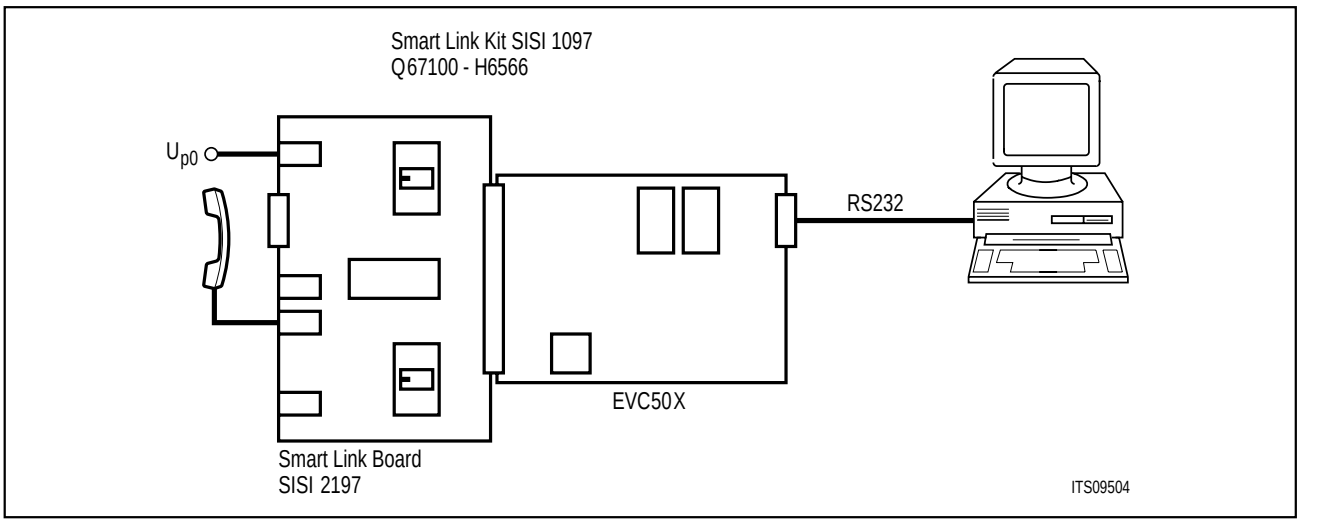


Figure 60
Setup for the Smart Link Kit

The STUT 2000 PERCOFI Board is mainly intended for measuring purposes and can directly be connected to the PCM4 measurement device from Wandel&Goltermann, but nevertheless it can be used to provide an IOM-2 interface for the SIPB 5132-SP telephones equipped with the PSB 2163/61. The timeslot assignment for measurements with the PCM4 measurement device is given in **table 10**.

Please note, that especially together with the STUT 2000 board, the programming of all the coefficients over the serial interface takes significantly longer than with the SIPB 5000 system. When the ARCOS-SP PLUS software accesses the serial port, the message "RS232 active" appears in the status line.

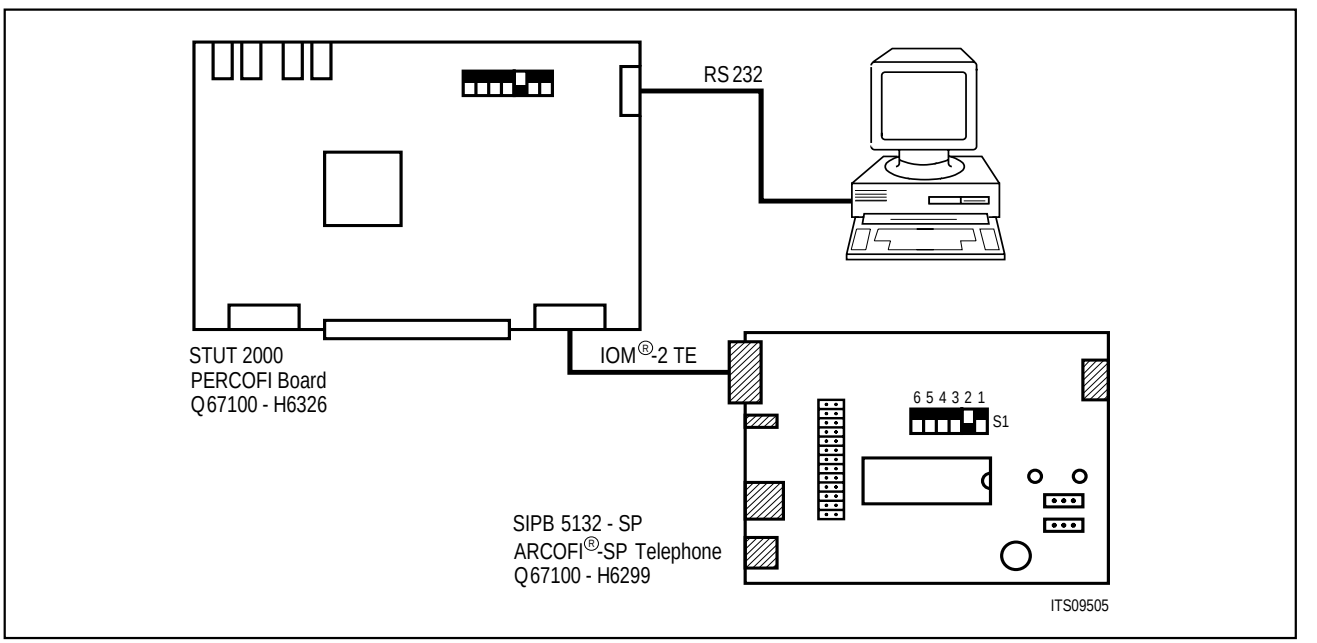


Figure 61
Setup for the STUT 2000 PERCOFI Board

Table 10
Timeslot Assignment for Measurements with the STUT 2000 Board and the PCM4

Timeslot PCM4	IOM-2 Channel
TS1	B1
TS2	B2
TS3	IC1
TS4	IC2

Choosing the COM Port

There are two different programs that have to access the serial port. First of all the ARCOS-SP PLUS software itself, but also the SIMPLV24.EXE utility for downloading the firmware.

The serial port number for ARCOS-SP PLUS is defined in the RS232.INI file. This file can be altered with the help of an ASCII editor (default is COM1).

The serial port number for the download of the firmware is given as a command line argument for SIMPLV24.EXE. If no option for the COM port is given, the utility uses COM1, otherwise the option /P<n> must be added, where <n> is the number of the COM port. For this purpose it is convenient to edit the corresponding batch file (see **table 8**) and to add e.g. the option /P2 for COM2.

9.5 Error Messages and Troubleshooting

This chapter does not offer an complete overview of all error messages since most of them are self explanatory. Instead, it gives some hints to locate the problems that are most likely to occur.

9.5.1 Hardware related Problems

Message: "Configuration of the Mainboard not supported"

ARCOS-SP PLUS has tried to initialize the hardware but is not able to recognize the hardware configuration that is currently set with the switches in the user area and/or with the /V switch in the command line.

Check the configuration of the external hardware (including DIP-switches and jumpers); does the setting in the user area match with the hardware configuration?; reset the hardware (reset button), terminate ARCOS-SP PLUS and try it again.

Message: "No ARCOFI found"

The hardware is successfully initialized but it is not possible to establish a connection with the ARCOFI-SP.

Check the connection between hardware and ARCOFI (e.g. the IOM2 cable between the SIPB 5000 mainboard and the SIPB 5133-SP Evaluation Board). Is the ARCOFI in the correct interface mode (DIP-switches on the SIPB 5133-SP Evaluation Board)? Is the IOM-2 cable defect or too long? Again a good idea is to reset the hardware, terminate the software and to try it a second time.

Message: "No A-Chip found"

ARCOS-SP PLUS expects to work with an ARCOFI whose address is $A1_H$ (A-Chip) but does not get a response from an A-Chip.

Check the DIP switch on the hardware determining the chip address (SW 1: ON on the SIPB 5133-SP Evaluation Board) or measure the logic level at pin 25 (AD-pin), it must be low.

Message: "No B-Chip found"

ARCOS-SP PLUS expects to work with an ARCOFI whose address is $B1_H$ (B-Chip) but does not get a response from an B-Chip.

Check the DIP switch on the hardware determining the chip address (SW 1: OFF on the SIPB 5133-SP Evaluation Board) or measure the logic level at pin 25 (AD-pin), it must be high.

Message: "This version of the A-Chip is not supported" or
"This version of the B-Chip is not supported"
"This version of the ARCOFI is not supported"

ARCOS-SP PLUS has detected an PSB 2160, or PSB 2165, or an other device, but not the PSB 2163 nor the PSB 2161.

Message: "No ICC/ISAC found"

The field "ICC/ISAC" is activated but ARCOS-SP PLUS cannot find an ICC or an ISAC-S or an ISAC-P on the external hardware.

Check the configuration of the external hardware (including DIP-switches and jumpers); does the setting in the user area match with the hardware configuration?

Message: "No EPIC/ELIC found"

The field "EPIC/ELIC" is activated but ARCOS-SP PLUS cannot find an EPIC or an ELIC on the external hardware.

The EPIC/ELIC is part of the STUT 2000 PERCOFI Board and of the LineCard Module. Check the configuration of the external hardware; does the setting in the user area match with the hardware configuration?

Message: "Serial I/F Init failed at COM port"

ARCOS-SP PLUS was started with the option /V and has tried to detect one of the hardware platforms from **table 8** without success.

This message can have many reasons:

- none of the boards from **table 8** is connected to the COM port
- the wrong cable is used (see **table 8**)
- the wrong port number is given in the RS232.INI file
- the firmware for the external hardware was not loaded before
- the external hardware is not in program mode (but in loader mode instead)
- the external hardware has no power supply

Message: "Unable to write the ARCOFI"

The communication with the ARCOFI-SP is disturbed.

Has anything changed that concerns the interface mode, the chip address or the hardware configuration? Is any cable removed or loose? Does the software try to execute a file that was created by the ARCOS-SP PLUS program for the PSB 2165? A good idea is to quit the ARCOS-SP software and to start again with the initialization of the hardware.

Message: "Unable to read the ARCOFI"

The communication with the ARCOFI is disturbed (see above)

9.5.2 Other Problems

Message: "Opening Coefficient-file failed"

ARCOS-SP PLUS was not able to open the file ARC63.TAB. Make sure that this file is in the same directory as ARC63.EXE itself.

Message: "Syntax Error or command not allowed"

An input in the command line does not match the syntax given in **chapter 9.2.4**.

Message: "Interpreter Error! File loading stopped"

A file that should be executed contains an unknown command. Probably it is not a file that was created with ARCOS-SP PLUS for the PSB 2163.

Message: "ARCOS-SP program does not support this command"

You are using the ARCOS-SP software which is a demo-version that does not support hardware access in any way. Only the ARCOS-SP PLUS software is able to execute the desired command.

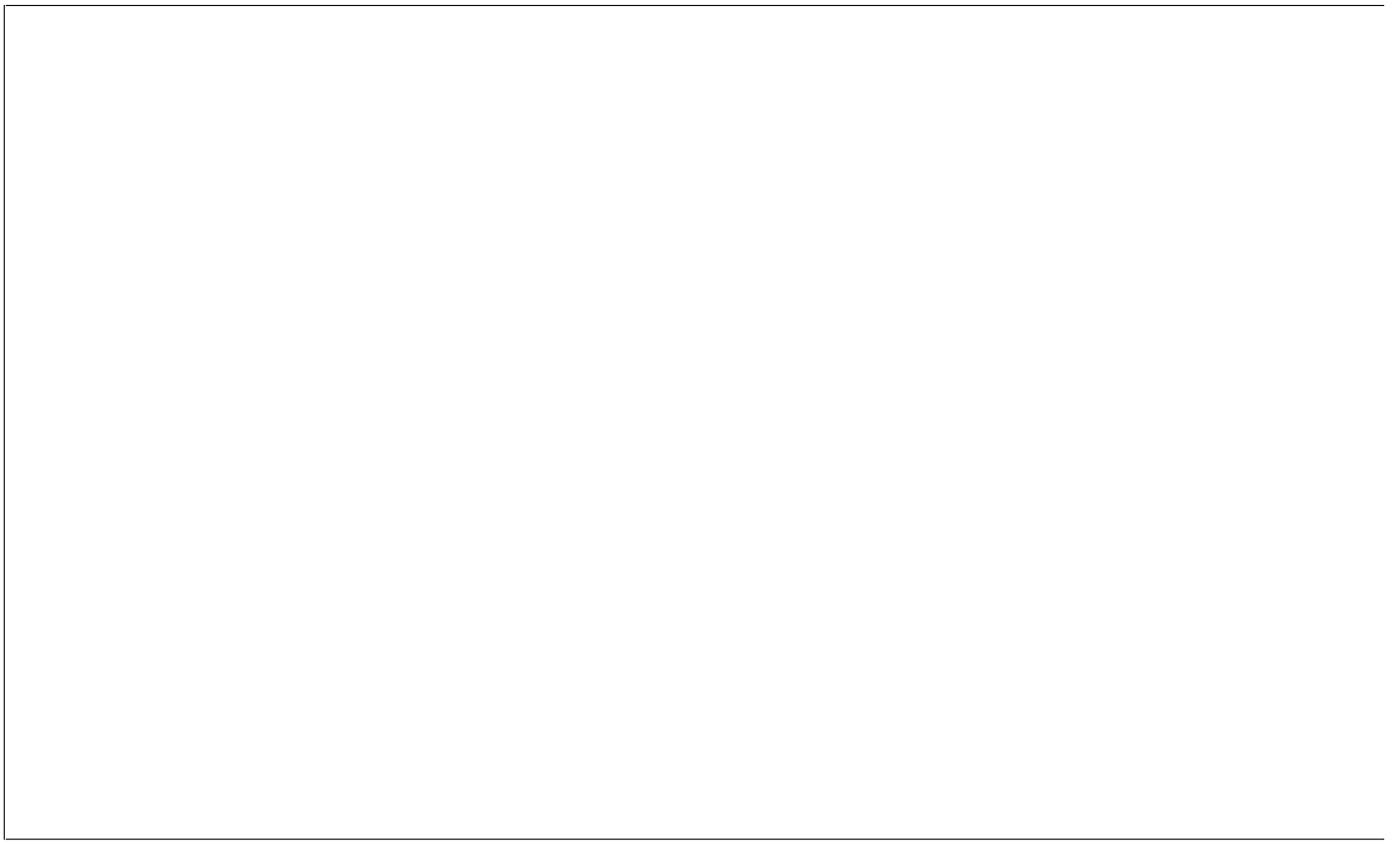
Message: "ARCOS-SP program does not support this window"

You are using the ARCOS-SP software which is a demo-version that does not support hardware access in any way.

Message: "Not enough memory" or "Unable to allocate enough memory…"

The ARCOS-SP PLUS software requires at least 500kB free conventional DOS memory. Remove any other memory resident programs that are not necessary for running a DOS application to get enough memory space.

SIEMENS



ICs for Communications

Analog Line Interface with the ARCOFI®-BA

PSB 2161

Application Note 06.96

PSB 2161 Revision History: Current Version: 1996-06-01		
Previous Version:		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

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10 Application Note – Analog Line Interface with the ARCOFI®-BA

10.1 Introduction

This application note gives a general introduction into analog line interface circuits that are intended to connect PCM-based digital equipment to an analog telephone line. It is assumed that galvanic isolation between the line and the digital equipment is necessary thus a transformer is used and not an integrated speech circuit. Furthermore the D/A and A/D converter is the ARCOFI-BA PSB 2161, a high quality PCM Codec. The ARCOFI-BA has some advantages that make it the perfect device for this kind of application:

- true differential analog in- and outputs
- analog output capable of driving a transformer directly
- gain adjustable in 0.1 dB steps
- DSP based frequency correction filters
- integrated tone generator e.g. for call progress tones or DTMF
- low power consumption, single 5 V supply
- flexible PCM interface, compatible to all time-slot oriented interfaces including IOM-2
- PCM signals can be A-law, µ-law, or 16-bit linear coded

Typical products incorporating this kind of line interface are any kind of PC-cards with an analog port, ISDN terminal adaptors, or small PBX systems with 1-3 analog lines.

The purpose of the present paper is to explain how to realize the 2/4-wire conversion between the telephone line and the ARCOFI-BA and how to achieve impedance matching at the analog 2-wire interface. Additionally, the following items are discussed:

- transhybrid balance
- DC characteristic
- ring detection

It should be noted that the circuits described in this application note are mainly designed for a terminal, not for a Linecard or PBX where the analog line has to be fed with DC and ring voltage. However, the principle of impedance matching and achieving good values for transhybrid balancing is the same for both kind of applications. Therefore it is not difficult to modify the circuits presented here for use on e.g. a Linecard. This topic is discussed more in detail in **chapter 10.5**.

10.2 Realization

10.2.1 General Architecture

The wires of the analog line are labeled “tip” and “ring” in **figure 62**. Between the Codec (PSB 2161 ARCOFI-BA) and the line a 2/4-wire conversion has to take place in order to separate the incoming and outgoing signals. The transformer itself only provides the galvanic isolation and separates the high- and low-level parts of the circuit.

To draw a DC current in the off-hook condition a special block (“DC”) is introduced. The small sized transformers proposed in this application note are not capable of drawing the DC current since this would cause saturation of the magnetic core. Therefore the transformer is AC coupled with the help of a single capacitor (“C” in **figure 62**). While on-hook the complete system is not connected to the analog line (not shown in **figure 62**).

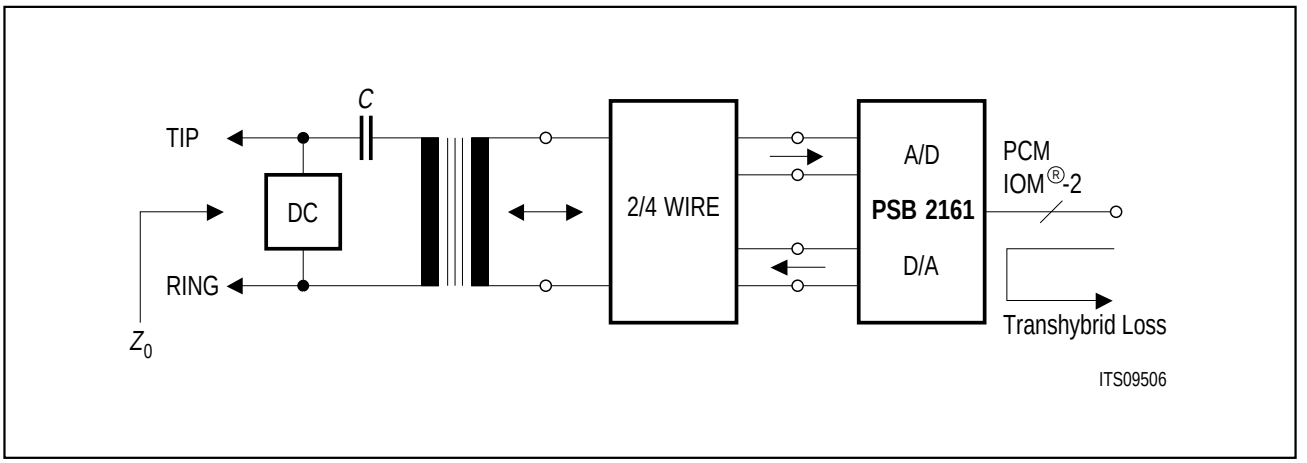


Figure 62
Overview of all Functional Blocks

Depending on the country the circuit is being designed for, different requirements exist for the impedance Z_0 that has to be offered to the line (compare with **table 11**). One main task is to achieve impedance matching at the tip/ring port. Impedance matching is expressed in terms of **return loss**. The return loss can be measured with a Wheatstone bridge where the unknown impedance is placed in one arm. The higher the value for the return loss, the better is the impedance matching. Values > 1 5 dB are typical.

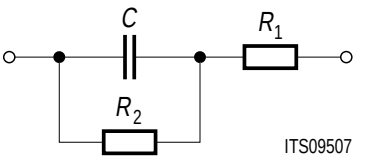


Figure 63

Table 11
Values for the Reference Impedance Z_0

Country	R_1	R_2	C
USA and many others	600 Ω	–	–
UK	370 Ω	620 Ω	310 nF
Germany	220 Ω	820 Ω	115 nF
China	200 Ω	680 Ω	100 nF

On the other hand, any digital signal applied to the PCM interface of the ARCOFI-BA will cause a certain echo coming back out of the digital Codec output. The level of the reflected signal related to the applied signal level is called **transhybrid loss** (compare with **figure 62**). High values for the transhybrid loss (e.g. > 20 dB) mean a good transhybrid balance for the circuit. The echo is caused by a non-perfect 2/4-wire conversion respectively impedance mismatching at the tip/ring port.

The transfer functions from the analog line to the PCM interface and from the PCM interface to the analog line are important characteristics for the design as well. These transfer functions have to meet the country specific requirements. The application circuits given in the app. note are flat over the whole voice band (300 Hz … 3400 Hz). With the help of the DSP based frequency correction filters FX and FR almost any response can be achieved (see the description of the ARCOS software).

Especially if data transmission at high baud rates (e.g. with V.34 modems) is desired, the harmonic distortion becomes important. The circuits in this application note allow a reliable transmission of modem signals with at least 28800 bit/s.

10.2.2 DC Characteristic

The DC characteristic of the line interface has to meet the requirements of the national PTT[1]. Today either integrated speech circuits or a separate DC current sink are responsible for adjusting the DC characteristic. Special requirements exist to ensure that the minimum line hold current can flow even under worst case conditions like long lines if the subscriber goes off-hook.

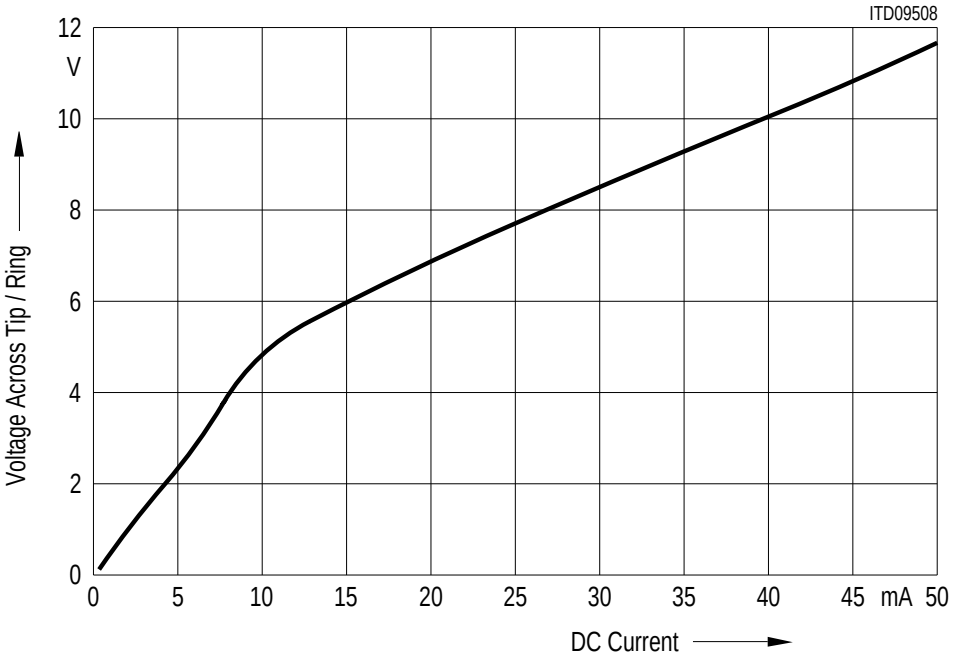


Figure 64
Measured DC Characteristic

The schematic on **page 190** shows a DC current sink with the transistors Q1, Q2. **Figure 64** contains the corresponding measuring results. Since C2 allows only a DC-voltage at the basis of Q2, the circuit presents a high impedance for AC signals. The DC characteristic meets the requirements of the German PTT; it might be necessary to adapt the values for R5/R6 and D8 for other countries.

[1] e.g. BS 6317:1992 in the UK; BAPT 223 ZV 5 in Germany

10.2.3 Impedance Matching

If the secondary winding of an ideal transformer is connected to a load Z, at the primary winding a impedance of w^2Z appears (w: turns ratio); compare with **figure 65**. If therefore the impedance Z_0 should be presented to the tip/ring line a 1:1 transformer has to be connected to the load Z_0.

If a differential analog output drives the transformer, a impedance Z_0 has to connected in series to one of the outputs. This is shown in **figure 66** with the difference that the transformer can be a non-ideal type and the series impedance Z_0^* is not exactly the same that is really presented to the tip/ring line. With a slightly different value for Z_0^* the non-ideal behavior of the transformer can be compensated to a certain extent.

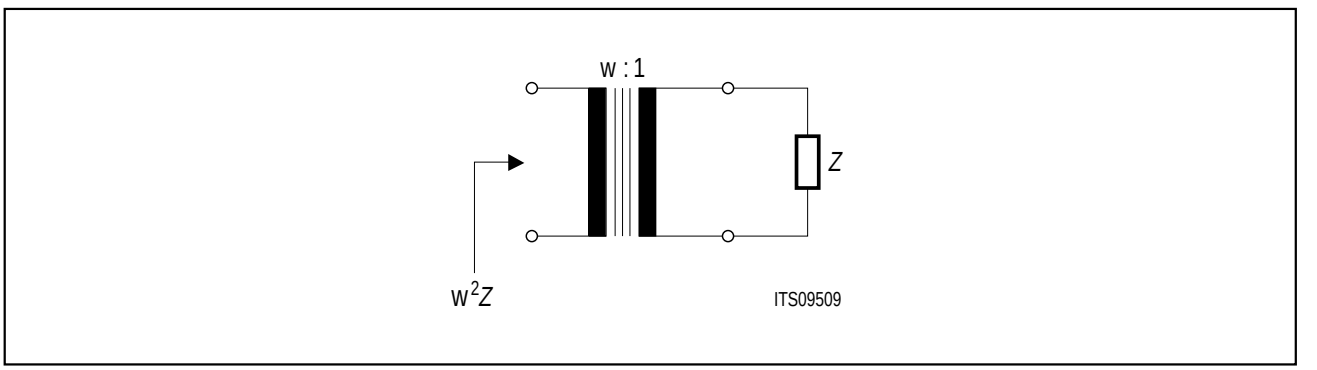


Figure 65
Ideal Transformer with Load Z

The easiest way to find the best suited value for Z_0^* for a certain transformer and a particular impedance Z_0 is to replace the PSB 2161 in **figure 66** with a short circuit and to alter Z_0^* until the best match is achieved. If a suitable model for the transformer is available, simulation results may lead to Z_0^* as well. The output impedance of the PSB 2161 is assumed to 2 Ω and therefore neglectable.

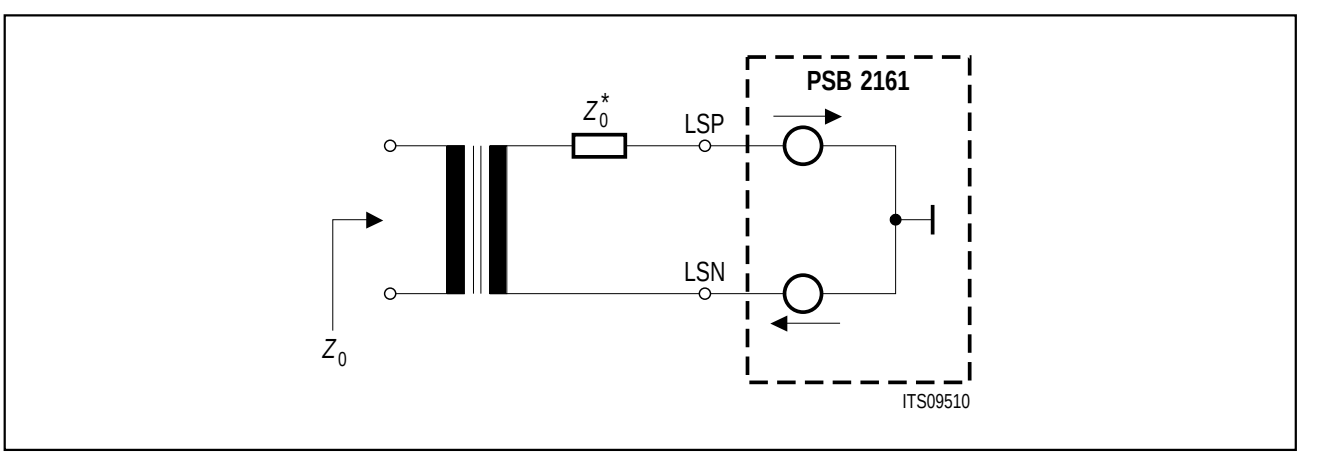


Figure 66
Principle of Impedance Matching (non-ideal transformer)

10.2.4 2-wire / 4-wire Conversion

In **figure 66** there is only a signal transmission from the Codec to the analog line possible. In addition any signal coming from the tip/ring line has to be presented to the analog Codec inputs. But signals leaving the analog Codec outputs (pins LSP, LSN in **figure 66**) are obviously not allowed to appear at the analog Codec inputs.

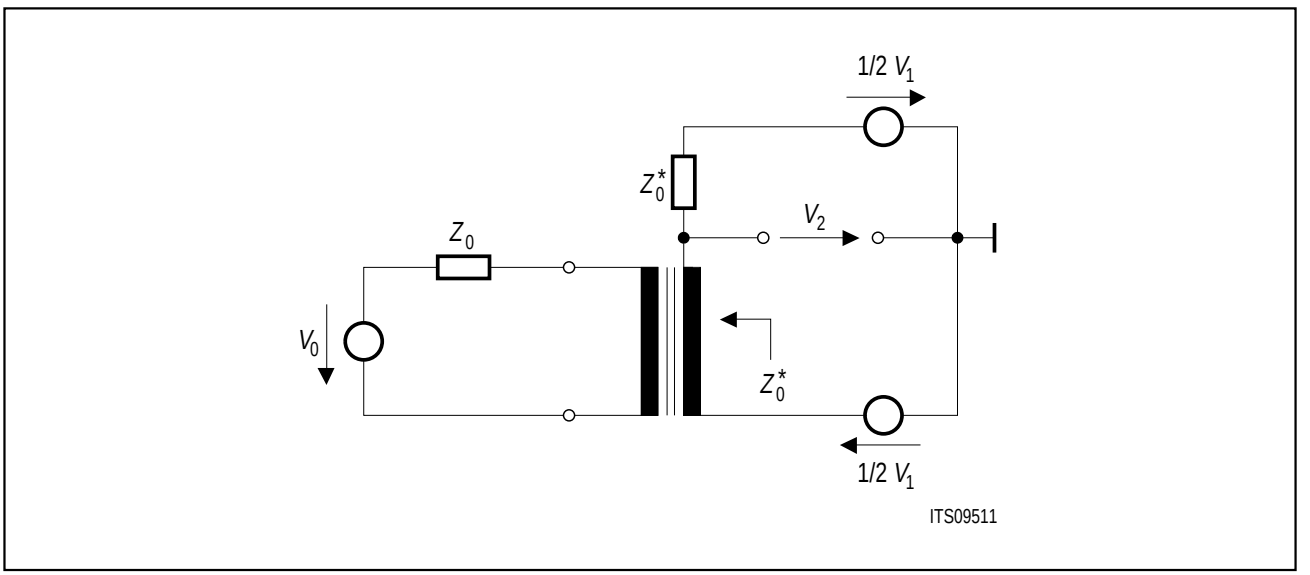


Figure 67
How to do the 2/4 Wire Conversion

Figure 67 explains how a simple bridge configuration performs the 2/4-conversion. V_1 is the voltage generated by the analog output amplifier of the PSB 2161. With Z_0^* impedance matching is achieved. If the tip/ring line is connected to the reference impedance Z_0 (at the central office) the two arms of the bridge (Z_0^* and the secondary winding of the transformer) are balanced, thus the voltage V_2 is always zero. In the other direction always $V_2 = 1/2V_0$. Therefore the incoming and outgoing signals from/to the analog line are separated and presented to the corresponding in- and output pins of the Codec.

The same circuit as in **figure 67** is shown in **figure 68** but now with the in- and output pins of the ARCOFI-BA PSB 2161. The differential microphone input MIN1/MIP1 is used in a single ended configuration (MIP connected to V_{REF}). Since the DC voltage at the outputs is the same as at the microphone input pins, no DC decoupling capacitor is required.

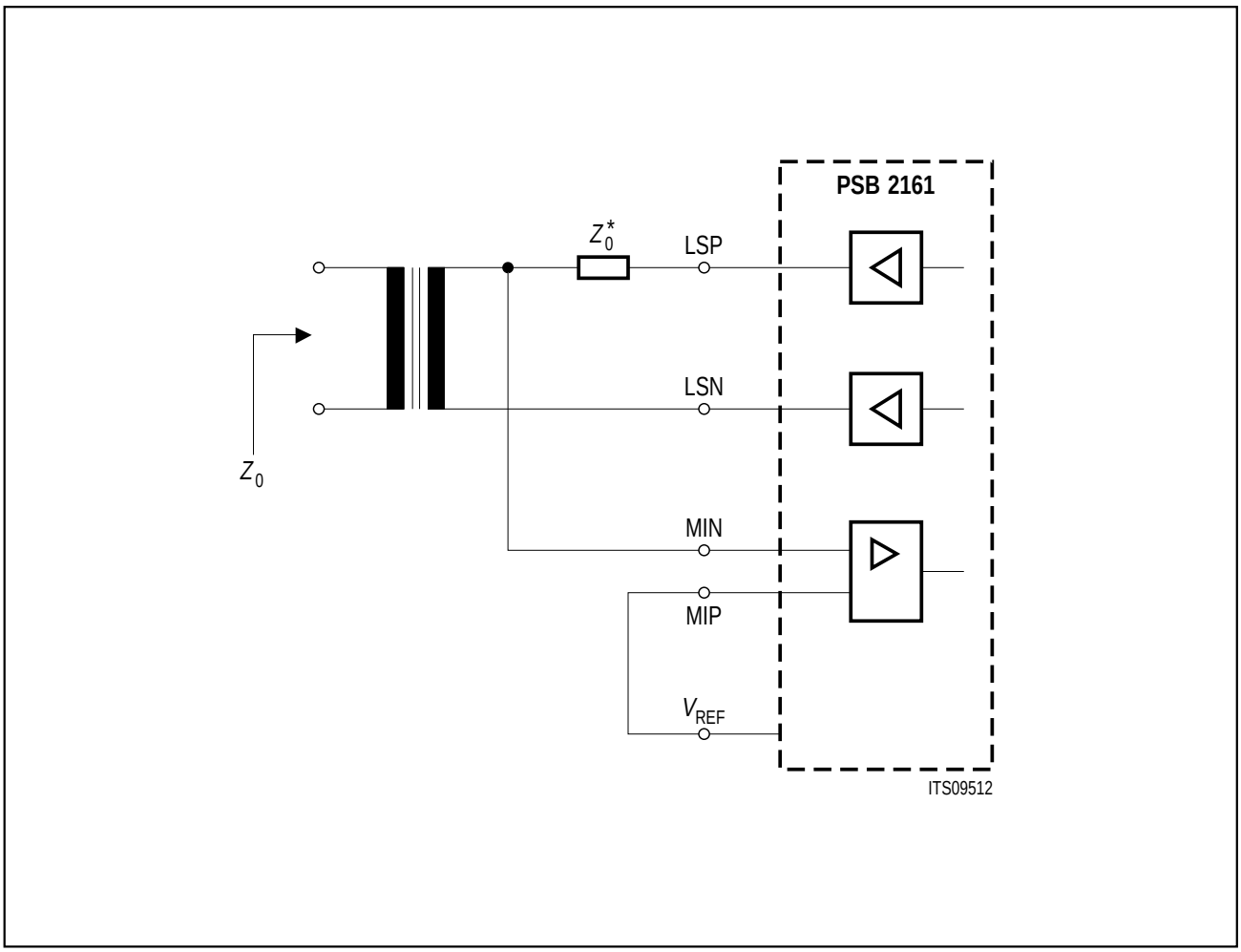


Figure 68
Realization of 2/4 Wire Conversion with PSB 2161

10.2.5 Transhybrid Balance

Provided that the impedance is perfectly matched and the bridge in **figure 67** is perfectly balanced, there is no signal path from the analog Codec outputs to the inputs. In a real application this will never be the case. One will always have to make a compromise in designing Z_0^* and tolerances as well as nonlinearity in the transformer lead to a limited balance of the bridge. However, with a little additional effort the transhybrid balance can be improved for a given impedance match. The principle is shown in **figure 69**. The voltage V_2 across R_2 serves as input voltage for the Codec. This voltage is not taken directly from point “A” as it would be the case with a configuration like in **figure 67**. Instead a certain portion of the signal available at point “B” is substracted before.

A simulation can reveal the improvement that this topology offers in terms of transhybrid loss. For a practical realization the value for R_1 is chosen in a way that $R_1 >> |Z_0|$; this ensures that R_1 does not affect impedance matching. R_2 should be small compared to the input impedance of the Codec. Then Z_1 is empirically chosen while observing the echo at the digital output of the ARCOFI-BA. Again, $|Z_1| >> |Z_0|$ for not to affect the result of the impedance matching.

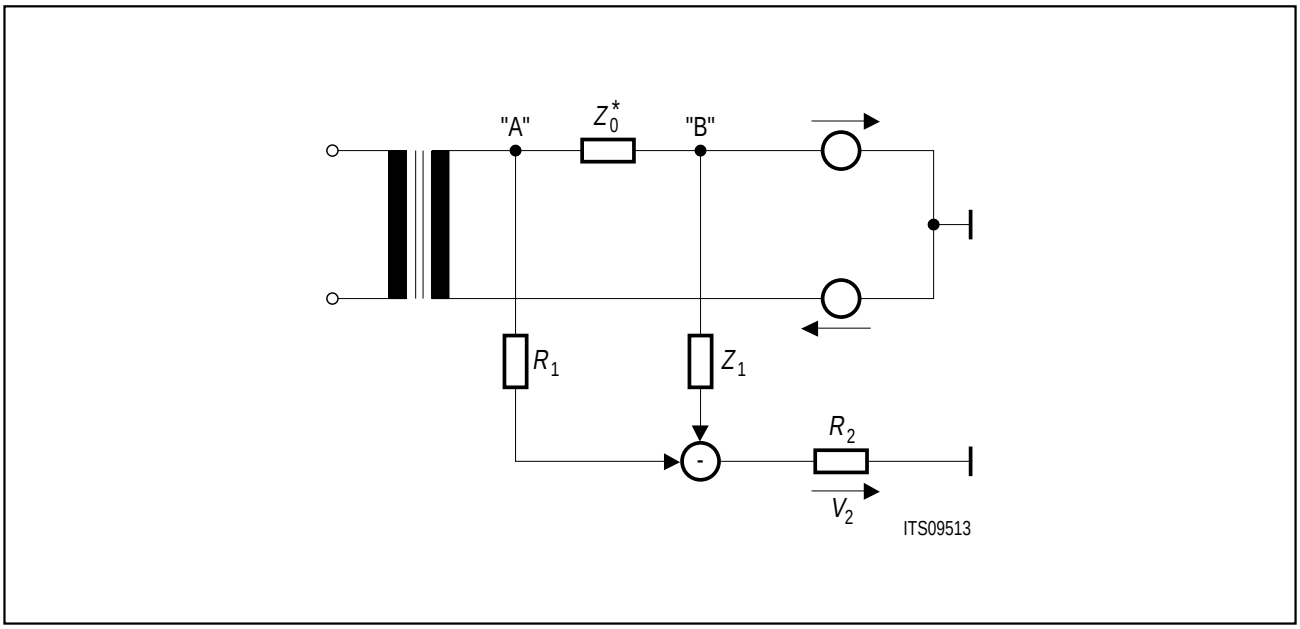


Figure 69
How to Improve Transhybrid Balancing

Due to the high performance differential microphone amplifier of the PSB 2161 the substraction shown in **figure 69** can be realized without an additional operational amplifier. Basically, R_1 is connected to the inverting and Z_1 to the noninverting input of the PSB 2161. This is shown in the complete schematic on page 190.

10.2.6 Hook-Switch and Pulse Dialling

In general, the hook switch is not included in the over-all circuit diagram. For this purpose normally a relays or a transistor is being used. **Figure 70** shows a common solution with a P-channel MOS transistor. The transistor is normally off and as soon as the optocoupler switches on, the MOS transistor exhibits a low impedance between Source and Drain, causing the terminal to draw line current. “DC” is the DC current sink and “RING DET.” stands for a ring detection circuit like presented in the next chapter.

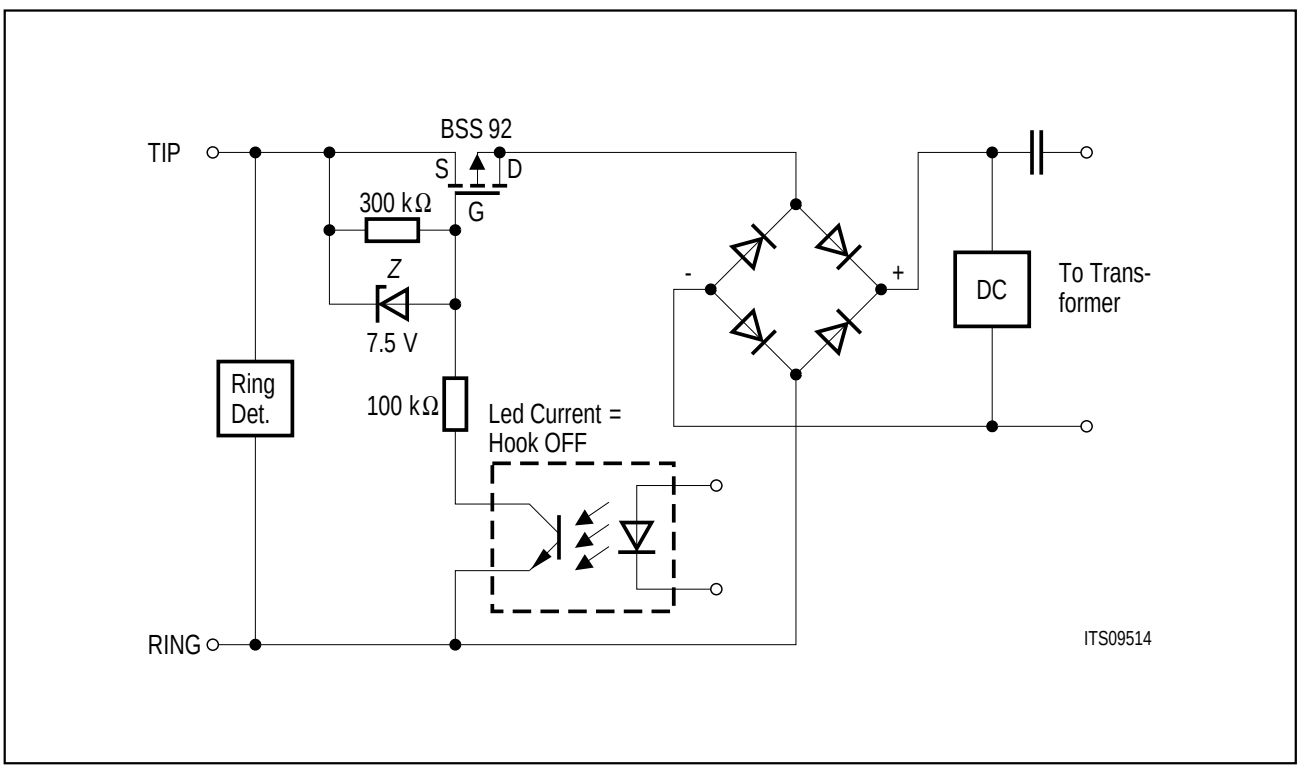


Figure 70
Implementing an Electronic Hook Switch

10.2.7 Ring Detection

In order to inform the system controller about an incoming call a simple ring detection circuit like shown in **figure 71** can be used.

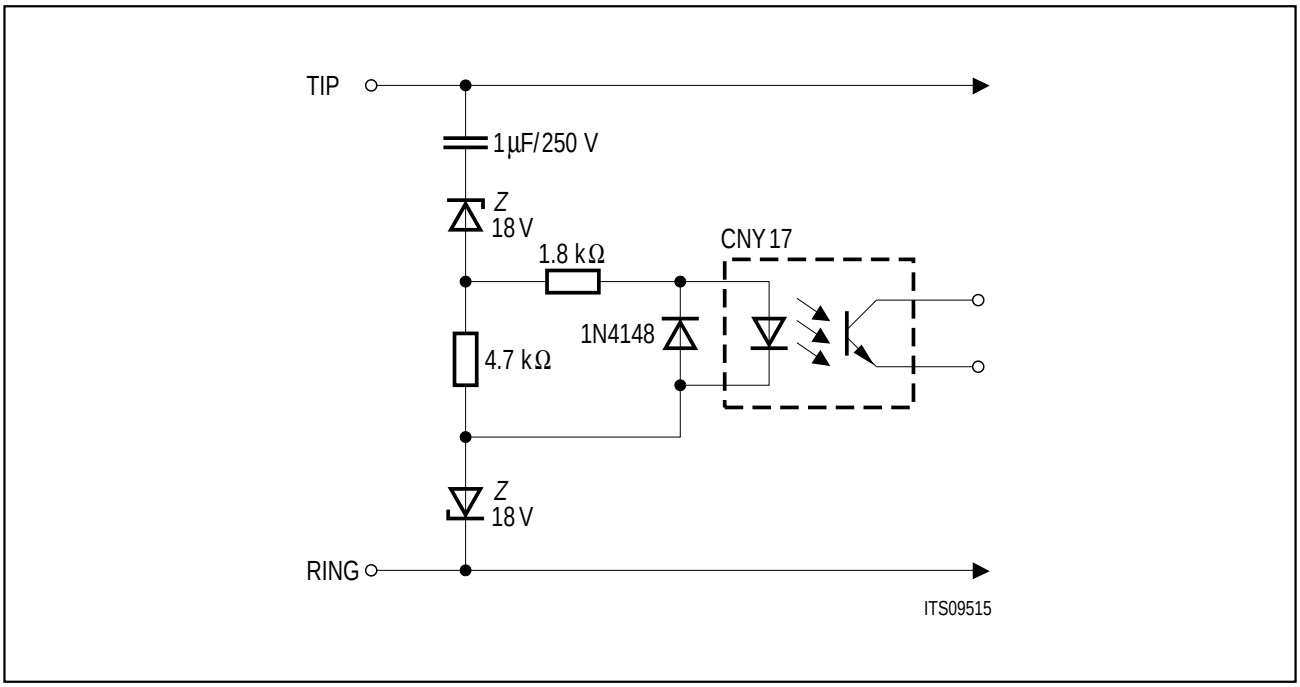


Figure 71
Example for Ring Detection

10.3 Circuit Diagram

10.3.1 Component Values

On page 190 and page 191 there are two circuit diagrams showing a complete application incorporating everything discussed in the preceding chapters except a hook switch. On the left hand of the schematics the connections to the tip and ring line are shown; on the right hand connections have to be made to the PSB 2161. The pins numbers and pin names are attached to the labels. MIN1/MIP1 is the differential input of the PSB 2161, LSP/LSN the differential output. V_{REF} is the reference voltage pin (2.4 V_{DC}).

The diagram on page 190 differs from the one on page 191 by the use of an additional metering filter to suppress 16 kHz teletax pulses. This filter is useful in countries like Germany that utilize 16 kHz pulses.

Several elements in the circuit diagrams are labeled with Z_1 ... Z_5 only. They have the values given in **table 12, 13, and 14** and take the different impedances for different countries into account. A “+” sign means a series connections of two elements whereas a “||” sign stands for paralleling two components. For all country specific tables the gain setting for the PSB 2161 is given.

Table 12
Component Values for Circuit Diagram on page 190

(Germany) Z_0 = 220 Ω + 820 Ω||115 nF; Transformer 9003, 9004				
C3	**Z1**	**Z2**	**Z3**	**Z4**
1 µF||820 nF	160 Ω	1 kΩ||120 nF	47 kΩ + 22 nF	20 kΩ

AMI	**GX**	**ALS**	**GR**
+ 18 dB	+ 2.0 dB	+ 5.5 dB	– 2.0 dB

The values for Z_1 ... Z_5 have been designed for two common transformers from *Critchley Components* (refer to page 195 for address), type 9003 and 9004. The electrical characteristics of the transformers are similar thus in most cases they can both be used without modifying the external component values (see tables). In terms of distortion both transformers offer a performance that is sufficient for high speed modems signals.

Additional components guarantee a certain robustness of the circuit; C4 ... C7 as well as D3 and D6 provide overvoltage protection and suppression of radio frequency signals.

Table 13
Component Values for Circuit Diagram on page 191 and 600 Ω Impedance

(USA and others) Z_0 = 600 Ω; Transformer 9003					
C3	**Z1**	**Z2**	**Z3**	**Z4**	**Z5**
2.2 µF	560 Ω	0 Ω	330 kΩ	30 kΩ	470 Ω+ 10 nF

AMI	**GX**	**ALS**	**GR**
+ 24 dB	+ 0.8 dB	+ 2.5 dB	+ 0.75 dB

(USA and others) Z_0 = 600 Ω; Transformer 9004					
C3	**Z1**	**Z2**	**Z3**	**Z4**	**Z5**
2.2 µF	560 Ω	68 Ω || 330 nF	N.C.	30 kΩ	N.C.

AMI	**GX**	**ALS**	**GR**
+ 24 dB	+ 0.8 dB	+ 2.5 dB	+ 0.75 dB

Table 14
Component Values for Circuit Diagram on page 191 and a Complex Impedance

(UK) Z_0 = 370 Ω + (620 Ω||310 nF); Transformer 9004, 9003					
C3	**Z1**	**Z2**	**Z3**	**Z4**	**Z5**
2.2 µF	300 Ω	680 Ω||150 nF	100 kΩ + 10 nF	30 kΩ	N.C.

AMI	**GX**	**ALS**	**GR**
+ 24 dB	+ 0.5 dB	+ 5.5 dB	– 2.0 dB

(China) Z_0 = 200 Ω + (680 Ω||100 nF); Transformer 9004, 9003					
C3	**Z1**	**Z2**	**Z3**	**Z4**	**Z5**
1 µF	75 Ω	680 Ω||100 nF	56 kΩ + 10 nF	30 kΩ	N.C.

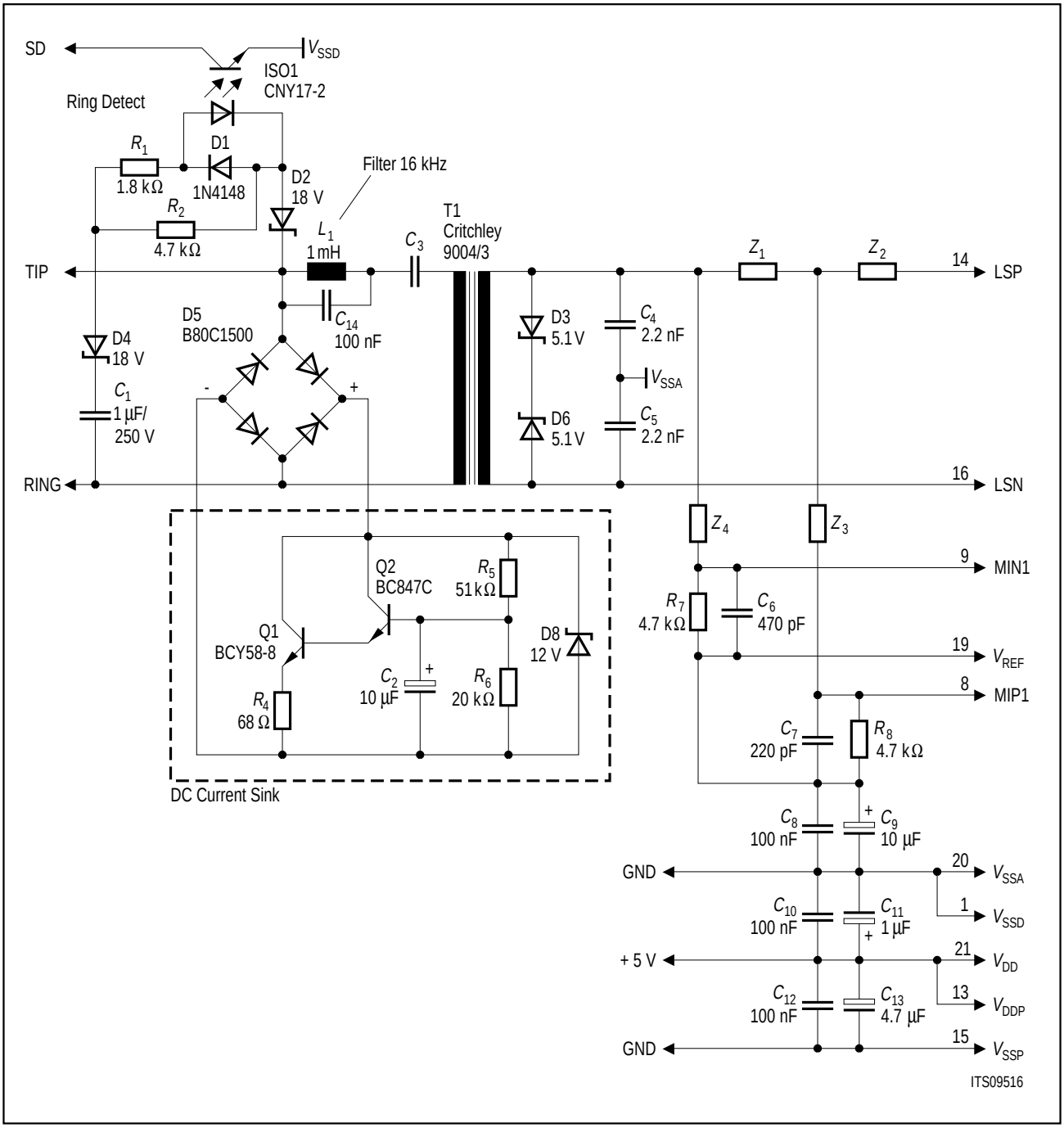
AMI	**GX**	**ALS**	**GR**
+ 24 dB	+ 1.0 dB	– 0.5 dB	0.0 dB

In both schematics a DC current sink around Q1 and Q2 is shown (see also **chapter 10.2.2**). With D2, D4 and the optocoupler a simple ring detection with galvanic isolation is realized. The connection labelled SD indicates an incoming call.

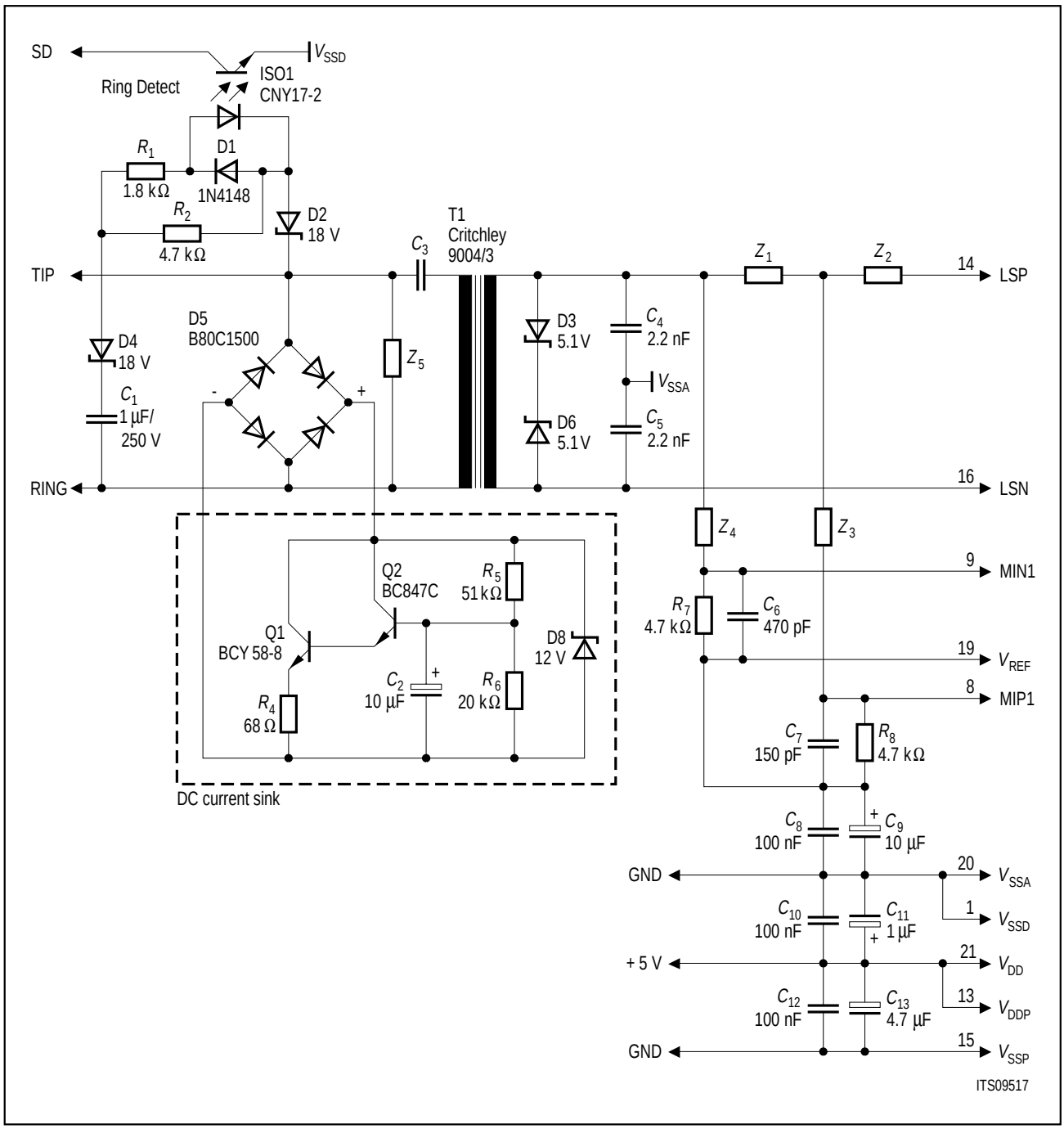
It should be noted that the current sink is polarity dependent; therefore the rectifier bridge D5 is inserted into the signal path. The AC transmission characteristic is not influenced as long as a DC current flows through the current sink that forward biases two of the diodes.

The transmit and receive gains are adjusted with the analog amplifiers AMI (microphone amplifier) and ALS (loudspeaker amplifier) and with the digital gain stages GR and GX. The values are chosen in a way that 0 dBm @ Z_0 lead to a digital level of 0 dBm0 at the PCM interface of the PSB 2161. The digital frequency correction filters FX and FR that the PSB 2161 offers are not utilized but can additionally be used to achieve the desired frequency response; without the filters the response is flat within a +/-1.5 dB band across 300 … 3400 Hz.

10.3.2 Circuit Diagram 1



10.3.3 Circuit Diagram 2



10.4 Measurement Results

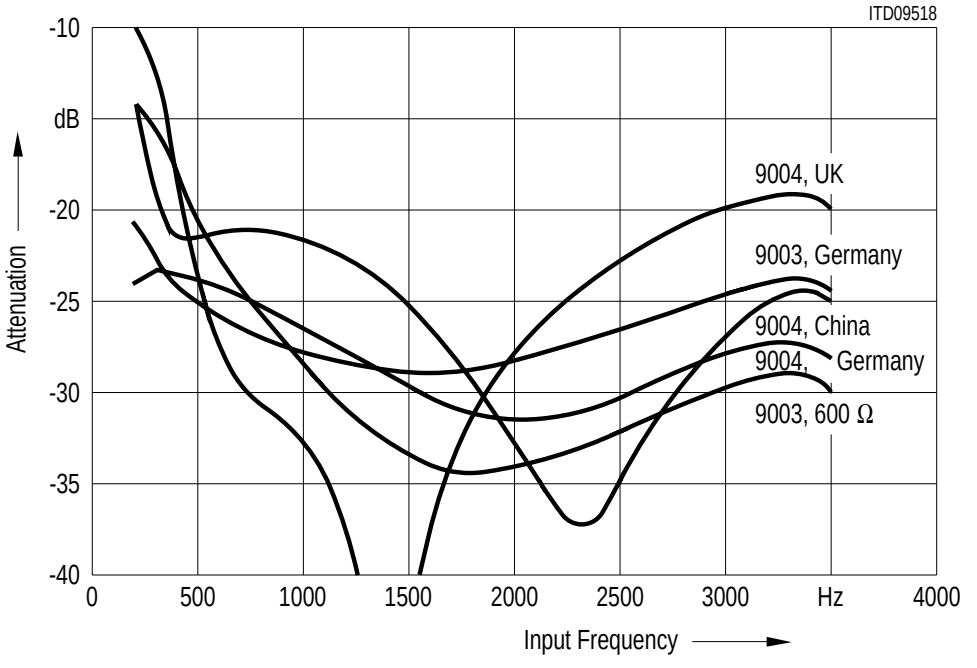


Figure 72
Measured Values for the Transhybrid Loss

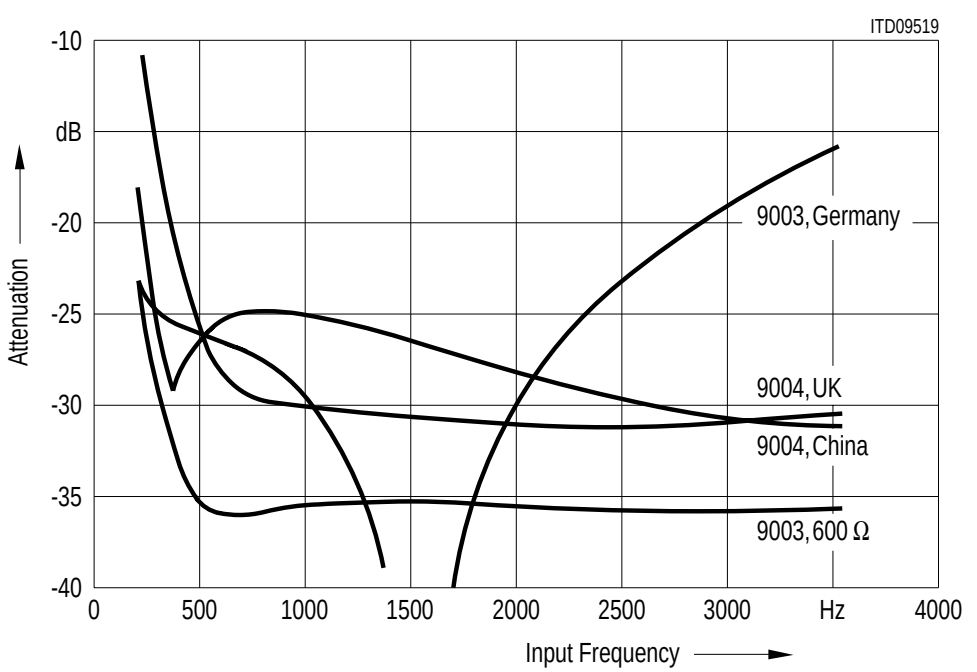


Figure 73
Measured Values for the Return Loss

10.5 Line Interface for use on a Linecard

The situation on a linecard or a small PBX does not basically differ from a terminal line interface. At both sides of the analog line (at the terminal and at the linecard) the 2/4-wire conversion has to take place and impedance matching as well as transhybrid loss are key parameters. The remaining differences are listed in **table 15**.

Table 15
Main Differences between a Line Interface for a Subscriber and on a Linecard

	Subscriber / Terminal	Central Office / PBX / Linecard
DC	While off-hook, current must be drawn (line hold current)	DC feeding; detection of current flow (if subscriber goes off-hook)
Ring	Detection of ring voltage	Ring voltage must be applied
Dialling	DTMF generation	DTMF detection

The DC feeding on a Linecard normally causes more trouble than the current sink inside a terminal. As long as DC feeding is not allowed to have an impact on the impedance matching, the feeding mechanism has to be designed carefully. The transformers that are normally used are not capable of taking any DC current so an arrangement like in **figure 74** with transformer and a high impedance DC source in parallel is the solution.

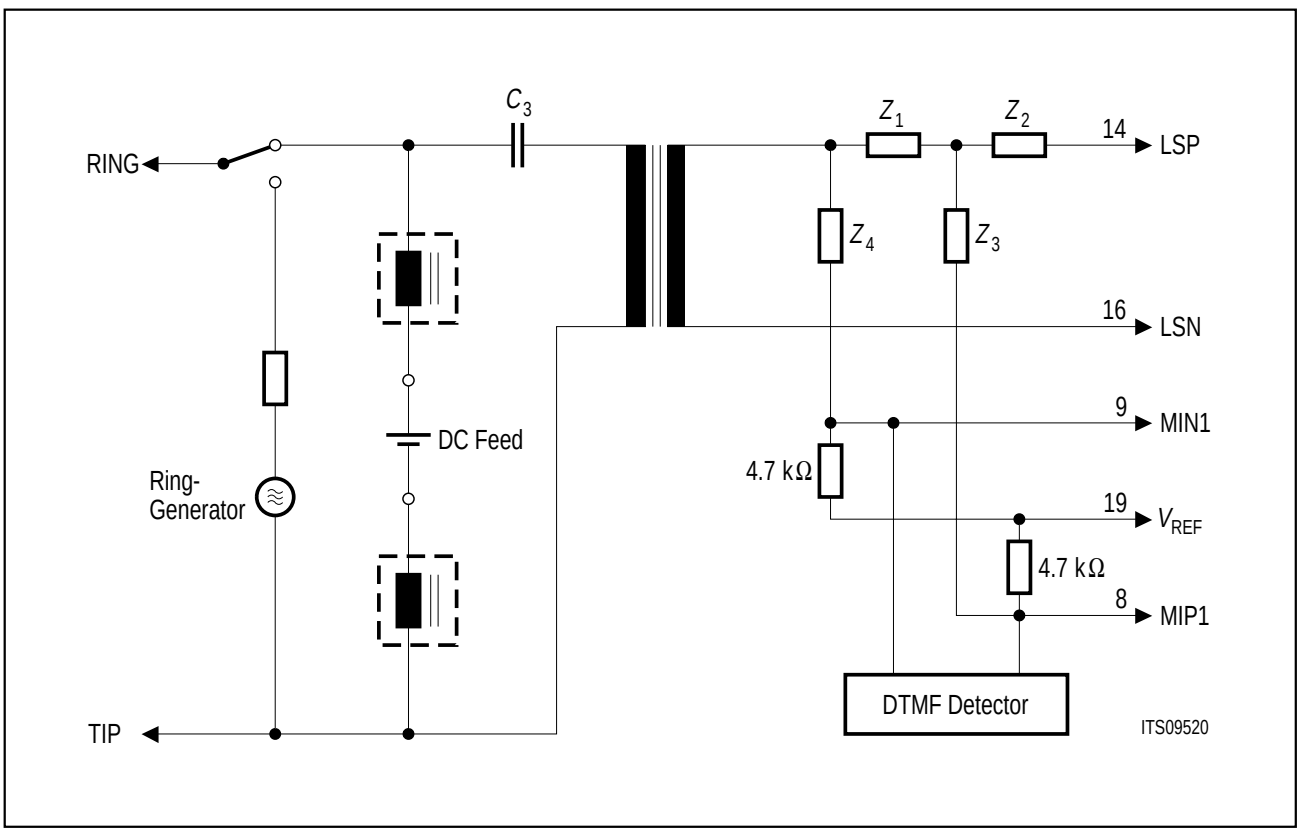


Figure 74
Basic Solution for Feeding the Tip/Ring Line

A bipolar transistor utilized as constant current sink (see e.g. schematic on page 190) shows a high impedance across emitter and collector as long as the maximum current flows ($U_{CE} > U_{CEsat}$). This impedance is about several kΩ. But on a Linecard the current sink is not always operating under this constant current condition and therefore the impedance might go down to several 100 Ω thus the DC feeding strongly affects the impedance matching. A solution for this problem is to

- use a “wet” transformer (capable of handling DC currents)
- take the influence of the DC feeding into consideration when designing the component values for impedance matching (matching is not always possible)
- use a more sophisticated DC current source, e.g. a circuit that always ensures $U_{CE} > U_{CEsat}$ for the main transistor.

Due to these effects in **figure 74** the current sink/source is only shown with an inductor symbol and a dashed box around it.

The generation of the ring voltage is independent of all the discussed matching issues and can for example be done with a simple secondary winding of the mains transformer. Of course this solution is applicable for a small PBX only.

DTMF detection cannot be handled by the PSB 2161 so normally a separate, analog DTMF detector is placed in parallel to the PSB 2161 inputs like shown in **figure 74**. This detector must have a high impedance input (> 50 kΩ) for not do disturb the balancing network.

10.6 Appendix

Transformer Manufacturer

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Hong Kong:	Excelpoint Systems Ltd., Phone +852 2503 2212
Taiwan:	Acer Sertek Inc., Phone +886 (0) 2 500 6363
USA / Alabama:	EI Tech Inc., Phone +1 205 464 0599
USA / Atlanta:	EI Tech Inc., Phone +1 770 564 1236
USA / Kentucky:	EI Tech Inc., Phone +1 606 331 3495

Important Standards

The following Standards are only a selection; they contain information about the required impedance Z_0, the transmission performance and the DC characteristic.

UK	BS6305; BS6317:1992
Germany	BAPT 223 ZV 5; BAPT 223 ZV 24
France	B11-11
Europe (in general)	Draft prETS 300 001 (Candidate NET4)

SIEMENS

ICs for Communications

Audio Ringing Codec Filter
ARCOFI®-BA

PSB 2161

Analog Line Interface: Using the ARCOFI®-BA with a SLIC

Application Note 03.96

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11 Application Note – Using the ARCOFI®-BA with a SLIC

11.1 Introduction

The ARCOFI-BA PSB 2161 is a high performance codec filter device with a state of the art tone generator and a universal analog front end.

This application note describes how to use the PSB 2161 to interface analog terminals like telephones, fax machines, or modems to the digital ISDN world. To be more specific, a terminal adapter with an analog tip/ring interface and an IOM-2/PCM interface is presented. The adapter makes use of the high-performance Codec ARCOFI-BA PSB 2161 from Siemens and the subscriber line interface controller (“SLIC”) HC5502B from Harris Semiconductor. Topics covered by this application note are

- complex impedance matching for tip/ring that fulfils the high German PTT standards
- resistive impedance matching
- using the IOM-2 bus for programming and transferring status information between a system microcontroller and ARCOFI-BA / SLIC
- using only two supply voltages for the whole system (– 48 V_{DC} for feeding the tip/ring line and + 5 V_{DC} for ARCOFI-BA and SLIC)

However, some issues are left open since they strongly depend on the particular application. For example the generation of the ring signal and the DTMF detection can differ significantly and are not covered here.

In addition to this application note, the following documents/software are recommended:

- [1] “PSB 2161 ARCOFI-BA User’s Manual”, Siemens AG
  (not available yet, use “PSB 2163 ARCOFI-SP User’s Manual” instead)
- “ARCOS-SP PLUS” ARCOFI coefficient software or “ARCOS-SP” (demo version)
- [2] “HC-5502B SLIC Data Sheet”, Harris Semiconductor, 3.93
- [3] “The HC-550X Telephone Subscriber Line Interface Circuits (SLIC)”,
  Harris Application Note No. 549

The programming bytes for the CRAM coefficients of the ARCOFI-BA are delivered by the ARCOS-SP PLUS software SIPO 2163. This can be helpful if the tone generator of the PSB 2161 is used or filter coefficients for the frequency correction filters FX/FR are needed. A demo version of this software is available as well (ARCOS-SP).

Although the PSB 2161 ARCOFI-BA is the typical device for this kind of application, the PSB 2163 ARCOFI-SP can be used as well, since both ICs differ only in the speakerphone support (which is not available for the PSB 2161).

11.2 The Harris SLIC HC5502B

The HC5502B from Harris Semiconductor was chosen for this application since it can handle a variety of battery voltages and requires only a + 5 V_{DC} supply (+ 12 V_{DC} possible as well). The other features include

- battery feeding with loop current limiting
- overvoltage protection
- ring relay driver
- supervisory functions (off-hook detection, ground key detection)
- hybrid functions

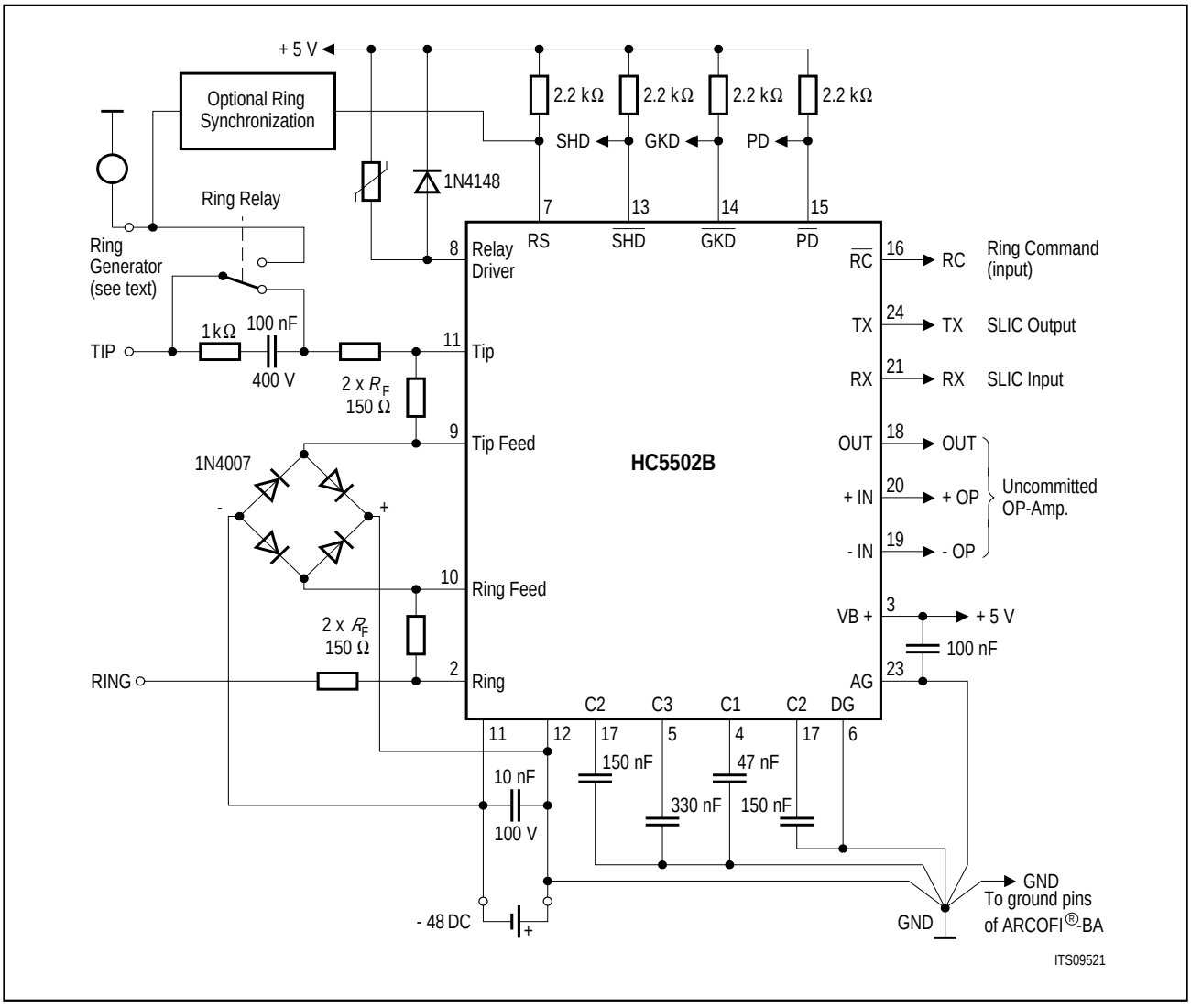

Figure 75
Circuitry for the HC5502B

The SLIC provides the interface between the 4-wire ground referenced terminal adapter environment and the 2-wire high voltage loop environment. Internally, signals in both directions are amplified by 6 dB but the feed resistors RF (150 Ω + 150 Ω) attenuate the corresponding signals by 6 dB again.

Figure 75 shows the HC5502B with all external components like they are required for a basic terminal adapter application. TIP and RING state the interface to any analog terminal equipment while the pins 21 and 24 are the analog in-/outputs to the ARCOFI-BA. Note, that the pin numbers are related to the DIP-24 package.

Additional circuitry for primary protection at tip/ring might be needed and is not included in **figure 75**.

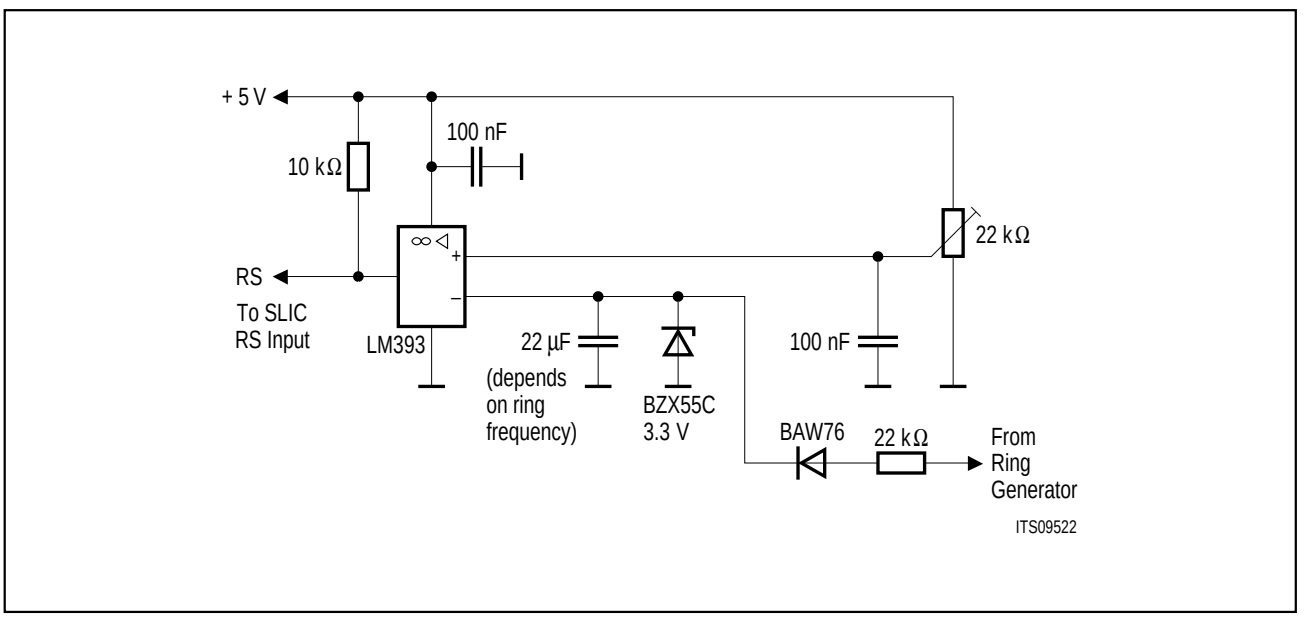

Figure 76
Optional Ring Synchronization

Ringing

Single ended ground referenced ringing is used with the HC5502B. An AC signal (20 Hz … 50 Hz, less than 150 V_{PEAK}) is generated by the ring generator. The ring generator can be anything from a power amplifier driven by a sinewave generator (which can be the tone generator of the ARCOFI-BA) or simply a secondary winding on the mains transformer. To synchronize the switching of the ring relay with the zero crossing of the ring signal, an optional ring synchronization circuit can be provided. An example for such a circuit shows **figure 76**. If the user hooks up the analog telephone during ringing, the flow of loop current is detected by the SLIC and indicated at the SHD output.

Logic Signals to/from the SLIC

The signals SHD and GKD are logic outputs indicating the flow of loop current (user has hooked up) or a short circuit to ground (user has pressed a ground key). Usually SHD (“Switch Hook Detection”) and perhaps GKD (“Ground Key Detection”) are transferred to the system microcontroller. This can be done either by connecting these pins directly to µC I/O-ports or by connecting them to the PCI-interface pins of the ARCOFI-BA (pins SA, SB, SC, SD). The logic level at the PCI-interface pins is mirrored in the C/I1 channel of the IOM2 bus. The C/I1 channel can be accessed by a microcontroller via any of the typical transceiver devices from Siemens Semiconductor (ISAC-S, ISAC-P, ICC).

The signals PD (power denial) and RC (ring command) state logic inputs to the SLIC. At least the RC signal must be provided either by the system µC or from a separate circuitry in order to activate the ring relays. If the system µC provides the ring command, again the PCI interface of the PSB 2161 can be used because the four pins SA, SB, SC, SD can be independently configured as in- or outputs.

About the C/I1 channel one should note that in certain applications the C/I1 channel is already occupied and cannot be used. On the other hand, if the serial control interface of the ARCOFI-BA is used instead of the IOM2, no C/I channel exists at all.

11.3 Resistive Impedance Matching

To achieve purely resistive impedance matching at the tip/ring port, a simple circuitry as shown in **figure 77** has to be connected to the TX and TR pins of the SLIC. As signal input at the PSB 2161 the single ended input MI3 is being used. One output pin of the differential loudspeaker driver (LSP) is coupled directly to the SLIC input. The digital interface to the IOM-2 or PCM bus consists of the four pins DU, DD, FSC, and DCL. Here the A-law or µ-law coded PCM signals are transferred to further signal processing or transceiver devices. A data format of 16bit is possible as well.

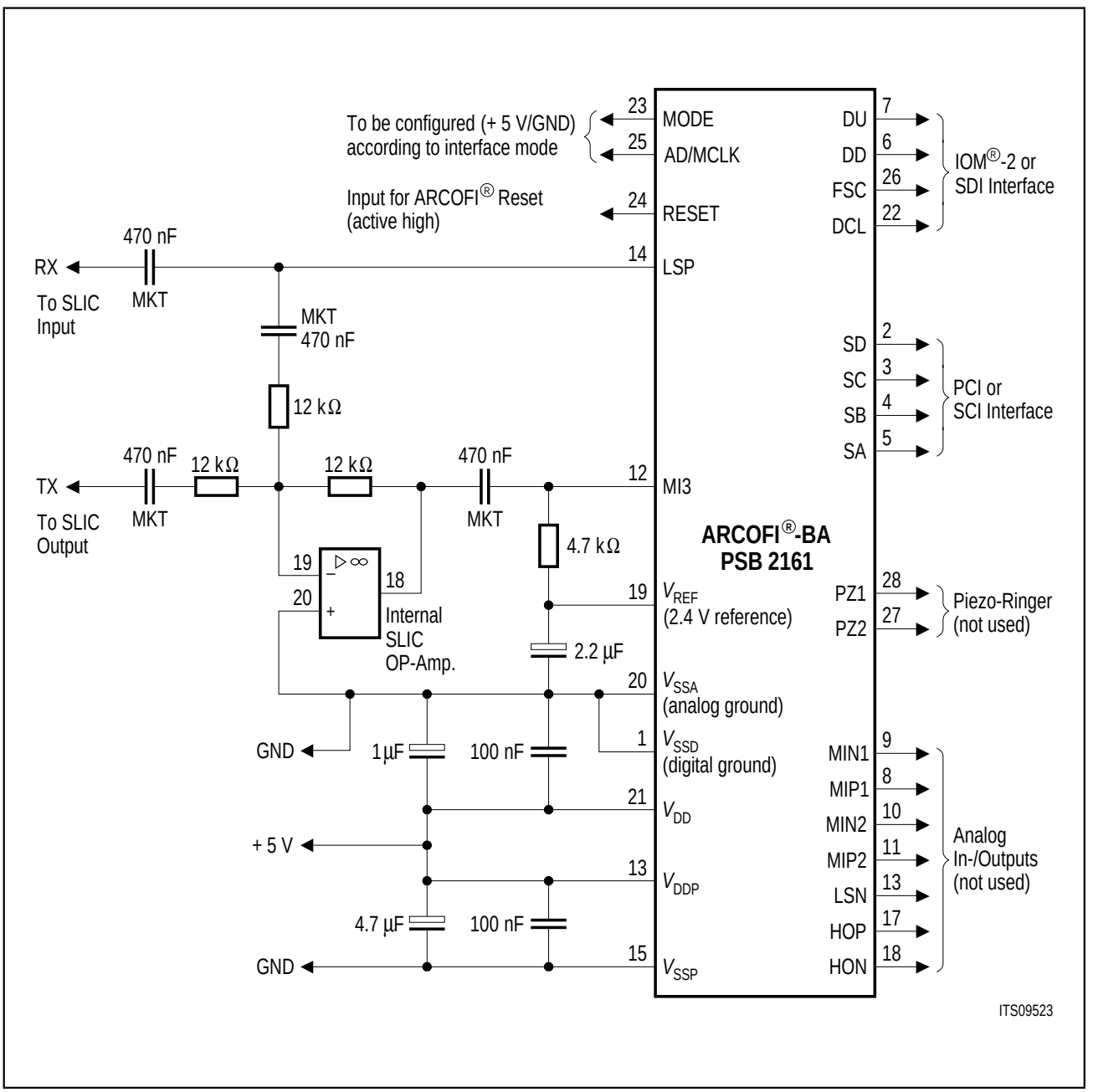

Figure 77
Implementation of Resistive Impedance Matching (600 Ω) with PSB 2161

11.4 Complex Impedance Matching

A typical example for a complex impedance is the 220 Ω in series with (820 Ω || 115 nF) for the German Telecom. To achieve a complex impedance at the tip/ring port the Harris application note explains different approaches [2]. One basic configuration taken from [2] is shown in **figure 78**. It offers the advantage of independent adjustment of impedance and transhybrid balance matching. A disadvantage is the need for three operational amplifiers. A practical realization with the PSB 2161 makes the summing amplifier OP3 obsolete, since the differential inputs of the PSB 2161 can be used for summing as well.

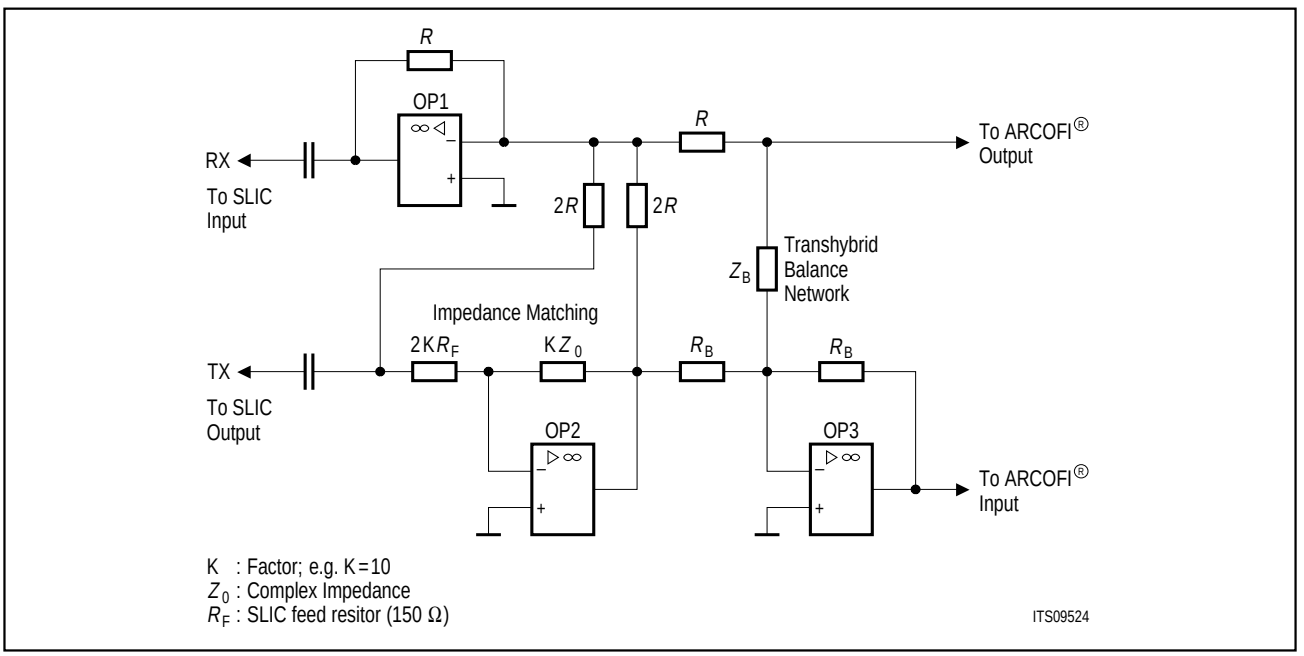

Figure 78
Principle of Complex Impedance Matching (taken from Harris App. Note 549)

The schematic in **figure 79** shows an implementation of the circuit from **figure 78** and is already optimized in terms of device count; the matched impedance is 220 Ω in series with (820 Ω || 115 nF). The circuit is able to fulfill the level requirements of the German Telecom with only a single + 5 V supply. That means, with a digital signal level of 0 dBm0 an analog level of – 7 dBm at tip/ring is generated. In the other direction, 0 dBm at tip/ring cause a PCM codeword that equals 0 dBm0.

With a 5 V supply the limiting factor for the voltage swing is first of all the external operational amplifier. If more headroom is required, the external operational amplifier has to be supplied with + 12/- 12 V. Then the SLIC can be fed by + 12 V as well.

The resistors must have 1% tolerance (or better). At least 5% capacitors are required for the 220n/330n/1000n types. The 4.7 nF capacitor should be even better, depending on the performance requirements. If the input impedance needs to be fine tuned, this can be done with the 3.9 kΩ and 27 kΩ resistor of the impedance matching network. The transhybrid balance depends solely on ZB (20 kΩ).

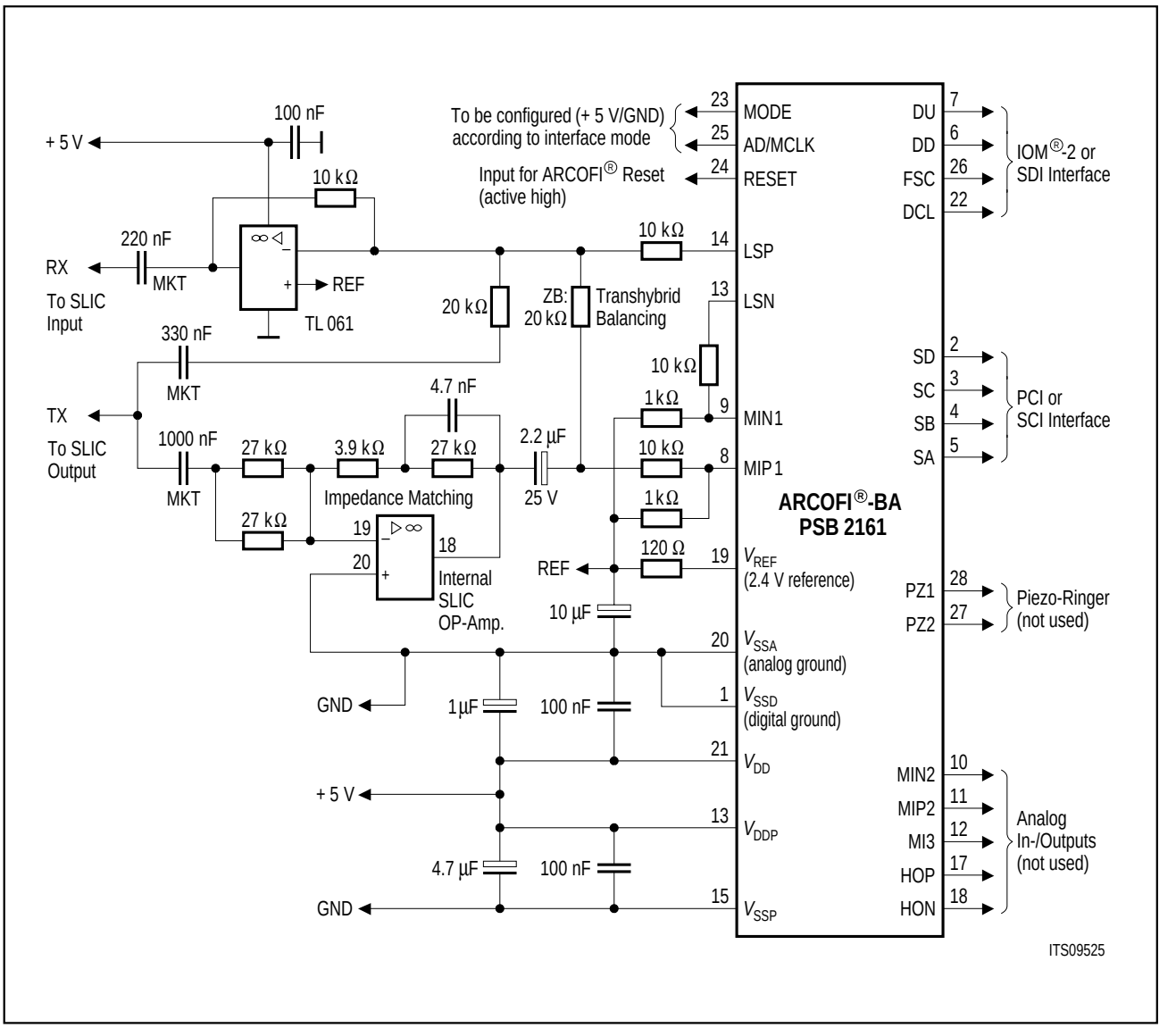

Figure 79
Implementation of Complex Impedance Matching with the PSB 2161

Programming

The initialization of the PSB 2161 is simple task since only one SOP_F sequence is sufficient for setting up all gains and interface modes. For a fine tuning of the level response the digital gain stages GX and GR can be used; coefficients for the gain stages can be obtained from the User's Manual[1)] or the ARCOS-SP software is used. The programming sequence for the circuit in **figure 79** is (refer to User's Manual):

COP_5 B3 51 91 AC (GX = – 0.8 dB; GR = – 2.1 dB)
SOP_F 00 05 50 00 00 C0 F1 16 (see table below)

Table 16
Register Setting

Register	Name	Value	Comment
GCR	General configuration	16_H	PCM channel for IOM2 applications and coding law; here: B1 and A-law; device is power up
DFICR	Data format and interface	$F1_H$	16 bit linear PCM words could be chosen here; configuration of pins SA, SB, SC, SD as in- or outputs depending on connection SLIC-ARCOFI
PFCR	Programmable filter	$C0_H$	GX and GR gain stages for level fine-tuning activated; FX/FR filters are not enabled
TGCR	Tone generator configuration	00_H	Not used
TGSR	Tone generator switch	00_H	Generator off; signalling tones could be switched to the tip/ring interface if the TRR bit is set
ATCR	AFE transmit configuration	50_H	Microphone input MIN1/MIP1 selected; amplification + 24 dB (needed due to 20 dB loss from 10 kΩ / 1 kΩ resistive divider); for the circuit in **figure 77** input MI3 and 0 dB gain would be needed
ARCR	AFE receive configuration	05_H	Loudspeaker amplifier with – 0.5 dB gain activated; earpiece amplifier is power down
TFCR	Test function	00_H	Not used

1 for the PSB 2163 **Chapter 2.2.3** in the User's Manual 6.95 applies

11.5 Measurement Results

The following measurement results were made with the circuit from **figure 75** and **figure 79** using the programming from the previous page. The measurement instrument is a PCM4 measuring device from Wandel&Goltermann which is connected to the PSB 2161 with the help of an STUT 2000 PERCOFI board (Siemens Evaluation Tool).

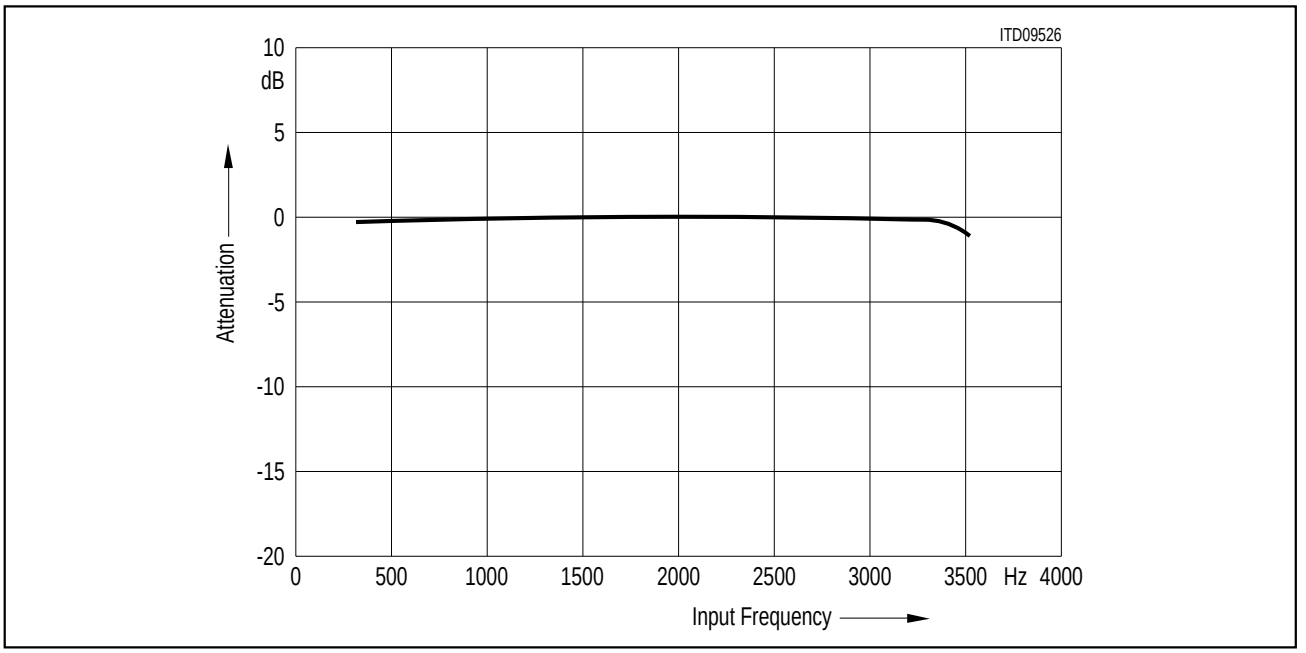

Figure 80
Encode Level Response (A/D)

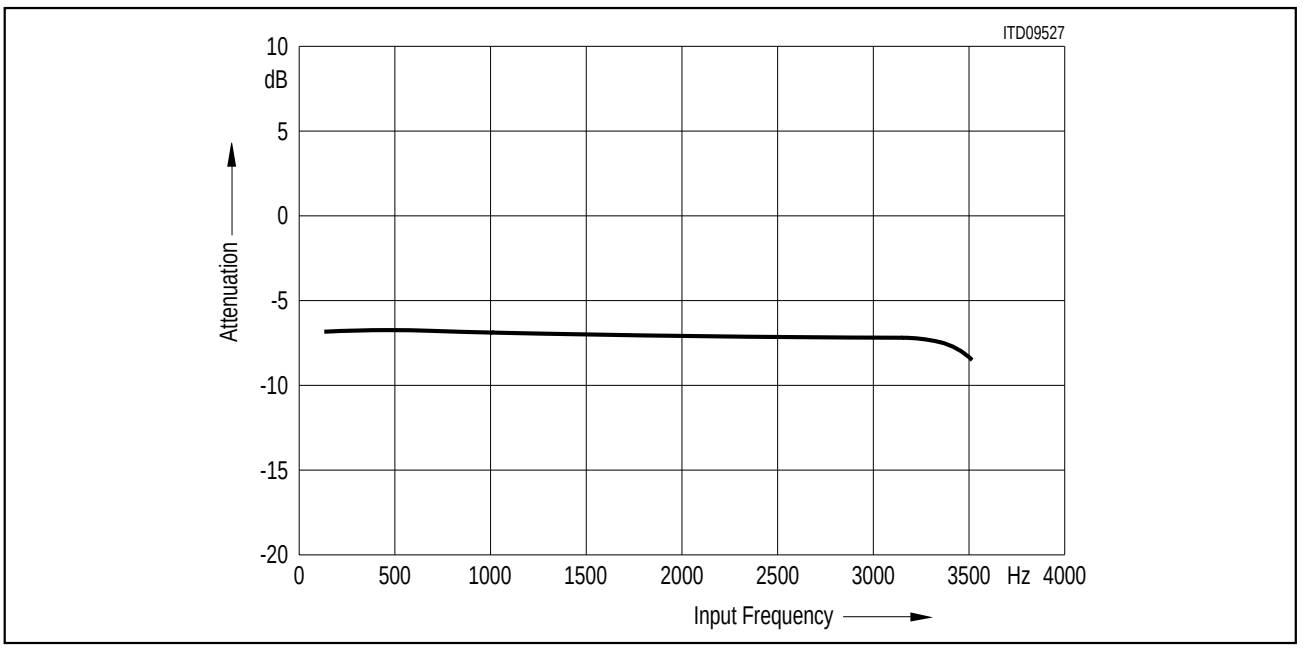

Figure 81
Decode Level Response (D/A)

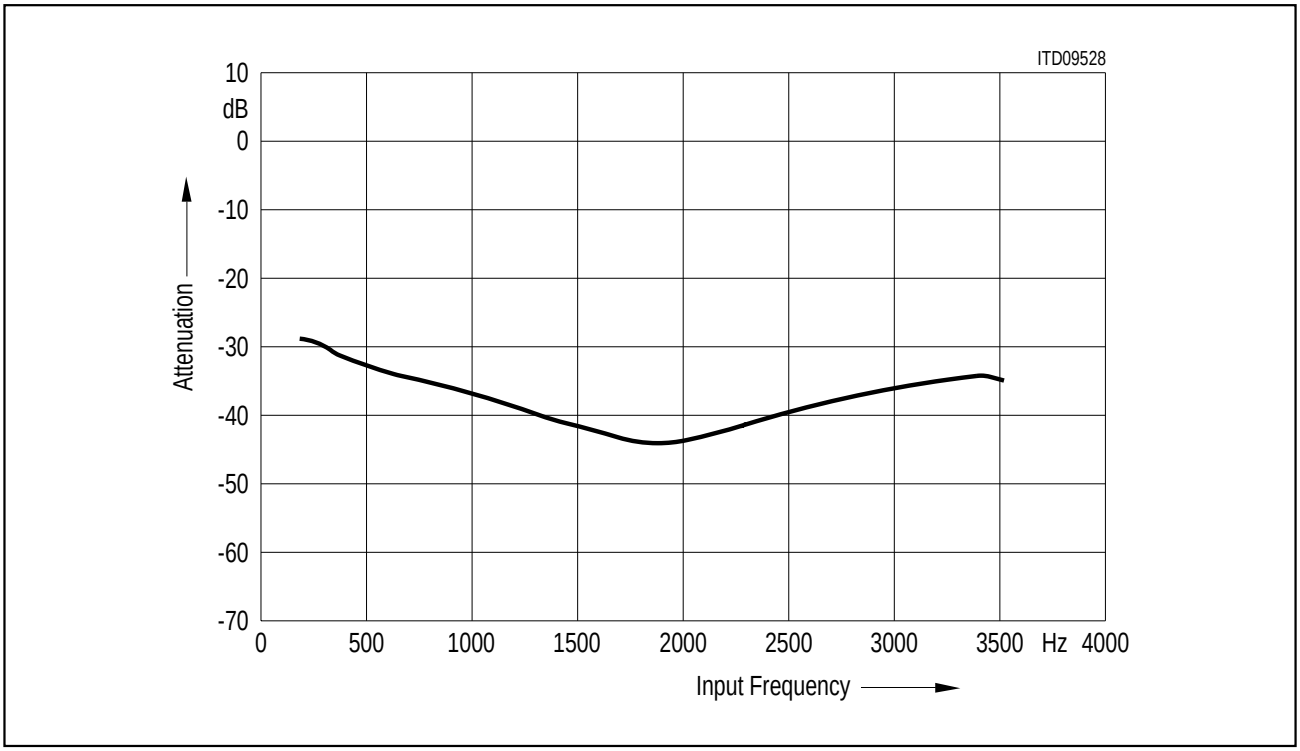

Figure 82
Transhybrid Loss

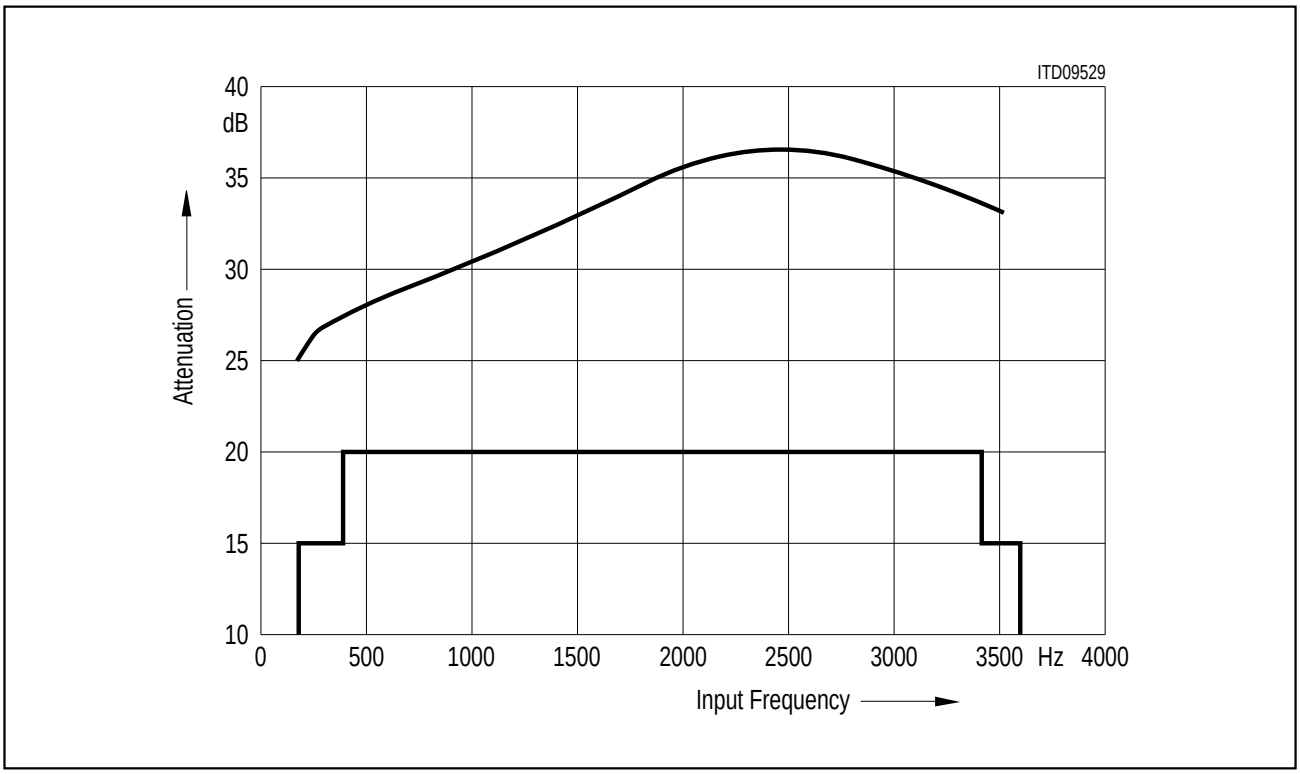

Figure 83
Return Loss