SIEMENS

# ICs for Communications

ISDN PC Adapter Circuit
IPAC

PSB 2115 Version 1.1
PSF 2115 Version 1.1

Delta Sheet 06.97

T2115-XV11-L2-7600

| PSB 2115<br>Revision History: Current Version: 06.97 | | |
|---|---|---|
| Previous Version: 05.97 | | |
| Page (in previous Version) | Page (in new Version) | Subjects (major changes since last revision) |
| | <br>3<br>4 | New functionality:<br>Soft Reset<br>Interrupt Output |
| | | |

**Edition 06.97**

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**ISDN PC Adapter Circuit** **PSB 2115**
**IPAC** **PSF 2115**

**Delta Sheet for Preliminary Data Sheet 03.97** **CMOS**

The features of the IPAC V1.1 are specified in the Preliminary Data Sheet 03.97. In addition to that the following features are provided.

## 1 Soft Reset

The host can issue a reset command to the IPAC which has the same functionality as a hardware reset. Bit POTA2:SRES is used as a RESET bit to release the reset, which has only effect on the internal functional blocks of the IPAC, the Reset pin is not activated.

**POTA2 - PCM Output Time Slot Assignment B2 (Read/Write)**

Value after reset: $00_H$

| | 7 | | | | 0 | |
|---|---|---|---|---|---|---|
| POTA2 | ENA | DUDD | SRES | TNTX | | (C9) |

**SRES... Soft Reset**

0: Deactivates ...

1: Activates ... the internal RESET state of the IPAC.

The RESET state is activated to the internal blocks of the IPAC when a ’1’ is written to SRES and it is active until the SRES-bit is set to ’0’ again, i.e. the host must ensure the required RESET timing of the IPAC which is 4 ms.

*Note: The other bits of the register are not described here as they are already contained in the Preliminary Data Sheet 03.97.*

## 2 Interrupt Output

The interrupt output of the IPAC is low active which is suitable if several interrrupt sources need to be connected together via a pull up resistor. Especially for single chip applications the IPAC additionally provides a high active interrupt output which is available at pin AUX2 (pin no. 33) in TE mode only.

**Table 1**
**AUX Pin Functions**

| Pin | TE mode | LT-T mode | LT-S mode |
|---|---|---|---|
| AUX0 | DRQTA | CH0 | CH0 |
| AUX1 | DRQRA | CH1 | CH1 |
| AUX2 | AUX2 / INT | CH2 | CH2 |
| AUX3 | AUX3 | AUX3 / FBOUT | AUX3 / FBOUT |
| AUX4 | AUX4 | AUX4 / PCMIN | AUX4 / PCMIN |
| AUX5 | AUX5 | AUX5 / PCMOUT | AUX5 / PCMOUT |
| AUX6 | $\overline{\text{INT0}}$ | $\overline{\text{INT0}}$ | $\overline{\text{INT0}}$ |
| AUX7 | $\overline{\text{INT1}}$ | $\overline{\text{INT1}}$ / SGOUT | $\overline{\text{INT1}}$ |

**AUX2 / INT**

If configured as output, pin AUX2 provides the high active interrupt output signal. If configured as input, it can be used as a general purpose input pin.

*Note: The other pins are not described here as they are already contained in the Preliminary Data Sheet 03.97.*