PS200
Data Sheet

PowerSmart® Configurable Lithium Ion/ Lithium Polymer Battery Charger

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PS200

PowerSmart® Configurable Lithium Ion/Lithium Polymer Battery Charger

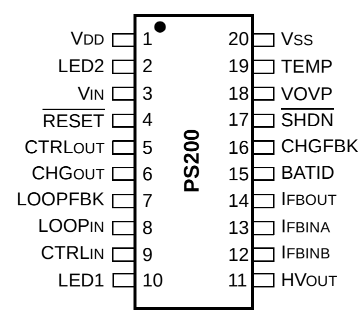
Features

- User configurable battery charger for Lithium Ion/ Lithium Polymer battery packs:
- 10-bit ADC for voltage, current and temperature measurement:
  - Accurate Voltage Regulation (+/-1%)
  - Accurate Current Regulation (+/-5%)
- Advanced Li Ion/Li Polymer Charge Algorithm:
  - Constant current/constant voltage charge
  - Charge qualification to detect shorted, damaged or heated cells
  - Precharge for deeply discharged cells
  - Configurable overtemperature and overvoltage charge suspension
  - Charge termination at user specified minimum current or time-out
- Maximum integration for optimal size:
  - Integrated voltage regulator
  - Internal 8 MHz clock oscillator
  - High-Frequency Switch mode charging – configurable switching frequency up to 1 MHz
- 256 bytes EEPROM storage for charging parameters
- Supports Switch mode charger topology
- Configurable charge status display via two LEDs
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Power-saving Sleep mode

Applications

- Single-Cell and Multi-Cell Lithium Ion and Lithium Polymer Battery Chargers
- Notebook Computers
- Personal Data Assistants
- Cellular Telephones
- Digital Still Cameras
- Camcorders
- Portable Audio Products
- Bluetooth® Devices

Pin Diagram



20-Pin PDIP, SOIC, SSOP

Pinout Description

Pin	Pin Name	Pin Type	Input Type	Output Type	Description
1	V_{DD}	Supply	Power	—	Supply voltage
2	LED2	O	—	CMOS	Status indicator
3	V_{IN}	I	Analog	—	Battery voltage input
4	$\overline{\text{RESET}}$	I	ST	—	Reset
5	$CTRL_{OUT}$	O	—	CMOS	PWM output for setting current level
6	CHG_{OUT}	O	—	CMOS	PWM output to a buck converter for charge control
7	LOOPFBK	I	Analog	—	Current feedback loop
8	$LOOP_{IN}$	I	Analog	—	Current feedback loop input
9	$CTRL_{IN}$	I	Analog	—	Current level control
10	LED1	O	—	CMOS	Status indicator
11	HV_{OUT}	O	—	HVOD	High-voltage, open-drain output pin (optional)
12	I_{FBINB}	I	Analog	—	Current feedback input pin B used for current scaling
13	I_{FBINA}	I	Analog	—	Current feedback input pin A used for current scaling
14	I_{FBOUT}	O	—	Analog	Current feedback output
15	BATID	I	Analog	—	Battery ID select
16	CHGFBK	I	Analog	—	Charge control feedback
17	$\overline{\text{SHDN}}$	O	—	Analog	Shutdown signal, active-low
18	VOVP	I	Analog	—	Overvoltage protection
19	TEMP	I	Analog	—	Battery temperature input
20	V_{SS}	Supply	Power	—	Supply ground

Legend: I = Input, O = Output, ST = Schmitt Trigger Input Buffer, HVOD = High-Voltage Open-Drain

 Preliminary

1.0 PRODUCT OVERVIEW

The PS200 provides an unprecedented level of configurability for charging Lithium Ion/Lithium Polymer battery packs. It's precision, 10-bit Analog-to-Digital converter and high-frequency Pulse-Width Modulator enable the PS200 to provide optimum control of charging algorithms for lithium battery chemistries. Special features include an internal voltage regulator and an internal clock oscillator that reduce external component count.

1.1 Multi-Step Charging

To ensure the proper treatment of lithium chemistries during extreme temperature and voltage conditions, multi-step charging is required. The PS200 starts the charging cycle upon sensing the presence of a battery pack and a valid charging supply. During charge qualification, the battery's temperature and voltage are measured to determine the appropriate initial state. The initial states include Charge Suspend, Precharge and Current Regulation. Charge Suspend halts charging when the user defined preset conditions for charging are not met. Precharge allows for the recovery of deeply discharged batteries by applying a low charge (or C) rate. Current Regulation provides constant current, voltage limited charge. Upon reaching the target voltage during Current Regulation, the Voltage Regulation state is entered. Charging continues at a constant voltage until the current decreases to the user specified minimum current threshold (I_{MIN}). The user specified minimum current threshold can be configured for various charging temperatures. At this threshold, charging is terminated and the End-Of-Charge state is reached.

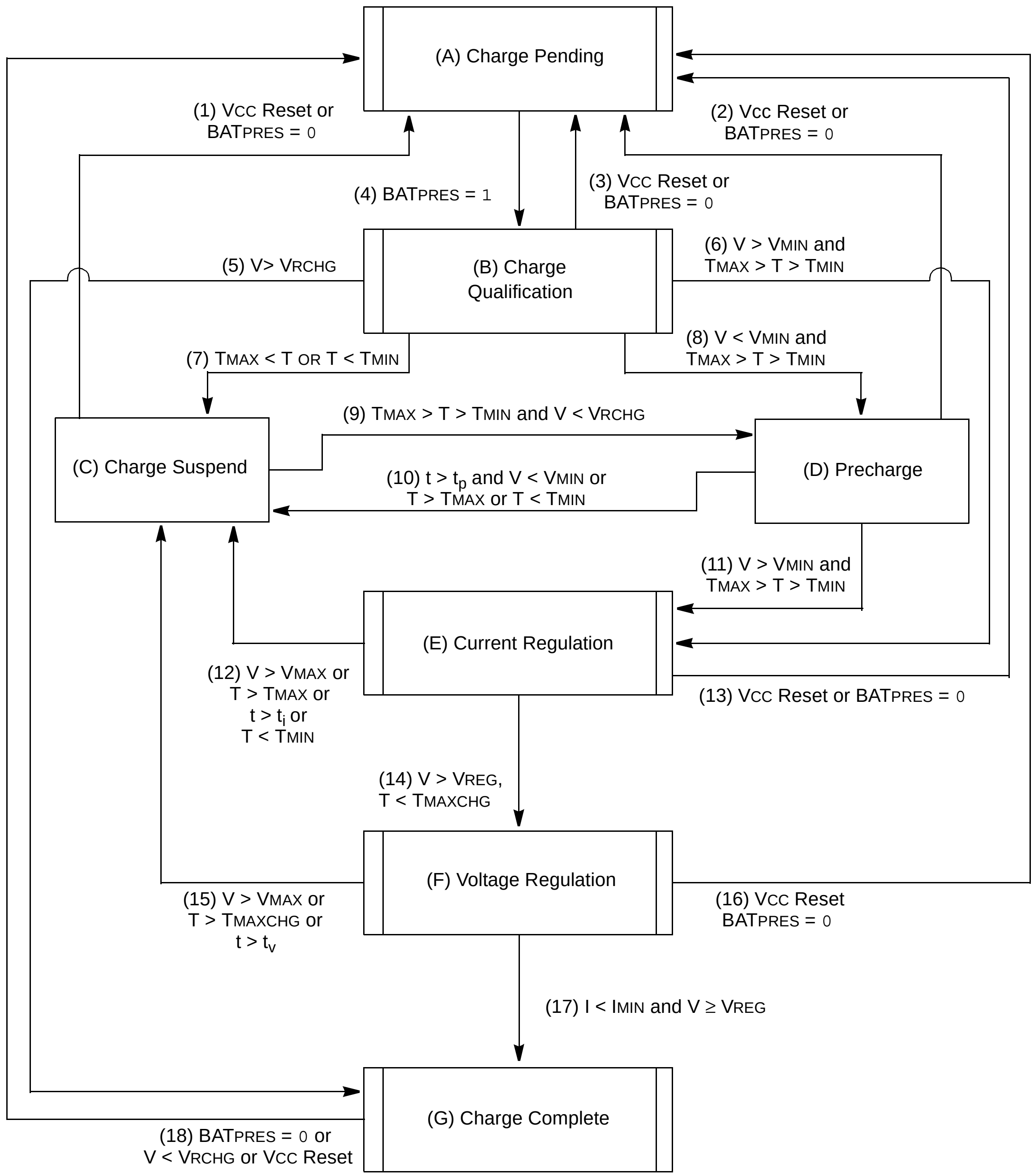
The state diagram illustrates the charging cycle (see Figure 1-1).

1.2 User Configurable Parameters

The PS200 supports user configurable parameters that allow for customizing the charging profile without changing the charger's hardware design. This feature allows for the maximum reuse of hardware, thus reducing time-to-market. These parameters include:

- Battery Temperature:
  - Minimum/maximum temperature for charge initiation
  - Maximum temperature allowed during charge
- Battery Voltage:
  - Minimum/maximum voltage for charge initiation
  - Target voltage during Voltage Regulation
  - Voltage at which the charger will restart charging after completion of a valid charge cycle
- Charge Current:
  - Target current during Current Regulation
  - Taper current threshold for End-Of-Charge during Voltage Regulation
  - Target current during Precharge
- Time:
  - Precharge time limit
  - Current Regulation time limit
  - Voltage Regulation time limit
- Status Display:
  - Two LEDs denote the charge states. Their flash rates can be modified.

FIGURE 1-1: PS200 STATE DIAGRAM LI CHARGER



Legend:

T	=	battery temperature
TMIN	=	minimum temperature allowed during charging
TMAX	=	maximum temperature allowed during charging
TMAXCHG	=	maximum temperature allowed during voltage regulation
V	=	battery voltage
VMIN	=	minimum voltage for entering current regulation
VMAX	=	maximum voltage for charge initiation
VREG	=	target voltage during charge regulation
VRCHG	=	voltage threshold at which charging will restart
I	=	charge current
IMIN	=	taper current threshold for End-Of-Charge during voltage regulation
t	=	time
t_p	=	precharge time limit
t_i	=	current regulation time limit
t_v	=	voltage current time limit
BATPRES	=	battery present variable; if '1', then battery is present; if '0', then battery is not present

Note: When the PS200 resets, it enters the Charge Pending state.

1.3 Features

The PS200 features are well-suited for Switch mode battery charging. The PS200 device's block diagram (Figure 1-2) is to be used in conjunction with the Switch mode charger example (Figure 4-1).

- Current/Voltage Measurement Block – The Current/Voltage Measurement Block consists of a 10-bit Analog-to-Digital converter, operational amplifiers and a comparator. The output of this block is fed into the Charge Control module. Please refer to Figure 1-2.

  The inputs into this block are to be connected as described in Figure 4-1. The following signals are inputs into this block:
  - LOOPFBK – to comparator
  - $LOOP_{IN}$ – to op amp and ADC
  - $CTRL_{IN}$ – to op amp
  - I_{FBINB} – to op amp
  - I_{FBINA} – to op amp
  - BATID – to ADC
  - TEMP – to ADC
  - CHGFBK – to comparator

  The following signals are outputs from this block:
  - I_{FBOUT} – from op amp
- Charge Control Module:
  - The charge control module generates a Pulse-Width Modulated signal called CHG_{OUT}. Its frequency is configurable and can be set up to 1 MHz. This signal is connected to an external DC/DC buck converter.
- Voltage Regulator
  - The integrated voltage regulator is designed to work with unregulated DC supplies.
  - There are guidelines that should be followed. A series limiting resistor (RV_{DD}) should be placed between the unregulated supply and the V_{DD} pin. The value for this series resistor (RV_{DD}) must be between R_{MIN} and R_{MAX} as shown in the following equation:

EQUATION 1-1:

$$R_{MAX} = \frac{Vs(min) - 5V) * 1000}{1.05 * (16\ mA + I(led))}$$

$$R_{MIN} = \frac{Vs(max) - 5V) * 1000}{.95 * (50\ mA)}$$

Where:

R_{MAX} = maximum value of series resistor (ohms)
R_{MIN} = minimum value of series resistor (ohms)

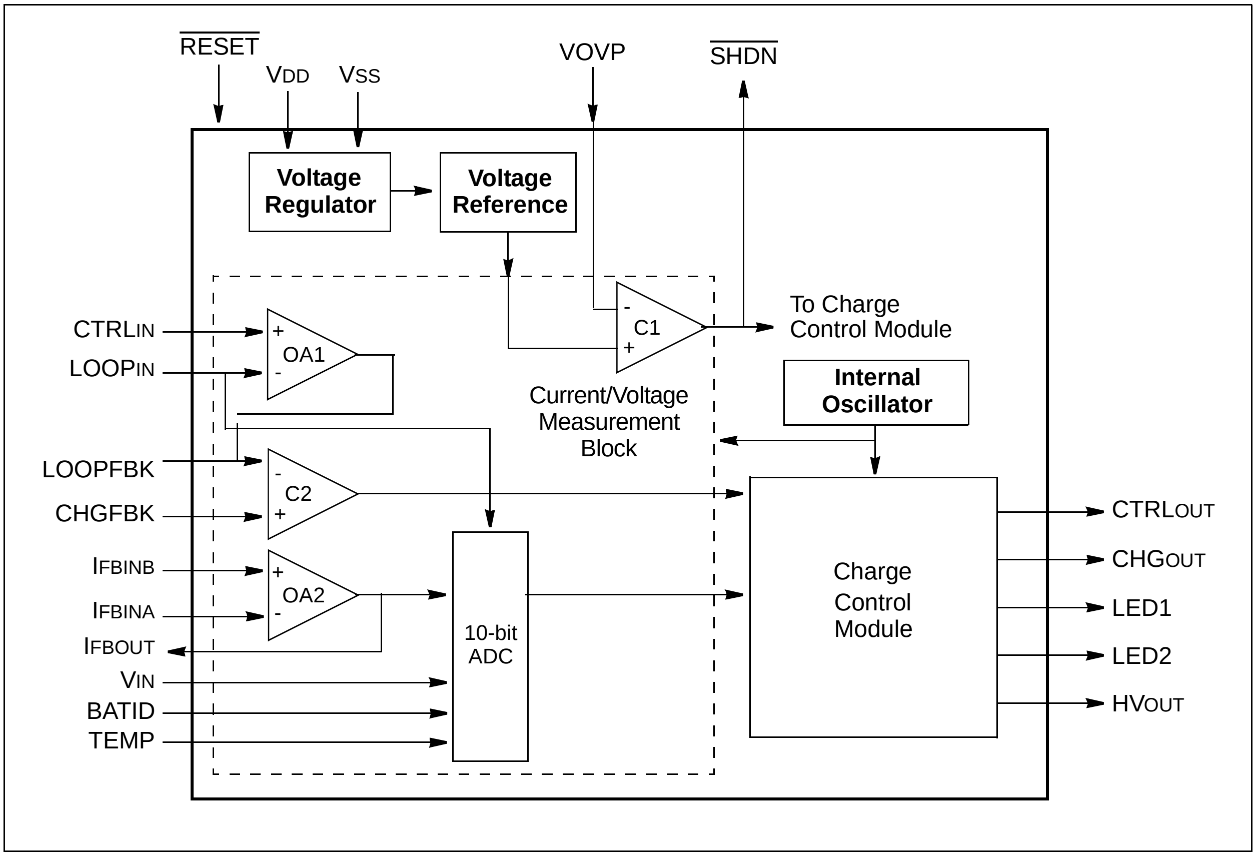
Vs(min) = minimum value of charger DC supply (V_{DC})
Vs(max) = maximum value of charger DC supply (V_{DC})

I(led) = total current drawn by all LEDs when illuminated simultaneously

The 1.05 and.95 constants are included to compensate for the tolerance of 5% resistors. The 16 mA constant is the anticipated load presented by the PS200, including the loading due to external components and a 4 mA minimum current for the shunt regulator itself. The 50 mA constant is the maximum acceptable current for the shunt regulator.

- The precision internal 8 MHz clock oscillator eliminates the need for external oscillator circuits.
- In-circuit configurability utilizing 256 bytes of on-board EEPROM.
- Power on Reset – The POR insures the proper start-up of the PS200 when voltage is applied to V_{DD}.
- Brown-out Reset – The BOR is activated when the input voltage falls to 2.1V; the PS200 is reset.

FIGURE 1-2: PS200 BLOCK DIAGRAM



2.0 ARCHITECTURAL OVERVIEW

To ensure the proper treatment of lithium chemistries during extreme temperature and voltage conditions, multi-step charging is required. The PS200 measures key voltage, temperature and time parameters. It compares them to user defined voltage, temperature and time limits. These limits are described in **Section 3.0 "User Configurable Parameters"**.

Note:	Refer to Figure 1-1 and Figure 2-1 for clarification when reading this section.

2.1 Charge Pending State – Beginning the Charge Cycle

The PS200 is initially set in the Charge Pending state (A). In this state, the presence of a battery pack must be sensed in order to begin the charging cycle. The PS200 comes up in the Charge Pending state, after a Reset, independent of the previous state.

2.2 Charge Qualification State

During charge qualification, the battery's temperature and voltage are measured to determine the next charging state. There are four possible next states (see Figure 1-1).

1. If the battery's temperature is outside of the limits for charge initiation (T_{MAX}, T_{MIN}) then the next state is Charge Suspend (C).
2. If the battery's voltage is less than the minimum voltage for charge initiation (V_{MIN}) and its temperature is within the limits for charge initiation (T_{MAX}, T_{MIN}), then the next state is Precharge (D).
3. If the battery's voltage is above the minimum voltage for charge initiation (V_{MIN}) and its temperature is within the limits for charge initiation (T_{MAX}, T_{MIN}), then the next state is Current Regulation (E).
4. If the battery's voltage is above the voltage at which charging will restart (V_{RCHG}), then the next state is Charge Complete (G).

2.3 Precharge State

The Precharge state allows for the recovery of a deeply discharged battery pack by applying a low charge rate. In this state, a user configured precharge current is applied to the battery, resulting in an increase in the battery's voltage (refer to Figure 2-1). There are three possible next states (see Figure 1-1).

1. If the battery's voltage is above the minimum voltage for charge initiation (V_{MIN}) and the battery's temperature is within the limits for charge initiation (T_{MAX}, T_{MIN}), then the next state is Current Regulation (E).
2. If the Precharge state time limit is exceeded (t_p) and the battery's voltage remains less than the minimum voltage for charge initiation (V_{MIN}), then the next state is Charge Suspend (C).

   If the Precharge state time limit is exceeded (t_p) and the battery's temperature is greater than the maximum temperature for charge initiation (T_{MAX}), then the next state is Charge Suspend (C).

   If the Precharge state time limit is exceeded (t_p) and the battery's temperature is less than the minimum temperature for charge initiation (T_{MIN}), then the next state is Charge Suspend (C).
3. If the battery pack is taken away (BAT_{PRES} = 0), then the PS200 enters the Charge Pending (A) state.

2.4 Charge Suspend State

In the Charge Suspend state, no current is applied to the battery pack. There are two possible next states (see Figure 1-1).

1. If the battery's temperature is within the limits for charge initiation (T_{MAX}, T_{MIN}) and its voltage is less than the voltage at which charging would restart (V_{RCHG}), then the next state is Precharge (D).
2. If the battery pack is taken away (BAT_{PRES} = 0), then the PS200 enters the Charge Pending (A) state.

2.5 Current Regulation State

The Current Regulation state can be entered from the Precharge state or Charge Qualification state. Battery charging is initiated. This state provides constant current, voltage limited charging (refer to Figure 2-1). The charge current is referred to as I_{REG} or the regulation current. While the current is applied, the battery's voltage increases until it reaches a voltage limit referred to as V_{REG} or regulation voltage. Charging continues, during which battery voltage and temperature are monitored. There are three possible next states.

1. If the battery's voltage reaches or exceeds the voltage limit, V_{REG} and its temperature remains below the maximum allowable during current regulated charging (T_{MAXCHG}), then the next state is Voltage Regulation (F).
2. If the battery exhibits any one of the following conditions then the next state is Charge Suspend (C):
   - Battery voltage exceeds upper voltage limit for charging (V_{MAX})
   - Battery temperature exceeds upper temperature limit for charging (T_{MAX})
   - Battery temperature is below the lower temperature limit for charging (T_{MIN})

   If the time in the Current Regulation state exceeds the time limit (t_i), then the next state is Charge Suspend (C).
3. If the battery pack is taken away (BAT_{PRES} = 0), then the PS200 enters the Charge Pending (A) state.

2.6 Voltage Regulation State

Voltage Regulation provides charging at a constant voltage while the charge current decreases (or tapers) to the user specified minimum current threshold (I_{MIN}). There are three possible next states.

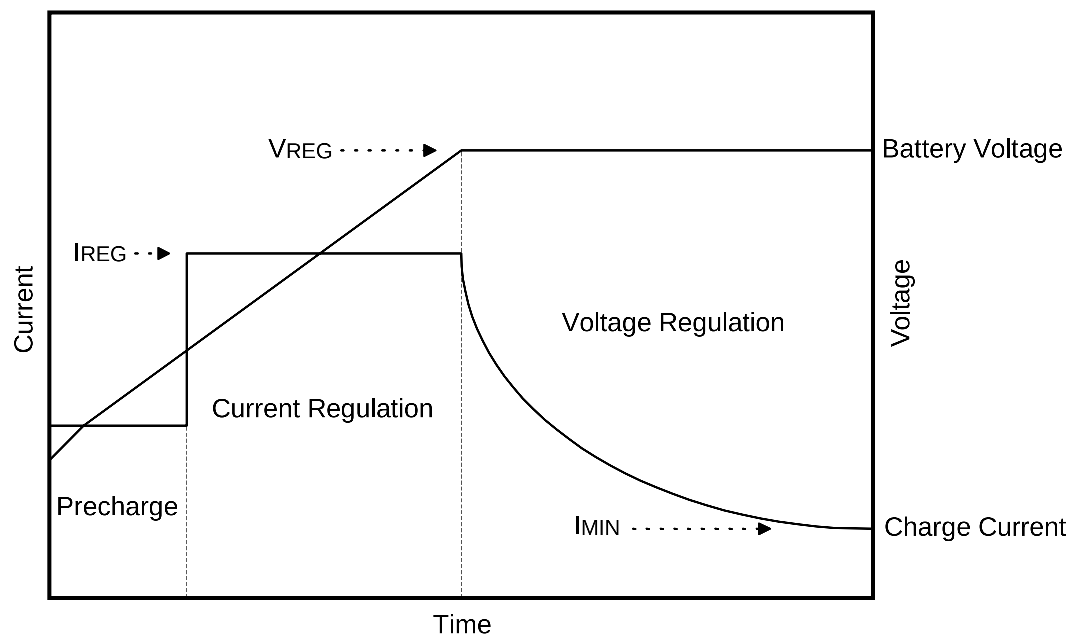
1. When the charge current reaches the taper current threshold for End-Of-Charge (I_{MIN}) and the battery's voltage remains at the regulated voltage value (V_{REG}), then the battery has reached the Charge Complete (G) state.
2. If the battery exhibits any one of the following conditions, then the next state is Charge Suspend (C).
   - Battery voltage exceeds upper voltage limit for charging (V_{MAX})
   - Battery temperature exceeds upper temperature limit for charging (T_{MAXCHG})

   If the time in the Voltage Regulation state exceeds the time limit (t_v), then the next state is Charge Suspend (C).
3. If the battery pack is taken away (BAT_{PRES} = 0), then the PS200 enters the Charge Pending (A) state.

2.7 Charge Cycle Complete State

The user specified minimum current threshold (I_{MIN}) can be configured for various charging temperatures. At this threshold, charging is terminated and the End-Of-Charge state is reached. The PS200 can renew the charge cycle by entering the Charge Pending (A) state when: 1) the battery is removed (BAT_{PRES} = 0), or 2) if the battery's voltage falls below the recharge threshold voltage (V_{RCHG}).

FIGURE 2-1: PS200 CHARGING PROFILE



NOTES:

3.0 USER CONFIGURABLE PARAMETERS

The PS200 device's configurable parameters allow for flexible changes in designing battery chargers. The parameters are categorized as follows:

- Configuration
- Precharge State
- Current Regulation State
- Voltage Regulation State
- LED Display Configuration

Please refer to Table 3-2 "PS200 Configurable Parameters".

3.1 Configuration Parameters

The configuration parameters provide an identity to the battery pack and provide its basic characteristics to the PS200.

- Manufacturing Name – A user defined text field for identifying the battery pack
- Device – A user defined text field for identifying the device in use
- Number of Cells – Identifies the number of series cells within the battery pack. The PS200 supports up to four cells.
- Battery Pack Capacity – Identifies the capacity of the battery pack in units of milliamp hour (mAh), a unit of current and time.
- PWM Frequency – The PS200 generates a PWM frequency for use in a Switch mode charger topology. The maximum frequency supported is 1 MHz.

3.2 Precharge State Parameters

The Precharge state parameters set the battery's operating condition in this initial battery charging phase. These parameters are:

- Minimum Voltage (V_{MIN}) – It is the minimum voltage required to enter Current Regulation. Otherwise, the charging process remains in the Precharge state.
- Maximum Temperature (T_{MAX}) – It is the maximum temperature allowed for the battery pack during any portion of the charging cycle. The PS200 allows a battery pack to continue its charging process as long as the battery pack's temperature is below T_{MAX}.
- Minimum Temperature (T_{MIN}) – It is the minimum temperature allowed for the battery pack during any portion of the charging cycle. The PS200 allows a battery pack to continue its charging process as long as the battery pack's temperature is above T_{MIN}.
- Precharge Current (I_{PRECHG}) – It is the current provided to the battery pack during the Precharge state. The value can be specified in mA.
- Precharge Time Limit (t_p) – It is the maximum amount of time allowable in the Precharge state. It is specified in minutes. The maximum number of minutes supported is 300.

3.3 Current Regulation State Parameters

The Current Regulation state parameters set the battery's operating condition in this second battery charging phase. These parameters are:

- Charge Current (I_{REG}) – It is the current provided to the battery pack during the Current Regulation state. The value can be specified in mA. The maximum C rate supported is 2.0.
- Maximum Temperature (T_{MAXCHG}) – It is the maximum battery temperature allowable during the Current Regulation state.
- Current Regulation Time Limit (t_i) – It is the maximum amount of time allowable in the Current Regulation state. It is specified in minutes. The maximum number of minutes supported is 300.
- Maximum Voltage (V_{MAX}) – It is the maximum voltage allowed for a battery pack's cell during any portion of the charging cycle. The values range from 4.0 to 4.5 volts. To determine the figure for a multi-cell pack, divide the maximum pack voltage by the number of cells. The PS200 allows a battery pack to continue its charging process as long as the battery pack's cell voltage is below V_{MAX}.

3.4 Voltage Regulation State Parameters

The Voltage Regulation state parameters set the battery's operating condition in this third battery charging phase. These parameters are:

- Target Voltage (V_{REG}) – It is the maximum voltage allowed per cell. 4.2V is the maximum supported value.
- Minimum Current (I_{MIN}) – During the Voltage Regulation phase, the current supplied to the battery pack decreases (or tapers) to a minimum current value. This value is compensated for temperature. Minimum current is implemented with a look-up table, 1 value for each of six temperature zones. The value for each zone is specified in units of 1/256 C-Rate (capacity). For example: Value of 10 for a 2000 mAh pack = 10/256 * 2000 = 78 mA.
- Voltage Regulation Time Limit (t_V) – It is the maximum amount of time allowable in the Voltage Regulation state. It is specified in minutes. The maximum number of minutes supported is 300.
- Maximum Voltage (V_{MAX}) – It is the maximum voltage allowed for a battery pack's cell during any portion of the charging cycle. The values range from 4.0 to 4.5 volts. To determine the figure for a multi-cell pack, divide the maximum pack voltage by the number of cells. The PS200 allows a battery pack to continue its charging process as long as the battery pack's cell voltage is below V_{MAX}.

3.5 LED Display Configuration

The PS200 supports two LEDs that communicate the charge state. It is recommended that LED1 be green, while LED2 be red. The table below shows the default blinking values.

TABLE 3-1: LED DISPLAY CONFIGURATION CHART

Charge State	LED1 (Green) Default	LED2 (Red) Default
Charge Pending	Off	Off
Charge Qualification	1 sec on, 4 sec off	Off
Charge Suspend	Off	On
Precharge	1 sec on, 1 sec off	Off
Current Regulation	1 sec on, 1 sec off	Off
Voltage Regulation	1 sec on, 1 sec off	Off
Charge Complete	On	Off

The user may customize the blinking of each LED.

TABLE 3-2: PS200 CONFIGURABLE PARAMETERS

Parameters in Step 1 – Configuration					
Parameter Name	**Variable Name**	**Min**	**Max**	**Default**	**Description**
Manufacturing Name	–	–	–	–	ASCII value.
Device	–	–	–	–	ASCII value.
Number of Cells	–	1	–	2	Number of cells in the pack.
Battery Pack Capacity (mAh)	–	500	65535	2,000	Typical value assumes 2-cell pack.
PWM Frequency (kHz)	–	100	1 MHz	250	Frequency is converted to period.
Parameters in Step 2 – Precharge State					
Parameter Name	**Variable Name**	**Min**	**Max**	**Default**	**Description**
Maximum Voltage (V)	VMAX	4.0	4.5	4.2	Maximum voltage allowed.
Minimum Voltage (V)	VMIN	0.0	3.0	2.0	Minimum voltage allowed.
Maximum Temperature for Charge Initiation (degC)	TMAX	0.0	85.0	40.0	Maximum temperature allowed.
Minimum Temperature for Charge Initiation (degC)	TMIN	0.0	85.0	0.0	Minimum temperature cannot be higher than maximum temperature.
Precharge Current (mA)	IPRECHG	0	65535	200	Current for precharging battery.
Precharge Time Limit (minutes)	t_p	0	300	45	Maximum value is 300 minutes.
Parameters in Step 3 – Current Regulation Phase					
Parameter Name	**Variable Name**	**Min**	**Max**	**Default**	**Description**
Charge Current (mA)	IREG	125	65535	2,000	Current defined for Current Regulation phase.
Maximum Temperature during Charge	TMAXCHG	0.0	85.0	55.0	Temperature measurement is an option.
Current Regulation Time Limit (min)	t_i	0	300	90	Maximum value is 300 minutes.
Parameters in Step 4 – Voltage Regulation Phase					
Parameter Name	**Variable Name**	**Min**	**Max**	**Default**	**Description**
Target Voltage	VREG	4	4.5	4.2	Maximum value is 4.5 volts.
Minimum Current (mA)	IMIN	0	65535	140	Minimum current is a function of temperature and capacity.
Restart Charging Threshold Voltage (V)	VRCHG	3.0	4.0	3.5	Voltage Threshold at which charging restarts (V)
Voltage Regulation Time Limit (min)	t_v	0	300	90	Maximum value is 300 minutes.
Parameters in Step 5 – LED Display Configuration					
Parameter Name	**Variable Name**	**Min**	**Max**	**Default**	**Description**
LED1 On/Off Time (sec)	LED1 mode	0.0	4.0	State Dep.	Increments of 0.25 second. 8-bit word defines the LED state.
LED2 On/Off Time (sec)	LED2 mode	0.0	4.0	State Dep.	Increments of 0.25 second. 8-bit word defines the LED state.

Default LED Display Configuration		
Charge State	**LED1 (Green) Default**	**LED2 (Red) Default**
Charge Pending	Off	Off
Charge Qualification	1 sec on, 4 sec off	Off
Charge Suspend	Off	On
Precharge	1 sec on, 1 sec off	Off
Current Regulation	1 sec on, 1 sec off	Off
Voltage Regulation	1 sec on, 1 sec off	Off
Charge Complete	On	Off

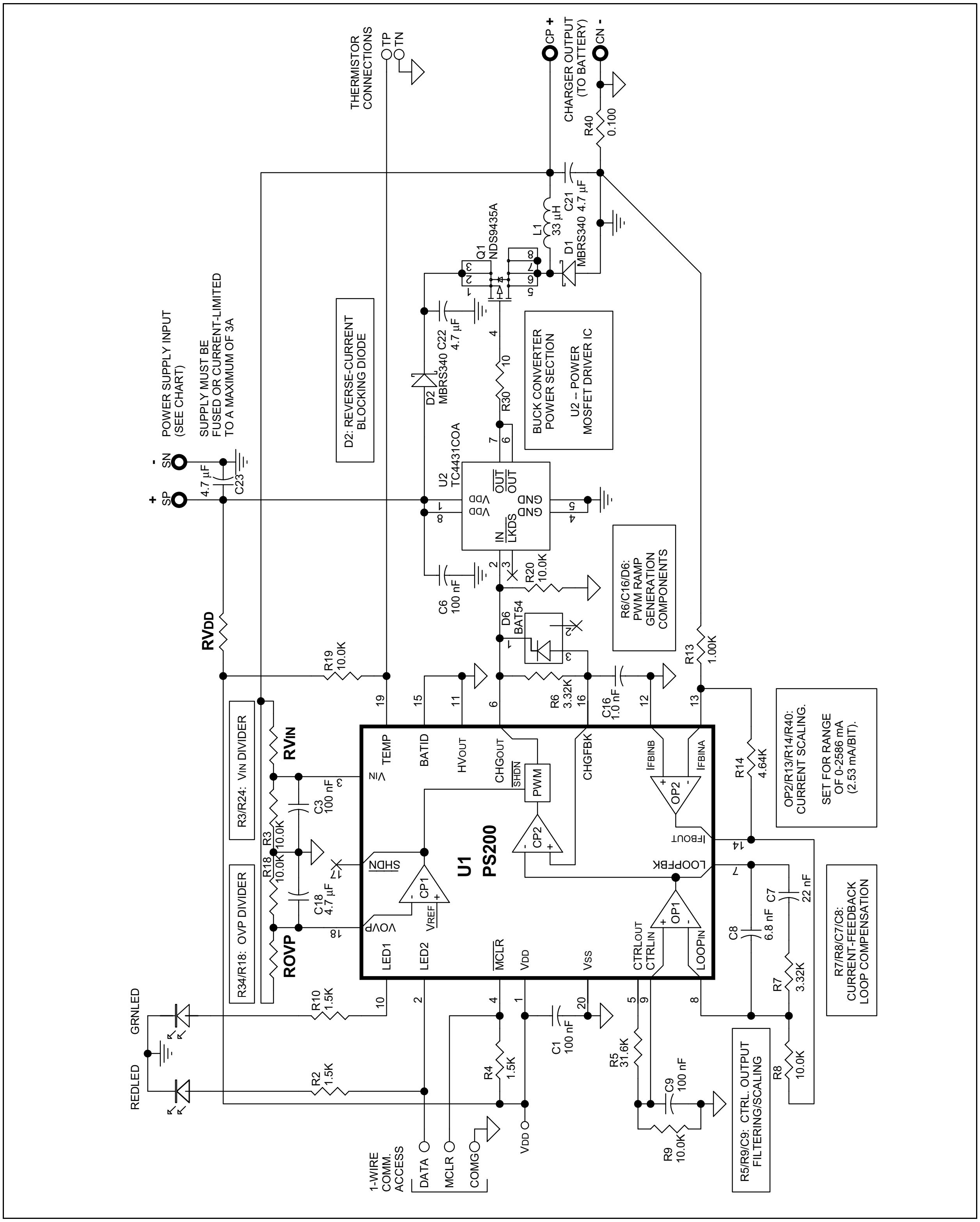
NOTES:

4.0 APPLICATION

Figure 4-1 is an example of the PS200 in a Switch mode charger for Lithium Ion batteries. The sense resistor (R_{SENSE}) is in a low side configuration.

Refer to the Microchip web site (www.microchip.com) for the latest Application Notes that reference this theory of operation and component values.

FIGURE 4-1: SWITCH MODE CHARGER CIRCUIT EXAMPLE



NOTES:

5.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Ambient temperature under bias .... -40 to +125°C
Storage temperature .... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... -0.3 to +6.5V
Voltage on $\overline{RESET}$ with respect to Vss .... -0.3 to +13.5V
Voltage on HV_{OUT} with respect to Vss .... 0V to +8.5V
Voltage on all other pins with respect to V_{SS} .... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) .... 800 mW
Maximum current out of V_{SS} pin .... 300 mA
Maximum current into V_{DD} pin .... 250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) .... ± 20 mA
Output clamp current, I_{OK} (Vo < 0 or Vo >V_{DD}) .... ± 20 mA
Maximum output current sunk by any I/O pin .... 25 mA(2)
Maximum output current sourced by each Port .... 50 mA(2)

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.

2: Total source current must not exceed the shunt regulator capacity.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.1 Reliability Targets

The device must be designed to target the following reliability specifications:

ESD: ±4000V HBM ±400V MM all pins including V_{DD}, V_{SS}, $\overline{RESET}$

Latch-up: ±400 mA @ 125°C

5.2 Design Targets

The AC/DC specifications included in the following sections are preliminary specifications that we intend to publish at product introduction. As the product matures, we intend to expand the specifications. Therefore, design should try and meet the following extended V_{DD}/temperature targets:

1. Frequency of operation: DC – 4 MHz, V_{DD} = 2.0V – 5.5V, -40°C to 125°C
2. Frequency of operation: DC – 20 MHz, V_{DD} = 4.5V – 5.5V, -40°C to 125°C

5.3 DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to +85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001B D001C	VDD	Supply Voltage	2.0 4.5	— —	5.0 5.0	V V	FOSC <= 4 MHz FOSC > 4 MHz
D002	VDR	RAM Data Retention Voltage(1)	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	VDD voltage required to initiate a Brown-out Detect	—	2.1	—	V	
D010S	IDD	Supply Current(2)	—	—	—	mA	VDD and current are constant due to shunt regulator.
D020	IPD	Power-down Current(3)	—	2.9	TBD	nA	VDD = 5.0V, WDT disabled

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; $\overline{\text{RESET}}$ = VDD.

3: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD and VSS.

5.4 Shunt Regulator

TABLE 5-1: SHUNT REGULATOR SPECIFICATIONS

Shunt Regulator Specifications	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to +125°C					
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Shunt Voltage	VSHUNT	4.75	—	5.25	Volts	
Shunt Current	ISHUNT	4	—	50	mA	
Shunt Resistance	RSHUNT	—	—	3	Ω	
Settling Time*	TSETTLE	—	—	150	ns	To 1% of final value
Load Capacitance	CLOAD	0.01	—	10	µF	Bypass capacitor on VDD pin
Regulator Operating Current	ΔISNT	—	180	—	µA	Includes band gap reference current

* These parameters are characterized but not tested.

Note: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

 Preliminary

5.5 DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to +85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	V_{IL}	**Input Low Voltage**					
D032		$\overline{\text{RESET}}$	V_{SS}	—	0.2 V_{DD}	V	4.5V ≤ V_{DD} ≤ 5.5V, otherwise entire range
	V_{IH}	**Input High Voltage**					
D042		$\overline{\text{RESET}}$	0.8 V_{DD}	—	V_{DD}	V	4.5V ≤ V_{DD} ≤ 5.5V, otherwise entire range
	I_{IL}	**Input Leakage Current**(2)					
D060A		Analog inputs	—	±0.1	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
D061		$\overline{\text{RESET}}$(1)	—	±1	±5	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
		Output Low Voltage					
D080	V_{OL}	Pins LED1, LED2, $CTRL_{OUT}$, CHG_{OUT}, HV_{OUT}	—	—	0.6	V	I_{OL} = 8.5 mA, V_{DD} = 4.5V
		Output High Voltage					
D090	V_{OH}	Pins LED1, LED2, $CTRL_{OUT}$, CHG_{OUT}, HV_{OUT}	V_{DD} – 0.7	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 4.5V

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{\text{RESET}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

5.6 DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to +85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D101	C_{IO}	Pins LED1, LED2, $CTRL_{OUT}$, CHG_{OUT}, HV_{OUT}	—	—	50*	pF	
		Data EEPROM Memory					
D120	E_D	Endurance	1M	10M	—	E/W	25°C at 5V
D121	V_{DRW}	V_{DD} for read/write	V_{MIN}	—	5.5	V	V_{MIN} = Minimum operating voltage
D122	T_{DEW}	Erase/Write cycle time	—	5	6	ms	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

5.7 AC Characteristics: PS200 (Industrial)

FIGURE 5-1: EXTERNAL CLOCK TIMING

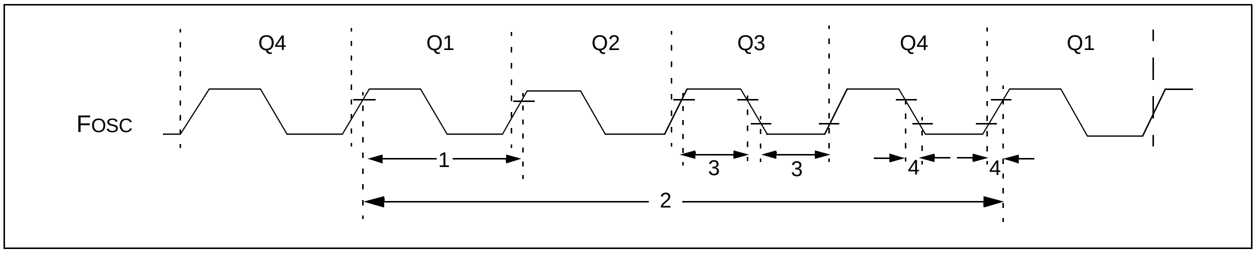


TABLE 5-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	Oscillator Frequency(1)	—	8	—	MHz	Using PS200 internal oscillator
1	Tosc	Oscillator Period(1)	—	125	—	ns	Using PS200 internal oscillator

† Data in "Typ" column is at 5 V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 5-2: CLKO AND I/O TIMING

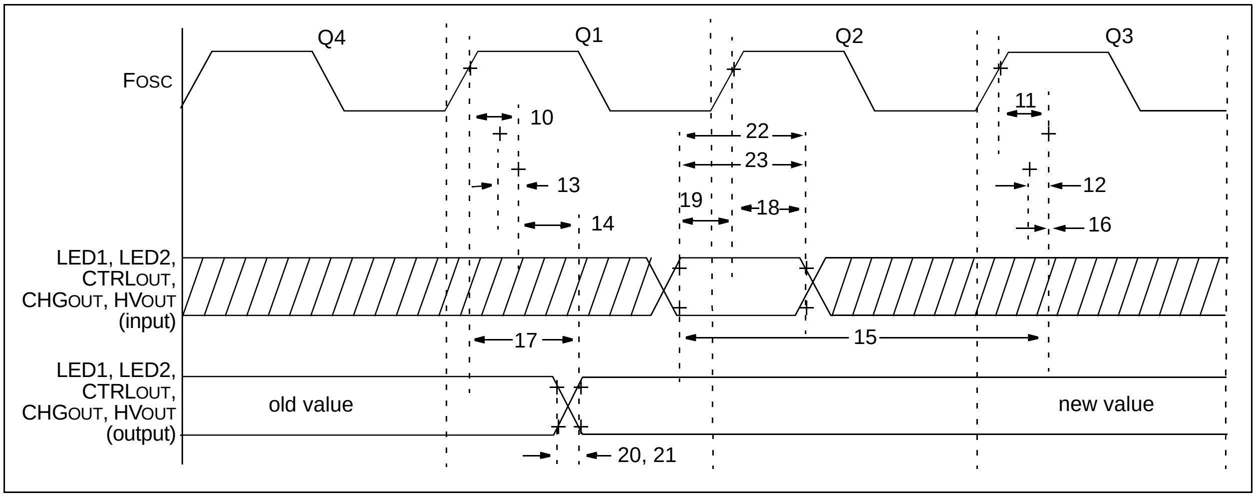


TABLE 5-3: CLKO AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
17	TosH2ioV	FOSC↑ (Q1 cycle) to Port Out Valid	—	50	150*	ns	
			—	—	300	ns	
18	TosH2ioI	FOSC↑ (Q2 cycle) to Port Input Invalid (I/O in hold time)	100	—	—	ns	
19	TioV2osH	Port Input Valid to FOSC↑ (I/O in setup time)	0	—	—	ns	
20	TioR	Port Output Rise Time	—	10	40	ns	
21	TioF	Port Output Fall Time	—	10	40	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0 V, 25°C unless otherwise stated.

FIGURE 5-3: RESET AND POWER-UP TIMER TIMING

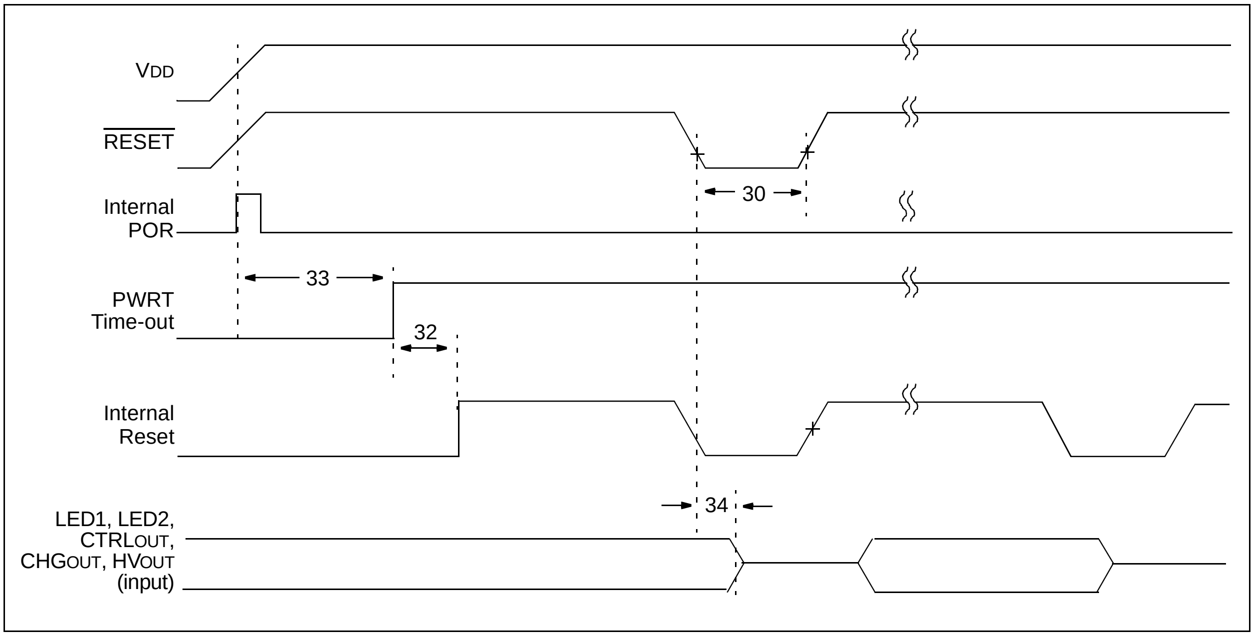


FIGURE 5-4: BROWN-OUT DETECT TIMING AND CHARACTERISTICS

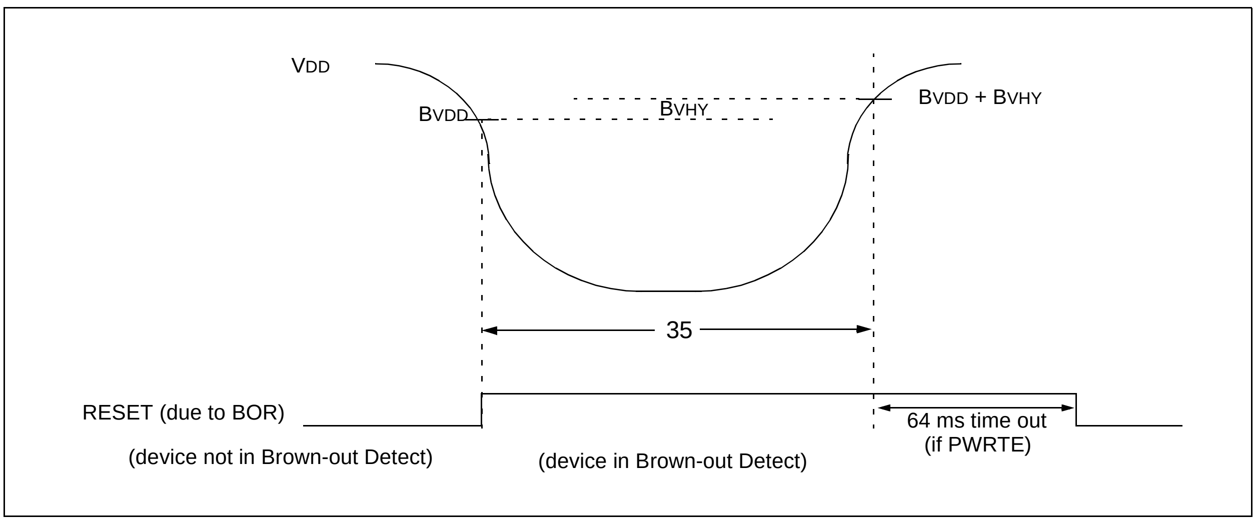


TABLE 5-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT DETECT REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	T_{MCL}	$\overline{RESET}$ Pulse Width (low)	2 11	— 18	— 24	µs ms	V_{DD} = 5 V, -40°C to +85°C Extended temperature
32	T_{OST}	Oscillation Start-up Timer Period	—	1024 T_{OSC}	—	—	T_{OSC} = F_{OSC} period
33*	T_{PWRT}	Power up Timer Period (4 x T_{WDT})	28* TBD	64 TBD	132* TBD	ms ms	V_{DD} = 5 V, -40°C to +85°C
34	T_{IOZ}	I/O high-impedance from $\overline{RESET}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
	B_{VDD}	Brown-out Detect voltage	2.025		2.175	V	
	B_{VHY}	Brown Out hysteresis		25		mV	
35	T_{BOR}	Brown-out Detect pulse width	100*	—	—	µs	$V_{DD} \leq B_{VDD}$ (D005)

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5 V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 5-5: PRECISION INTERNAL OSCILLATOR PARAMETERS

Param No.	Sym	Characteristic	Freq Tolerance	Min	Typ†	Max	Units	Conditions
F10	F_{OSC}	Internal Calibrated INTOSC Frequency(1)	±1%	—	8.00	TBD	MHz	V_{DD} and Temperature (TBD)
			±2%	—	8.00	TBD	MHz	2.5V ≤ V_{DD} ≤ 5.5V 0°C ≤ T_A ≤ +85°C
			±5%	—	8.00	TBD	MHz	2.0V ≤ V_{DD} ≤ 5.5V -40°C ≤ T_A ≤ +85°C (Ind.) -40°C ≤ T_A ≤ +125°C (Ext.)
F14	T_{IOSCST}	Oscillator wake-up from SLEEP start-up time*	—	—	TBD	TBD	µs	V_{DD} = 2.0V, -40°C to +85°C
			—	—	TBD	TBD	µs	V_{DD} = 3.0V, -40°C to +85°C
			—	—	TBD	TBD	µs	V_{DD} = 5.0V, -40°C to +85°C

Legend: TBD = To Be Determined

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 µF and .01 µF values in parallel are recommended.

FIGURE 5-5: CTRLOUT TIMINGS (PIN 5)

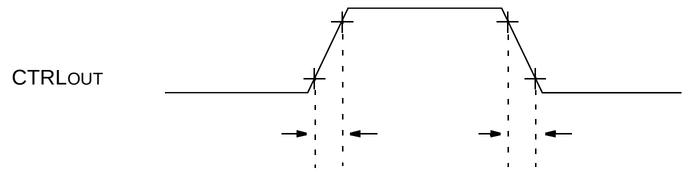


TABLE 5-6: CTRLOUT REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
53*	TccR	CTRLOUT Output Rise Time	—	25	50	ns	
54*	TccF	CTRLOUT Output Fall Time	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

5.8 Current Voltage Measurement Block

TABLE 5-7: DC CHARACTERISTICS (PINS LOOPIN, CTRLIN, IFBINB, IFBINA INPUTS; PIN IFBOUT OUTPUT)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** V_{DD} = 2.7V to 5.5V, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and V_{OUT} ~ V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Sym**	**Parameters**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
001	V_{OS}	**Input Offset Voltage**	—	±5	—	mV	
		Input Current and Impedance					
002	I_B	Input Bias Current	—	±2*	—	nA	
003	I_{OS}	Input Offset Bias Current	—	±1*	—	pA	
		Common Mode					
004	V_{CM}	Common Mode Input Range	V_{SS}	—	V_{DD} – 1.4	V	V_{DD} = 5V
005	CMR	Common Mode Rejection	TBD	70	—	dB	V_{CM} = V_{DD}/2, Frequency = DC
		Open-Loop Gain					
006A	A_{OL}	DC Open-Loop Gain	—	90	—	dB	No load
006B	A_{OL}	DC Open-Loop Gain	—	60	—	dB	Standard load
		Output					
007	V_{OUT}	Output Voltage Swing	V_{SS} + 50	—	V_{DD} – 50	mV	To V_{DD}/2 (20 kΩ connected to V_{DD}
008	I_{SC}	Output Short Circuit Current	—	25	TBD	mA	20 kΩ + 20 pF to V_{SS})
		Power Supply					
010	PSR	Power Supply Rejection	80	—	—	dB	

Legend: TBD = To Be Determined
* These parameters are characterized but not tested.

TABLE 5-8: AC CHARACTERISTICS (PINS LOOPIN, CTRLIN, IFBINB, IFBINA INPUTS; PIN IFBOUT OUTPUT)

AC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** V_{DD} = 2.7V to 5.5V, V_{SS} = GND, T_A = 25°C, VCM = V_{DD}/2, RL = 100 kΩ to V_{DD}/2 and V_{OUT} = V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Sym**	**Parameters**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
011	GBWP	**Gain Bandwidth Product**	—	3	—	MHz	V_{DD} = 5V
012	T_{ON}	**Turn On Time**	—	10	TBD	µs	V_{DD} = 5V
013	Θ_M	**Phase Margin**	—	60	—	degrees	V_{DD} = 5V
014	SR	**Slew Rate**	2	TBD	—	V/µs	V_{DD} = 5V

Legend: TBD = To Be Determined

TABLE 5-9: COMPARATOR SPECIFICATIONS (PINS LOOPFBK, CHGFBK, $\overline{SHDN}$, VOVP)

Comparator Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
C01	V_{OS}	Input Offset Voltage	—	± 2	± 5	mV	
C02	V_{CM}	Input Common Mode Voltage	0	—	V_{DD} – 1.5	V	
C03	I_{LC}	Input Leakage Current	—	—	200*	nA	
C04	C_{MRR}	Common Mode Rejection Ratio	+70*	—	—	dB	
C05	T_{RT}	Response Time(1)	— —	— —	20* 40*	ns ns	Internal Output to pin

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (V_{DD} – 1.5)/2, while the other input transitions from V_{SS} to V_{DD} – 1.5V.

TABLE 5-10: COMPARATOR VOLTAGE REFERENCE (V_{REF}) SPECIFICATIONS

Comparator Voltage Reference Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
CV01	CV_{RES}	Resolution	— —	V_{DD}/24* V_{DD}/32	— —	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV02		Absolute Accuracy	— —	— —	±1/4* ±1/2*	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03		Unit Resistor Value (R)	—	2K*	—	Ω	
CV04		Settling Time(1)	—	—	10*	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

TABLE 5-11: A/D CONVERTER CHARACTERISTICS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	N_R	Resolution	—	—	10 bits	bit	
A02	E_{ABS}	Total Absolute Error*(1)	—	—	±1	LSb	V_{REF} = 5.0V
A03	E_{IL}	Integral Error	—	—	±1	LSb	V_{REF} = 5.0V
A04	E_{DL}	Differential Error	—	—	±1	LSb	No missing codes to 10 bits V_{REF} = 5.0V
A05	E_{FS}	Full Scale Range	2.2*	—	5.5*	V	
A06	E_{OFF}	Offset Error	—	—	±1	LSb	V_{REF} = 5.0V
A07	E_{GN}	Gain Error	—	—	±1	LSb	V_{REF} = 5.0V
A10	—	Monotonicity	—	guaranteed(2)	—	—	$V_{SS} \le V_{AIN} \le V_{REF}$
A20 A20A	V_{REF}	Reference Voltage	2.2(4) 2.5	—	— V_{DD} + 0.3	V	 Absolute minimum to ensure 10-bit accuracy
A25	V_{AIN}	Analog Input Voltage	V_{SS}	—	V_{REF}(5)	V	
A30	Z_{AIN}	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
A50	I_{REF}	V_{REF} Input Current*(3)	10 —	— —	1000 10	µA µA	During V_{AIN} acquisition. Based on differential of V_{HOLD} to V_{AIN}. During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes Integral, Differential, Offset and Gain Errors.

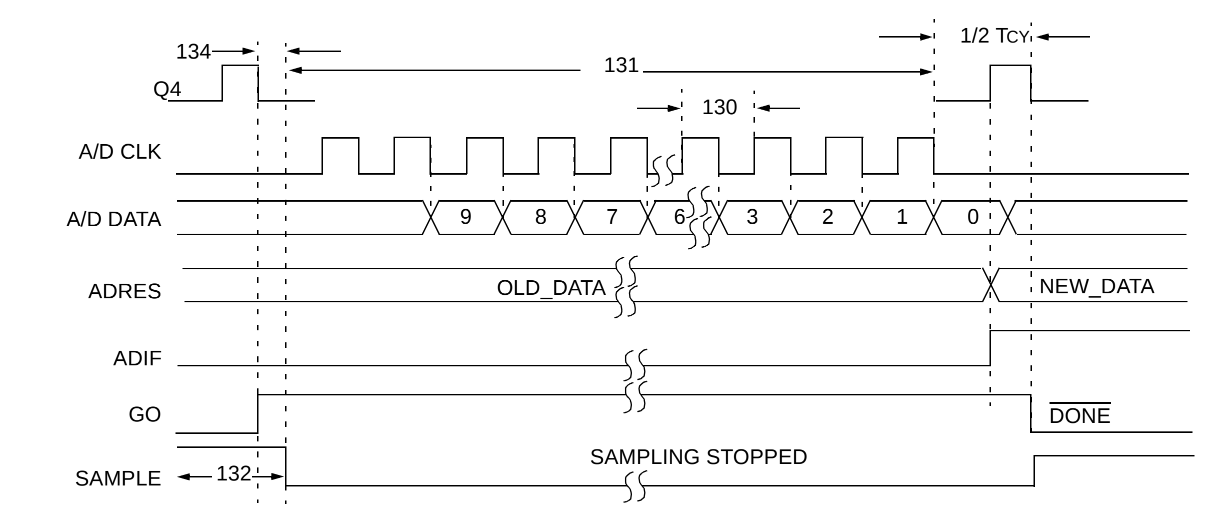
2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: V_{REF} current is from external V_{REF} or V_{DD} pin, whichever is selected as reference input.

4: Only limited when V_{DD} is at or below 2.5V. If V_{DD} is above 2.5V, V_{REF} is allowed to go as low as 1.0V.

5: Analog input voltages are allowed up to V_{DD}, however, the conversion accuracy is limited to V_{SS} to V_{REF}.

FIGURE 5-6: A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

TABLE 5-12: A/D CONVERSION REQUIREMENTS

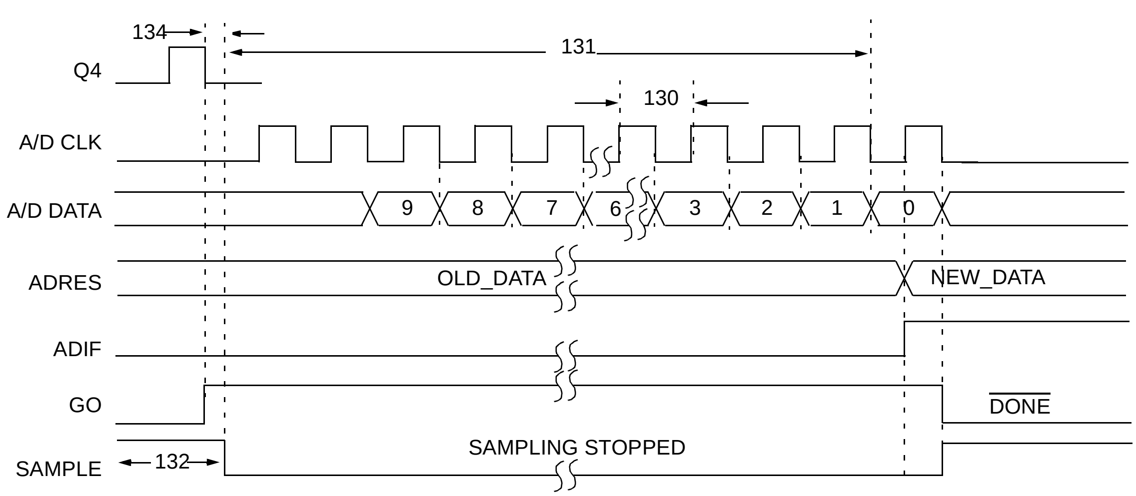
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*	T_{AD}	A/D Clock Period	1.6	—	—	µs	T_{OSC} based, $V_{REF} \geq 2.5V$
			3.0*	—	—	µs	T_{OSC} based, V_{REF} full range
130*	T_{AD}	A/D Internal RC Oscillator Period					ADCS<1:0> = `11` (RC mode)
			3.0*	6.0	9.0*	µs	At V_{DD} = 2.5V
			2.0*	4.0	6.0*	µs	At V_{DD} = 5.0V
131*	T_{CNV}	Conversion Time (not including acquisition time)(1)	—	11 T_{AD}	—	T_{AD}	Set GO bit to new data in A/D Result register
132*	T_{ACQ}	Acquisition Time	—	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on C_{HOLD}).
134*	T_{GO}	Q4 to A/D Clock Start	—	$T_{OSC}/2$	—	—	If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following T_{CY} cycle.

FIGURE 5-7: A/D CONVERSION TIMING (SLEEP MODE)

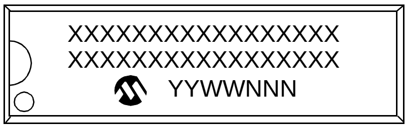


Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

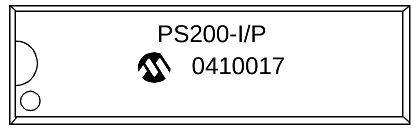
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

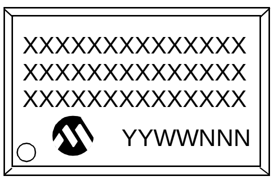
20-Lead PDIP



Example

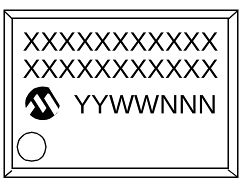


20-Lead SOIC

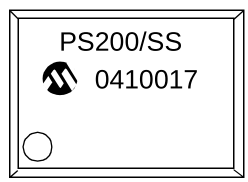


Example

20-Lead SSOP



Example



Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

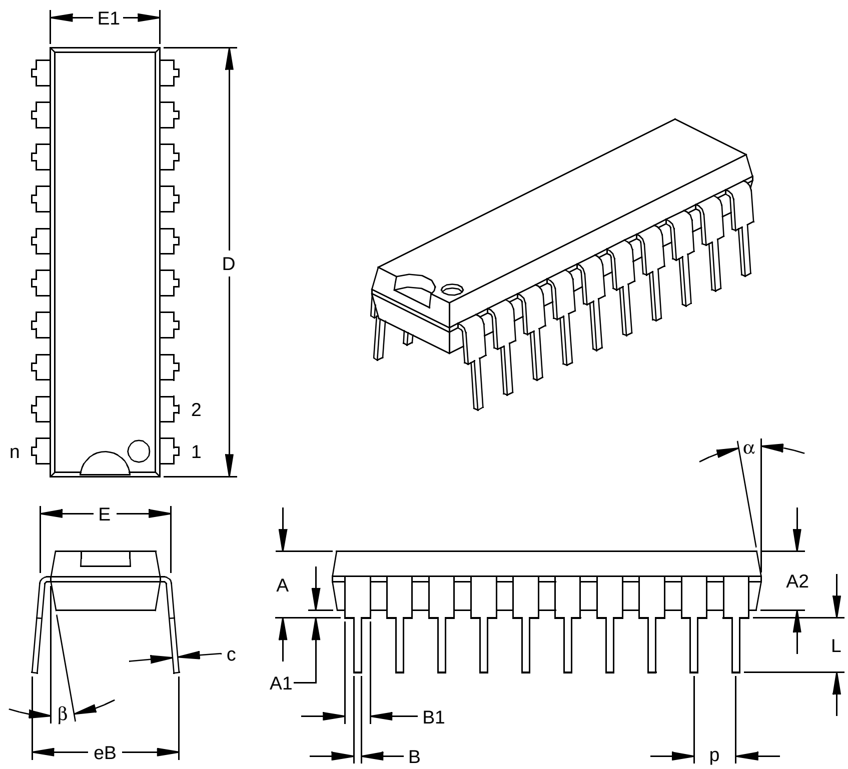
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard device marking consists of Microchip part number, year code, week code, and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

6.2 Package Details

The following sections give the technical details of the packages.

20-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



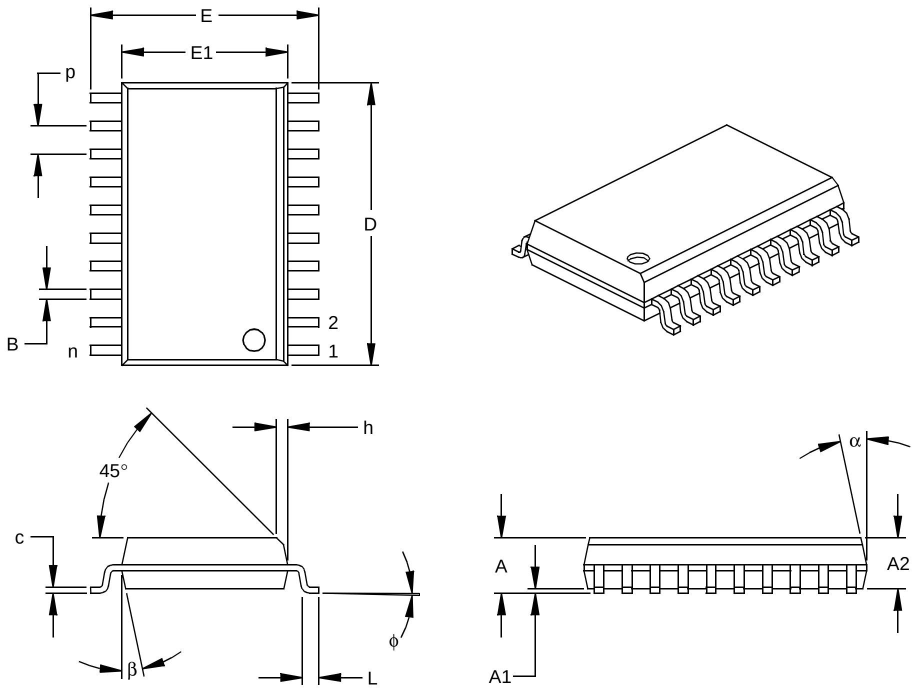
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.295	.310	.325	7.49	7.87	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	1.025	1.033	1.040	26.04	26.24	26.42
Tip to Seating Plane	L	.120	.130	.140	3.05	3.30	3.56
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.055	.060	.065	1.40	1.52	1.65
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-019

 Preliminary

20-Lead Plastic Small Outline (SO) – Wide, 300 mil Body (SOIC)

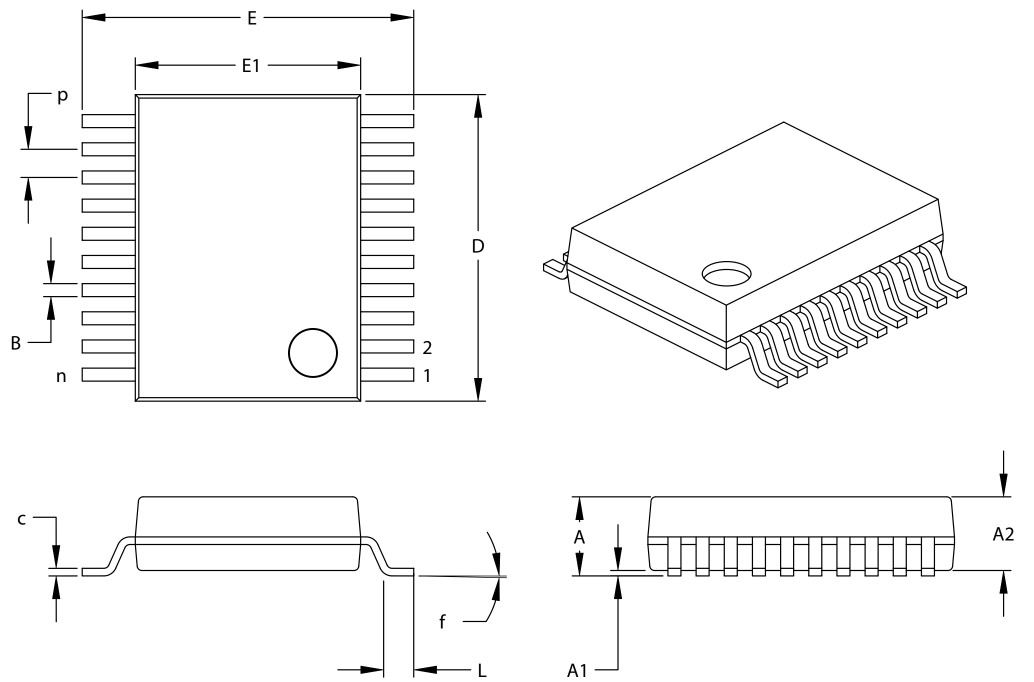


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.496	.504	.512	12.60	12.80	13.00
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-094

20-Lead Plastic Shrink Small Outline (SS) – 209 mil Body, 5.30 mm (SSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	-	-	.079	-	-	2.00
Molded Package Thickness	A2	.065	.069	.073	1.65	1.75	1.85
Standoff	A1	.002	-	-	0.05	-	-
Overall Width	E	.291	.307	.323	7.40	7.80	8.20
Molded Package Width	E1	.197	.209	.220	5.00	5.30	5.60
Overall Length	D	.272	.283	.289	.295	7.20	7.50
Foot Length	L	.022	.030	.037	0.55	0.75	0.95
Lead Thickness	c	.004	-	.010	0.09	-	0.25
Foot Angle	f	0°	4°	8°	0°	4°	8°
Lead Width	B	.009	-	.015	0.22	-	0.38

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-150

Drawing No. C04-072

Revised 11/03/03

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Device	PS200		
Temperature Range	I	= -20°C to +85°C (Industrial)	
Package	P	=	PDIP
	SO	=	SOIC
	SS	=	SSOP

Examples:

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