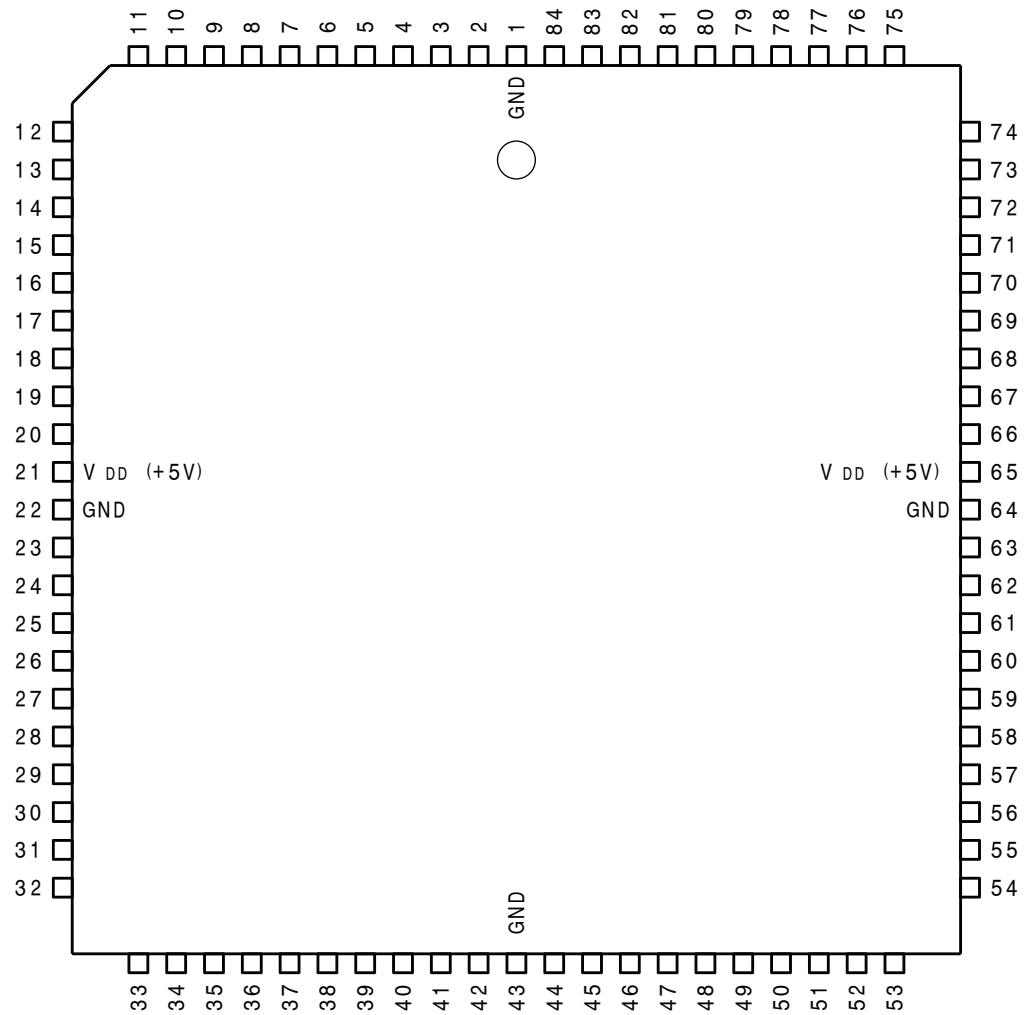
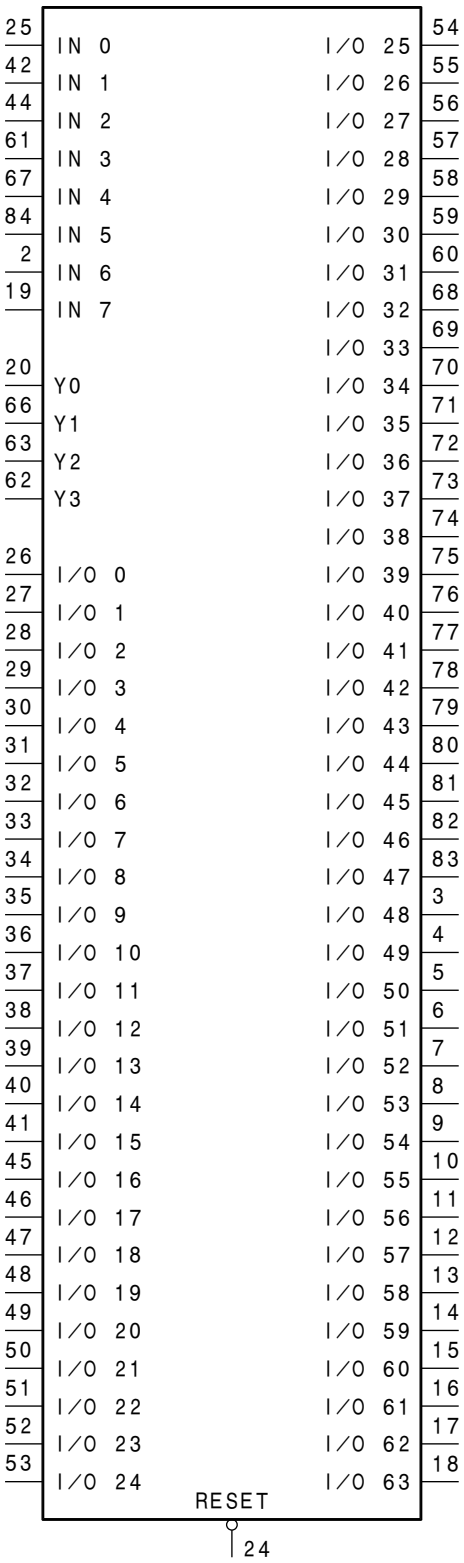
C-MOS PROGRAMMABLE LARGE SCALE INTEGRATION

-TOP VIEW-



(V_{DD} =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	-	GND	29	I/O	I/O 3	57	I/O	I/O 28
2	I	IN 6	30	I/O	I/O 4	58	I/O	I/O 29
3	I/O	I/O 48	31	I/O	I/O 5	59	I/O	I/O 30
4	I/O	I/O 49	32	I/O	I/O 6	60	I/O	I/O 31
5	I/O	I/O 50	33	I/O	I/O 7	61	I	IN 3
6	I/O	I/O 51	34	I/O	I/O 8	62	I	Y3
7	I/O	I/O 52	35	I/O	I/O 9	63	I	Y2
8	I/O	I/O 53	36	I/O	I/O 10	64	-	GND
9	I/O	I/O 54	37	I/O	I/O 11	65	-	V_{DD}
10	I/O	I/O 55	38	I/O	I/O 12	66	I	Y1
11	I/O	I/O 56	39	I/O	I/O 13	67	I	IN 4
12	I/O	I/O 57	40	I/O	I/O 14	68	I/O	I/O 32
13	I/O	I/O 58	41	I/O	I/O 15	69	I/O	I/O 33
14	I/O	I/O 59	42	I	IN 1	70	I/O	I/O 34
15	I/O	I/O 60	43	-	GND	71	I/O	I/O 35
16	I/O	I/O 61	44	I	IN 2	72	I/O	I/O 36
17	I/O	I/O 62	45	I/O	I/O 16	73	I/O	I/O 37
18	I/O	I/O 63	46	I/O	I/O 17	74	I/O	I/O 38
19	I	IN 7	47	I/O	I/O 18	75	I/O	I/O 39
20	I	Y0	48	I/O	I/O 19	76	I/O	I/O 40
21	-	V_{DD}	49	I/O	I/O 20	77	I/O	I/O 41
22	-	GND	50	I/O	I/O 21	78	I/O	I/O 42
23	-	NC	51	I/O	I/O 22	79	I/O	I/O 43
24	I	$\overline{\text{RESET}}$	52	I/O	I/O 23	80	I/O	I/O 44
25	I	IN 0	53	I/O	I/O 24	81	I/O	I/O 45
26	I/O	I/O 0	54	I/O	I/O 25	82	I/O	I/O 46
27	I/O	I/O 1	55	I/O	I/O 26	83	I/O	I/O 47
28	I/O	I/O 2	56	I/O	I/O 27	84	I	IN 5

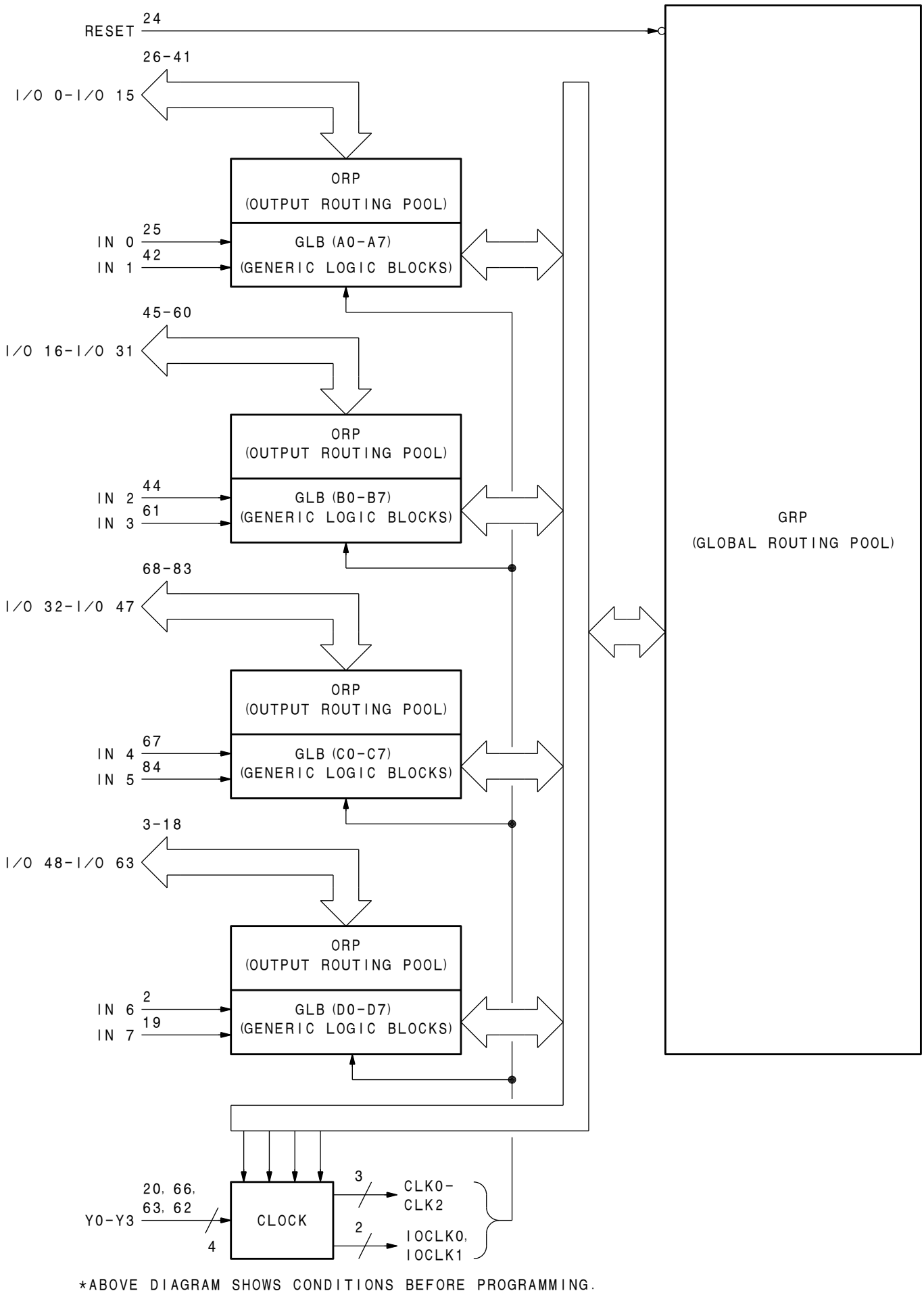


INPUT

IN 0-IN 7	;	INPUT PIN
$\overline{\text{RESET}}$	;	ACTIVE LOW (0) RESET PIN
Y0-Y3	;	INPUT CLOCK

INPUT/OUTPUT

I/O 0-I/O 63	;	INPUT/OUTPUT PIN



*ABOVE DIAGRAM SHOWS CONDITIONS BEFORE PROGRAMMING.