PIC17LC75X-16/PTL16

High-Performance 8-Bit CMOS EPROM Microcontrollers with 10-bit A/D

PIC17LC752/756A is tested for high frequency, low voltage operation - 16 MHz @ 3V

Microcontroller Core Features:

- Only 58 single word instructions to learn
- All single cycle instructions (250 ns) except for program branches and table reads/writes which are two-cycle
- Operating speed:
  - DC - 16 MHz clock input
  - DC - 250 ns instruction cycle
- 8 x 8 Single-Cycle Hardware Multiplier
- Interrupt capability
- 16 level deep hardware stack
- Direct, indirect, and relative addressing modes
- Internal/external program memory execution, Capable of addressing 64K x 16 program memory space

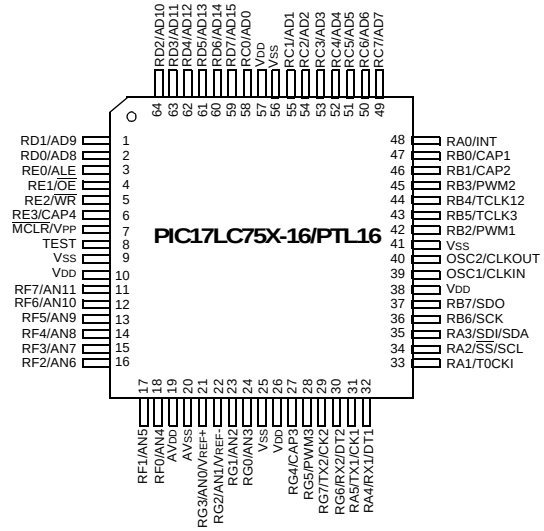
Device	Memory	
	Program (x16)	Data (x8)
PIC17LC752	8K	678
PIC17LC756A	16K	902

Peripheral Features:

- Up to 50 I/O pins with individual direction control
- 10-bit, multi-channel analog-to-digital converter
- High current sink/source for direct LED drive
- Four capture input pins
  - Captures are 16-bit, max resolution 250 ns
- Three PWM outputs (resolution is 1- to 10-bits)
- TMR0: 16-bit timer/counter with 8-bit programmable prescaler
- TMR1: 8-bit timer/counter
- TMR2: 8-bit timer/counter
- TMR3: 16-bit timer/counter
- Two Universal Synchronous Asynchronous Receiver Transmitters (USART/SCI) with Independent baud rate generators
- Master Synchronous Serial Port (MSSP) with SPI™ and I^2C™ modes (including I^2C master mode)

Pin Diagrams

64-Pin TQFP



Special Microcontroller Features:

- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Brown-out Reset
- Code-protection
- Power saving SLEEP mode
- Selectable oscillator options

CMOS Technology:

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range (3.0V to 5.5V)
- Commercial and Industrial temperature ranges
- Low-power consumption
  - < 5 mA @ 5V, 4 MHz
  - 100 µA typical @ 4.5V, 32 kHz
  - < 1 µA typical standby current @ 5V

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An errata sheet may exist for current devices, describing minor operational differences (from the data sheet) and recommended workarounds. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)
- The Microchip Corporate Literature Center; U.S. FAX: (480) 786-7277

When contacting a sales office or the literature center, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Corrections to this Data Sheet

We constantly strive to improve the quality of all our products and documentation. We have spent a great deal of time to ensure that this document is correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error, please:

- Fill out and mail in the reader response form in the back of this data sheet.
- E-mail us at webmaster@microchip.com.

We appreciate your assistance in making this a better document.

1.0 OVERVIEW

This data sheet covers the PIC17LC752-16/PTL16 and PIC17LC756A-16/PTL16 devices. The functional characteristics of these devices are identical to the PIC17LC752A/756A devices. For electrical specifications, see the electrical specifications contained within this document. For all other information about these devices, see the PIC17C7XX data sheet (DS30289).

TABLE 1-1: PIC17C7XX FAMILY OF DEVICES

Features		PIC17C752	PIC17LC752-16/PTL16	PIC17C756A	PIC17LC756A-16/PTL16	PIC17C762	PIC17C766
Maximum Frequency of Operation		33 MHz	16 MHz	33 MHz	16 MHz	33 MHz	33 MHz
Operating Voltage Range		3.0 - 5.5V	3.0 - 5.5V	3.0 - 5.5V	3.0 - 5.5V	3.0 - 5.5V	3.0 - 5.5V
Program Memory (x16)	(EPROM)	8K	8K	16K	16K	8K	16K
	(ROM)	—	—	—	—	—	—
Data Memory (bytes)		678	678	902	902	678	902
Hardware Multiplier (8 x 8)		Yes	Yes	Yes	Yes	Yes	Yes
Timer0 (16-bit + 8-bit postscaler)		Yes	Yes	Yes	Yes	Yes	Yes
Timer1 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes
Timer2 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes
Timer3 (16-bit)		Yes	Yes	Yes	Yes	Yes	Yes
Capture inputs (16-bit)		4	4	4	4	4	4
PWM outputs (up to 10-bit)		3	3	3	3	3	3
USART/SCI		2	2	2	2	2	2
A/D channels (10-bit)		12	12	12	12	16	16
SSP (SPI/I^2C w/Master mode)		Yes	Yes	Yes	Yes	Yes	Yes
Power-on Reset		Yes	Yes	Yes	Yes	Yes	Yes
Watchdog Timer		Yes	Yes	Yes	Yes	Yes	Yes
External Interrupts		Yes	Yes	Yes	Yes	Yes	Yes
Interrupt Sources		18	18	18	18	18	18
Code Protect		Yes	Yes	Yes	Yes	Yes	Yes
Brown-out Reset		Yes	Yes	Yes	Yes	Yes	Yes
In-circuit Serial Programming		Yes	Yes	Yes	Yes	Yes	Yes
I/O Pins		50	50	50	50	66	66
I/O High Current Capability	Source	25 mA	25 mA	25 mA	25 mA	25 mA	25 mA
	Sink	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)
Package Types		68-pin LCC 68-pin TQFP	64-pin TQFP	68-pin LCC 68-pin TQFP	64-pin TQFP	80-pin QFP 84-pin PLCC	80-pin QFP 84-pin PLCC

Note 1: Pins RA2 and RA3 can sink up to 60 mA.

2.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB™ IDE Software
- Assemblers/Compilers/Linkers
  - MPASM Assembler
  - MPLAB-C17 and MPLAB-C18 C Compilers
  - MPLINK/MPLIB Linker/Librarian
- Simulators
  - MPLAB-SIM Software Simulator
- Emulators
  - MPLAB-ICE Real-Time In-Circuit Emulator
  - PICMASTER®/PICMASTER-CE In-Circuit Emulator
  - ICEPIC™
- In-Circuit Debugger
  - MPLAB-ICD for PIC16F877
- Device Programmers
  - PRO MATE® II Universal Programmer
  - PICSTART® Plus Entry-Level Prototype Programmer
- Low-Cost Demonstration Boards
  - PICDEM-17

2.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a Windows®-based application which contains:

- Multiple functionality
  - editor
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
- A full featured editor
- A project manager
- Customizable tool bar and key mapping
- A status bar
- On-line help

MPLAB allows you to:

- Edit your source files (either assembly or ‘C’)
- One touch assemble (or compile) and download to PICmicro tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - object code

The ability to use MPLAB with Microchip’s simulator, MPLAB-SIM, allows a consistent platform and the ability to easily switch from the cost-effective simulator to the full featured emulator with minimal retraining.

2.2 MPASM Assembler

MPASM is a full featured universal macro assembler for all PICmicro MCU’s. It can produce absolute code directly in the form of HEX files for device programmers, or it can generate relocatable objects for MPLINK.

MPASM has a command line interface and a Windows shell and can be used as a standalone application on a Windows 3.x or greater system. MPASM generates relocatable object files, Intel standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file which contains source lines and generated machine code, and a COD file for MPLAB debugging.

MPASM features include:

- MPASM and MPLINK are integrated into MPLAB projects.
- MPASM allows user defined macros to be created for streamlined assembly.
- MPASM allows conditional assembly for multi purpose source files.
- MPASM directives allow complete control over the assembly process.

2.3 MPLAB-C17 and MPLAB-C18 C Compilers

The MPLAB-C17 and MPLAB-C18 Code Development Systems are complete ANSI ‘C’ compilers and integrated development environments for Microchip’s PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

2.4 MPLINK/MPLIB Linker/Librarian

MPLINK is a relocatable linker for MPASM and MPLAB-C17 and MPLAB-C18. It can link relocatable objects from assembly or C source files along with pre-compiled libraries using directives from a linker script.

MPLIB is a librarian for pre-compiled code to be used with MPLINK. When a routine from a library is called from another source file, only the modules that contains that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. MPLIB manages the creation and modification of library files.

MPLINK features include:

- MPLINK works with MPASM and MPLAB-C17 and MPLAB-C18.
- MPLINK allows all memory areas to be defined as sections to provide link-time flexibility.

MPLIB features include:

- MPLIB makes linking easier because single libraries can be included instead of many smaller files.
- MPLIB helps keep code maintainable by grouping related modules together.
- MPLIB commands allow libraries to be created and modules to be added, listed, replaced, deleted, or extracted.

2.5 MPLAB-SIM Software Simulator

The MPLAB-SIM Software Simulator allows code development in a PC host environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file or user-defined key press to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPLAB-C18 and MPASM. The Software Simulator offers the flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

2.6 MPLAB-ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers (MCUs). Software control of MPLAB-ICE is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, “make” and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support new PICmicro microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows 3.x/95/98 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE 2000 is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems use the same processor modules and will operate across the full operating speed range of the PICmicro MCU.

2.7 PICMASTER/PICMASTER CE

The PICMASTER system from Microchip Technology is a full-featured, professional quality emulator system. This flexible in-circuit emulator provides a high-quality, universal platform for emulating Microchip 8-bit PICmicro microcontrollers (MCUs). PICMASTER systems are sold worldwide, with a CE compliant model available for European Union (EU) countries.

2.8 ICEPIC

ICEPIC is a low-cost in-circuit emulation solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X, and PIC16CXXX families of 8-bit one-time-programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules or daughter boards. The emulator is capable of emulating without target application circuitry being present.

2.9 PRO MATE II Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable V_{DD} and V_{PP} supplies which allow it to verify programmed memory at V_{DD} min. and V_{DD} max. for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PICmicro devices. It can also set code-protect bits in this mode.

2.10 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

PICSTART Plus supports all PICmicro devices with up to 40 pins. Larger pin count devices such as the PIC16C92X, and PIC17C76X may be supported with an adapter socket. PICSTART Plus is CE compliant.

2.11 PICDEM-17

The PICDEM-17 is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756, PIC17C762, and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included, and the user may erase it and program it with the other sample programs using the PRO MATE II or PICSTART Plus device programmers and easily debug and test the sample code. In addition, PICDEM-17 supports down-loading of programs to and executing out of external FLASH memory on board. The PICDEM-17 is also usable with the MPLAB-ICE or PICMASTER emulator, and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

TABLE 2-1: DEVELOPMENT TOOLS FROM MICROCHIP

		PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	24CXX/ 25CXX/ 93CXX	HCSXXX	MCRFXXX	MCP2510
Software Tools	MPLAB™ Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	MPLAB™ C17 Compiler												✓	✓					
	MPLAB™ C18 Compiler														✓				
	MPASM/MPLINK	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Emulators	MPLAB™-ICE	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓				
	PICMASTER/PICMASTER-CE	✓	✓	✓	✓	✓		✓	✓	✓		✓	✓	✓					
	ICEPIC™ Low-Cost In-Circuit Emulator	✓		✓	✓	✓		✓	✓	✓		✓							
Debugger	MPLAB-ICD In-Circuit Debugger				✓*			✓*			✓								
Programmers	PICSTART®Plus Low-Cost Universal Dev. Kit	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓				
	PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓		✓		
Demo Boards and Eval Kits	SIMICE	✓		✓															
	PICDEM-1			✓		✓		✓†		✓			✓						
	PICDEM-2				✓†			✓†							✓				
	PICDEM-3											✓							
	PICDEM-14A		✓																
	PICDEM-17													✓					
	KEELOQ® Evaluation Kit																✓		
	KEELOQ Transponder Kit																✓		
	microID™ Programmer's Kit																	✓	
	125 kHz microID Developer's Kit																	✓	
	125 kHz Anticollision microID Developer's Kit																	✓	
	13.56 MHz Anticollision microID Developer's Kit																	✓	
	MCP2510 CAN Developer's Kit																		✓

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB-ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

3.0 PIC17LC75X-16/PTL16 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0V to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (Note 2) ..... -0.3V to +14V
Voltage on RA2 and RA3 with respect to V_{SS} ..... -0.3V to +8.5V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to V_{DD} + 0.3V
Total power dissipation (Note 1) 1.0W
Maximum current out of V_{SS} pin(s) - total (@ 70°C) ..... 500 mA
Maximum current into V_{DD} pin(s) - total (@ 70°C) ..... 500 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum output current sunk by any I/O pin (except RA2 and RA3) ..... 35 mA
Maximum output current sunk by RA2 or RA3 pins ..... 60 mA
Maximum output current sourced by any I/O pin ..... 20 mA
Maximum current sunk by PORTA and PORTB (combined) ..... 150 mA
Maximum current sourced by PORTA and PORTB (combined) ..... 100 mA
Maximum current sunk by PORTC, PORTD and PORTE (combined) ..... 150 mA
Maximum current sourced by PORTC, PORTD and PORTE (combined) ..... 100 mA
Maximum current sunk by PORTF and PORTG (combined) ..... 150 mA
Maximum current sourced by PORTF and PORTG (combined) ..... 100 mA

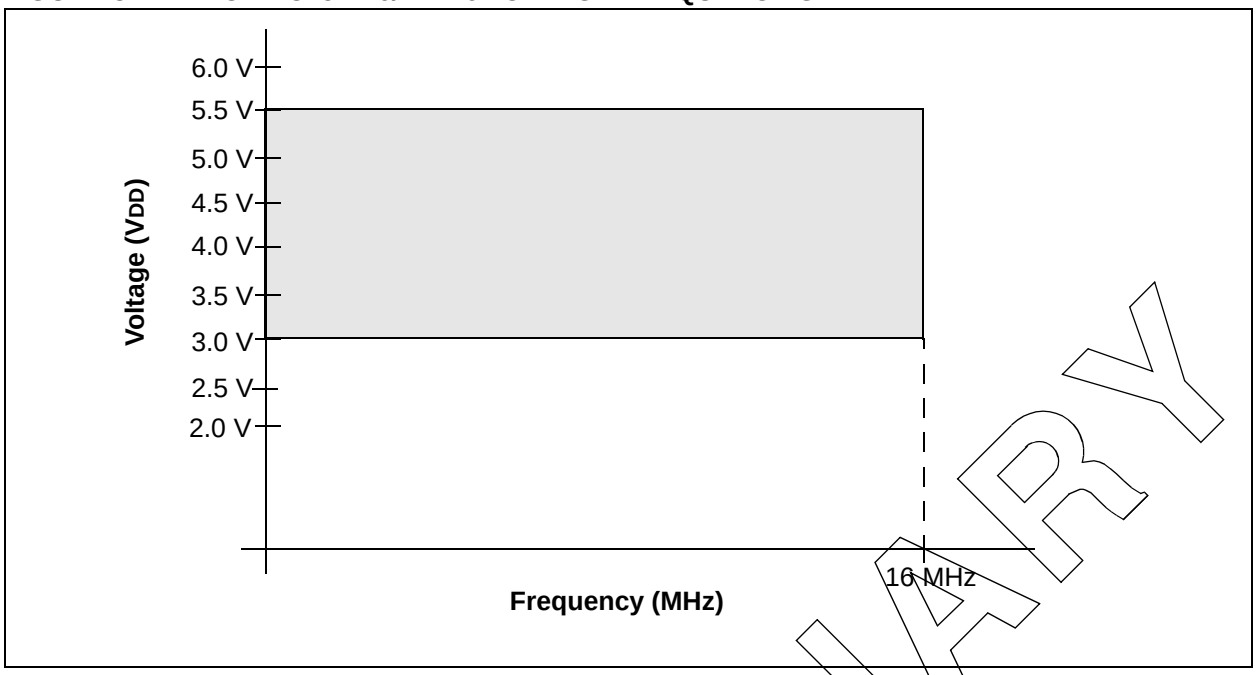
Note 1: Power dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

CAUTION: ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the PIC17LC75X-16/PTL16 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

FIGURE 3-1: PIC17LC75X-16/PTL16 VOLTAGE-FREQUENCY GRAPH



3.1 DC CHARACTERISTICS: PIC17LC75X-16/PTL16 (Commercial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	3.0	–	5.5	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	1.5 *	–	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	–	VSS	–	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure proper operation	0.010 *	–	–	V/ms	See section on Power-on Reset for details
D005	VBOR	Brown-out Reset voltage trip point	3.65	–	4.35	V	
D006	VPORTP	Power-on Reset trip point	–	2.2	–	V	VDD = VPORTP
D010 D011 D014	IDD	Supply Current (Note 2)	– – –	3 3 85	6 * 6 150	mA mA µA	FOSC = 4 MHz (Note 4) FOSC = 16 MHz, VDD = 3V FOSC = 32 kHz, (EC osc configuration)
D021	IPD	Power-down Current (Note 3)	–	< 1	5	µA	VDD = 3.0V, WDT disabled
		Module Differential Current					
D023	ΔIBOR	BOR circuitry	–	150	300	µA	VDD = 4.5V, BODEN enabled
D024	ΔIWDT	Watchdog Timer	–	10	35	µA	VDD = 5.5V
D026	ΔIAD	A/D converter	–	1	–	µA	VDD = 5.5V, A/D not converting

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT disabled.
Current consumed from the oscillator and I/O's driving external capacitive or resistive loads needs to be considered.
For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: VDD / (2 • R).
For capacitive loads, the current can be estimated (for an individual I/O pin) as (CL • VDD) • f
CL = Total capacitive load on the I/O pin; f = average frequency the I/O pin switches.
The capacitive currents are most significant when the device is configured for external execution (includes extended microcontroller mode).

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

3.2 DC CHARACTERISTICS: PIC17LC75X-16/PTL16 (Commercial)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in Section 3.1 of the PIC17C7XX Data Sheet, (DS30289)				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Input Low Voltage					
	VIL	I/O ports					
D030		with TTL buffer (Note 6)	VSS	–	0.8	V	4.5V ≤ VDD ≤ 5.5V
			VSS	–	0.2VDD	V	3.0V ≤ VDD ≤ 4.5V
D031		with Schmitt Trigger buffer					
		RA2, RA3	VSS	–	0.3VDD	V	I^2C compliant
		All others	VSS	–	0.2VDD	V	
D032		$\overline{MCLR}$, OSC1 (in EC and RC mode)	VSS	–	0.2VDD	V	Note1
D033		OSC1 (in XT, and LF mode)	–	0.5VDD	–	V	
		Input High Voltage					
	VIH	I/O ports					
D040		with TTL buffer (Note 6)	2.0	–	VDD	V	4.5V ≤ VDD ≤ 5.5V
			1 + 0.2VDD	–	VDD	V	3.0V ≤ VDD ≤ 4.5V
D041		with Schmitt Trigger buffer					
		RA2, RA3	0.7VDD	–	VDD	V	I^2C compliant
		All others	0.8VDD	–	VDD	V	
D042		$\overline{MCLR}$	0.8VDD	–	VDD	V	Note1
D043		OSC1 (XT, and LF mode)	–	0.5VDD	–	V	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15VDD *	–	–	V	
		Input Leakage Current (Notes 2, 3)					
D060	IIL	I/O ports (except RA2, RA3)	–	–	±1	µA	VSS ≤ VPIN ≤ VDD, I/O Pin (in digital mode) at hi-impedance PORTB weak pull-ups disabled
D061		$\overline{MCLR}$, TEST	–	–	±2	µA	VPIN = Vss or VPIN = VDD
D062		RA2, RA3			±2	µA	VSS ≤ VRA2, VRA3 ≤ 12V
D063		OSC1 (EC, RC modes)	–	–	±1	µA	VSS ≤ VPIN ≤ VDD
D063B		OSC1 (XT, LF modes)	–	–	VPIN	µA	RF ≥ 1 MΩ
D064		$\overline{MCLR}$, TEST	–	–	25	µA	$V_{\overline{MCLR}}$ = VPP = 12V (when not programming)
D070	IPURB	PORTB weak pull-up current	60	200	400	µA	VPIN = VSS, $\overline{RBPU}$ = 0 4.5V ≤ VDD ≤ 5.5V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17C7XX devices be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17C7XX Programming Specification (Literature number DS30274).

5: The $\overline{MCLR}$/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in Section 3.1 of the PIC17C7XX Data Sheet, (DS30289)				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Output Low Voltage					
D080	VOL	I/O ports					IOL = VDD/1.250 mA
			–	–	0.1VDD	V	4.5V ≤ VDD ≤ 5.5V
			–	–	0.1VDD *	V	VDD = 3.0V
D081		with TTL buffer	–	–	0.4	V	IOL = 6 mA, VDD = 4.5V Note 6
D082		RA2 and RA3	–	–	3.0	V	IOL = 60.0 mA, VDD = 5.5V
			–	–	0.4	V	IOL = 60.0 mA, VDD = 2.5V
			–	–	0.6	V	IOL = 60.0 mA, VDD = 4.5V
D083		OSC2/CLKOUT	–	–	0.4	V	IOL = 1 mA, VDD = 4.5V
D084		(RC and EC osc modes)	–	–	0.1VDD *	V	IOL = VDD/5 mA (PIC17LC75X-16/PTL16 only)
		Output High Voltage (Note 3)					
D090	VOH	I/O ports (except RA2 and RA3)					IOH = -VDD/2.5 mA
			0.9VDD	–	–	V	4.5V ≤ VDD ≤ 5.5V
			0.9VDD *	–	–	V	VDD = 3.0V
D091		with TTL buffer	2.4	–	–	V	IOH = -6.0 mA, VDD = 4.5V Note 6
D093		OSC2/CLKOUT	2.4	–	–	V	IOH = -5 mA, VDD = 4.5V
D094		(RC and EC osc modes)	0.9VDD *	–	–	V	IOH = -VDD/5 mA (PIC17LC75X-16/PTL16 only)
D150	VOD	**Open Drain High Voltage**	–	–	8.5	V	RA2 and RA3 pins only pulled-up to externally applied voltage
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2/CLKOUT pin	–	–	25 ‡	pF	In EC or RC osc modes when OSC2 pin is outputting CLKOUT. External clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC mode)	–	–	50 ‡	pF	
D102	CAD	System Interface Bus (PORTC, PORTD and PORTE)	–	–	50 ‡	pF	In microprocessor or extended microcontroller mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17C7XX devices be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17C7XX Programming Specification (Literature number DS30274).

5: The $\overline{MCLR}$/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +40°C Operating voltage VDD range as described in Section 3.1 of the PIC17C7XX Data Sheet, (DS30289)				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Internal Program Memory Programming Specs (Note 4)					
D110	VPP	Voltage on $\overline{MCLR}$/VPP pin	12.75	–	13.25	V	Note 5
D111	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
D112	IPP	Current into $\overline{MCLR}$/VPP pin	–	25 ‡	50 ‡	mA	
D113	IDDP	Supply current during programming	–	–	30 ‡	mA	
D114	TPROG	Programming pulse width	100	–	1000	µs	Terminated via internal/external interrupt or a reset

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17C7XX devices be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17C7XX Programming Specification (Literature number DS30274).

5: The $\overline{MCLR}$/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

Note: Internal Program Memory Programming Specs:
When using the Table Write for internal programming, the device temperature must be less than 40°C. For In-Circuit Serial Programming (ICSP™), refer to the device programming specification.

3.3 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase symbols (pp) and their meanings:

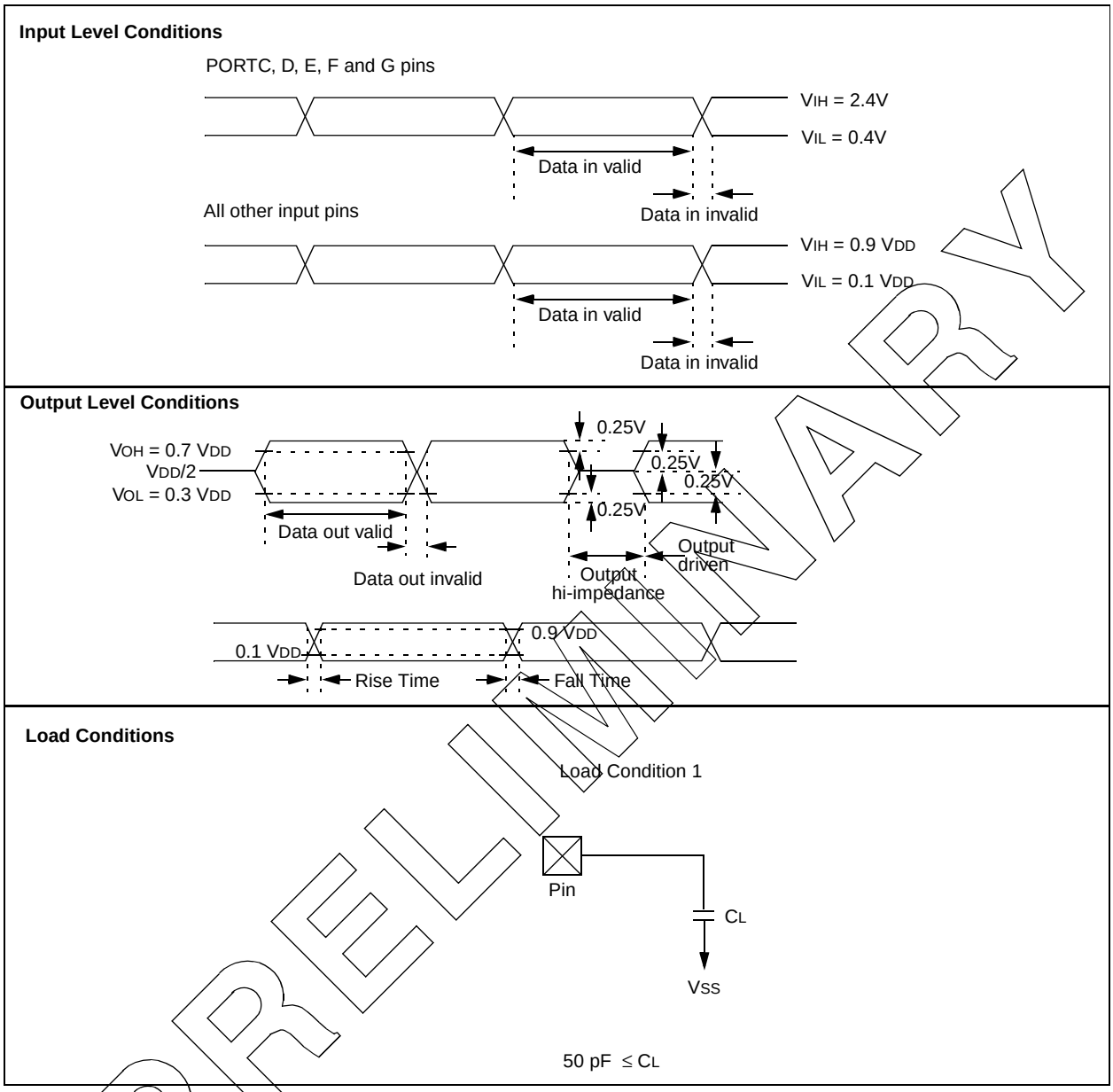
pp			
ad	Address/Data	ost	Oscillator Start-Up Timer
al	ALE	pwrt	Power-Up Timer
cc	Capture1 and Capture2	rb	PORTB
ck	CLKOUT or clock	rd	$\overline{RD}$
dt	Data in	rw	$\overline{RD}$ or $\overline{WR}$
in	INT pin	t0	T0CKI
io	I/O port	t123	TCLK12 and TCLK3
mc	$\overline{MCLR}$	wdt	Watchdog Timer
oe	$\overline{OE}$	wr	$\overline{WR}$
os	OSC1		

Uppercase symbols and their meanings:

S			
D	Driven	L	Low
E	Edge	P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance

FIGURE 3-2: PARAMETER MEASUREMENT INFORMATION

All timings are measured between high and low measurement points as indicated in the figures below.



3.4 Timing Diagrams and Specifications

FIGURE 3-3: EXTERNAL CLOCK TIMING

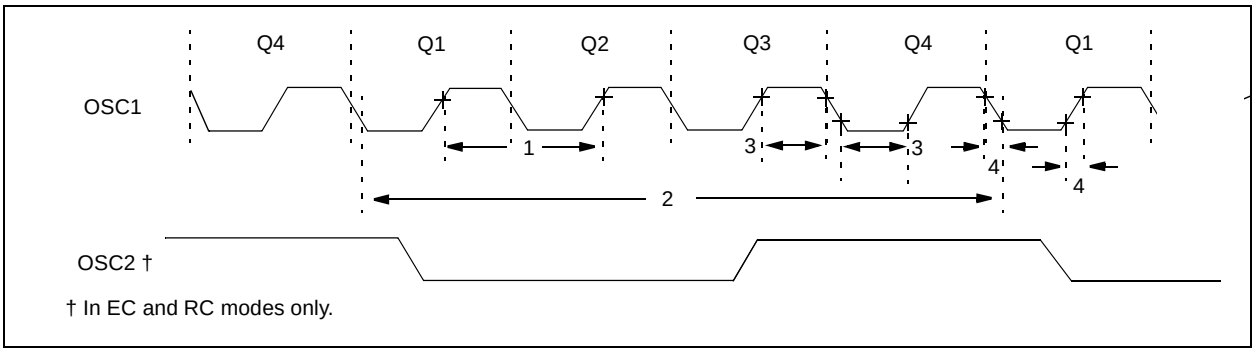


TABLE 3-1: EXTERNAL CLOCK TIMING REQUIREMENTS

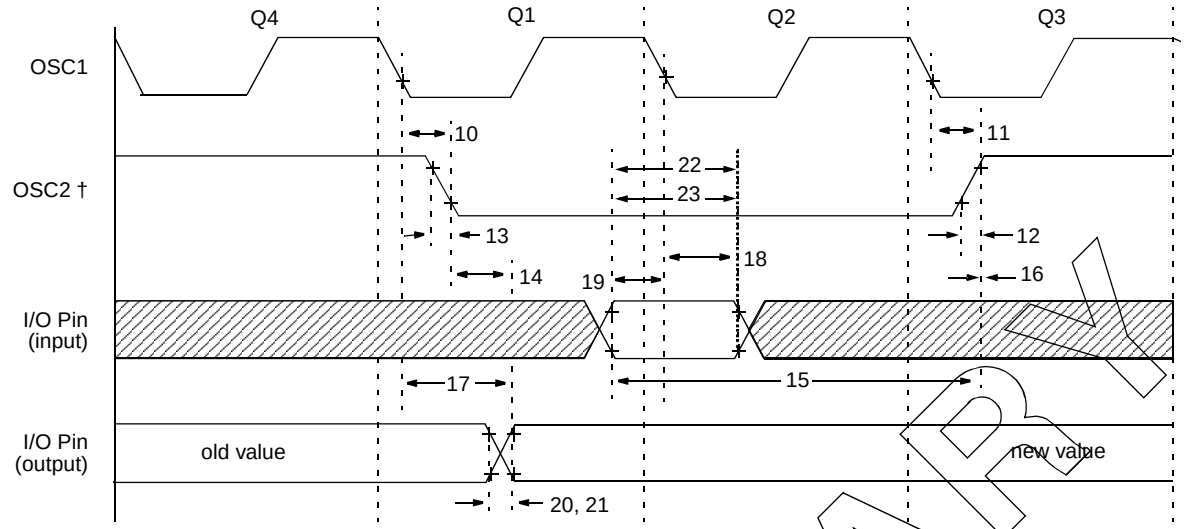
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency (Note 1)	DC	—	16	MHz	EC osc mode
		Oscillator Frequency (Note 1)	DC 2 DC	— — —	4 16 2	MHz MHz MHz	RC osc mode XT osc mode LF osc mode
1	TOSC	External CLKIN Period (Note 1)	62.5	—	—	ns	EC osc mode
		Oscillator Period (Note 1)	250 62.5 500	— — —	— 1,000 —	ns ns ns	RC osc mode XT osc mode LF osc mode
2	TCY	Instruction Cycle Time (Note 1)	121.2	4/FOSC	DC	ns	
3	TosL, TosH	Clock in (OSC1) high or low time	10 ‡	—	—	ns	EC oscillator
4	TosR, TosF	Clock in (OSC1) rise or fall time	—	—	5 ‡	ns	EC oscillator

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

FIGURE 3-4: CLKOUT AND I/O TIMING



† In EC and RC modes only.

TABLE 3-2: CLKOUT AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosL2ckL	OSC1↓ to CLKOUT↓	—	15 ‡	30 ‡	ns	Note 1
11	TosL2ckH	OSC1↓ to CLKOUT↑	—	15 ‡	30 ‡	ns	Note 1
12	TckR	CLKOUT rise time	—	5 ‡	15 ‡	ns	Note 1
13	TckF	CLKOUT fall time	—	5 ‡	15 ‡	ns	Note 1
14	TckH2ioV	CLKOUT ↑ to Port out valid	—	—	0.5TCY + 20 ‡	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT↑	0.25TCY + 25 ‡	—	—	ns	Note 1
16	TckH2ioI	Port in hold after CLKOUT↑	0 ‡	—	—	ns	Note 1
17	TosL2ioV	OSC1↓ (Q1 cycle) to Port out valid	—	—	100 ‡	ns	
18	TosL2ioI	OSC1↓ (Q2 cycle) to Port input invalid (I/O in hold time)	0 ‡	—	—	ns	
19	TioV2osL	Port input valid to OSC1↓ (I/O in setup time)	30 ‡	—	—	ns	
20	TioR	Port output rise time	—	10 ‡	35 ‡	ns	
21	TioF	Port output fall time	—	10 ‡	35 ‡	ns	
22	TinHL	INT pin high or low time	25 *	—	—	ns	
23	TrbHL	RB7:RB0 change INT high or low time	25 *	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Measurements are taken in EC Mode where CLKOUT output is 4 x TOSC.

FIGURE 3-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET TIMING

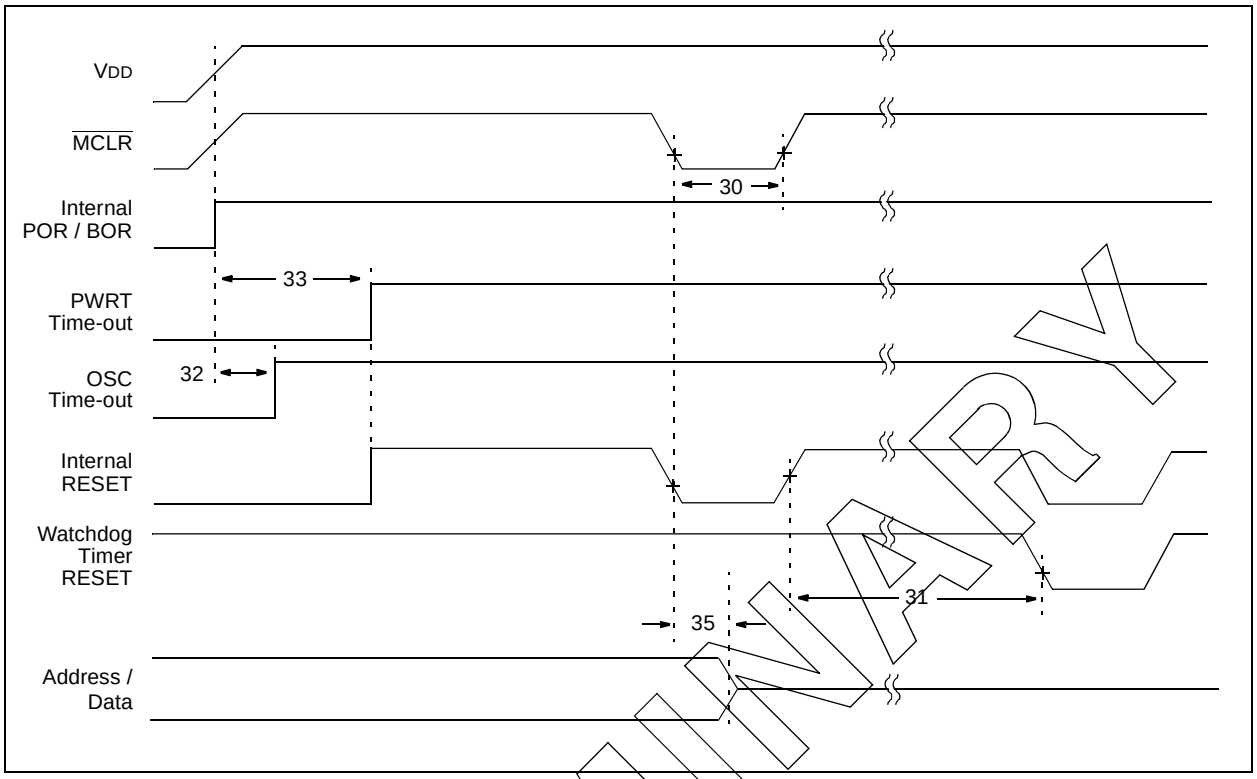


TABLE 3-3: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	100 *	—	—	ns	VDD = 5V
31	TWDT	Watchdog Timer Time-out Period (Postscale = 1)	5 *	12	25 *	ms	VDD = 5V
32	TOST	Oscillation Start-up Timer Period	—	1024TOSC§	—	ms	TOSC = OSC1 period
33	TPWRT	Power-up Timer Period	40 *	96	200 *	ms	VDD = 5V
34	TIOZ	$\overline{MCLR}$ to I/O hi-impedance	100 ‡	—	—	ns	Depends on pin load
35	TmcL2adI	$\overline{MCLR}$ to System Interface bus (AD15:AD0>) invalid	—	—	120 *	ns	
36	TBOR	Brown-out Reset Pulse Width (low)	100 *	—	—	ns	3.9V ≤ VDD ≤ 4.2V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

§ This specification ensured by design.

FIGURE 3-6: TIMER0 EXTERNAL CLOCK TIMINGS

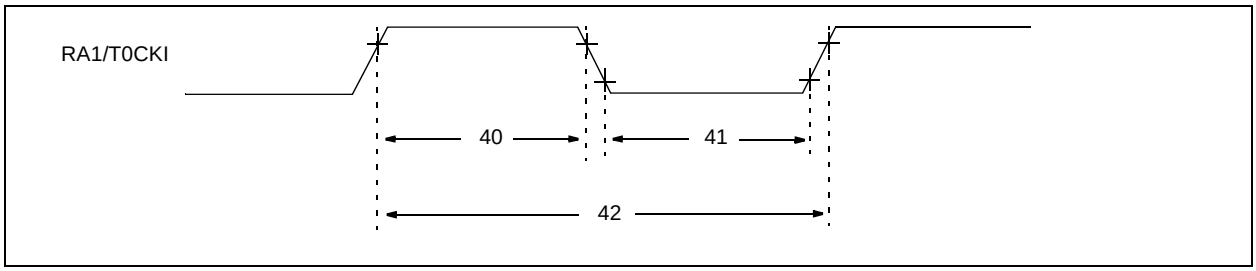


TABLE 3-4: TIMER0 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20 §	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20 §	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		GREATER OF: 20 NS OR TCY + 40 § / N	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

FIGURE 3-7: TIMER1, TIMER2, AND TIMER3 EXTERNAL CLOCK TIMINGS

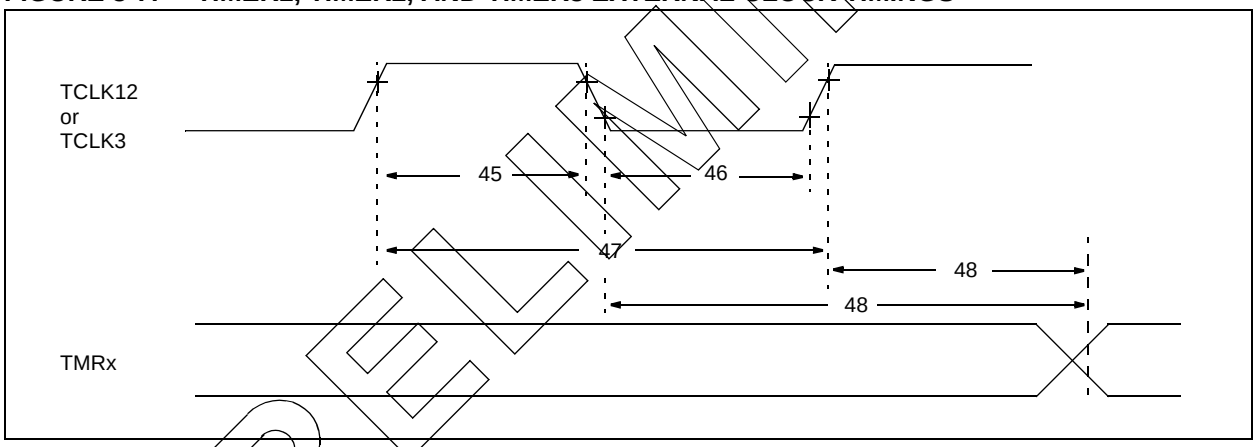


TABLE 3-5: TIMER1, TIMER2, AND TIMER3 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
45	Tt123H	TCLK12 and TCLK3 high time	0.5TCY + 20 §	—	—	ns	
46	Tt123L	TCLK12 and TCLK3 low time	0.5TCY + 20 §	—	—	ns	
47	Tt123P	TCLK12 and TCLK3 input period	TCY + 40 § / N	—	—	ns	N = prescale value (1, 2, 4, 8)
48	TckE2tmrI	Delay from selected External Clock Edge to Timer increment	2TOSC §	—	6TOSC §	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

FIGURE 3-8: CAPTURE TIMINGS

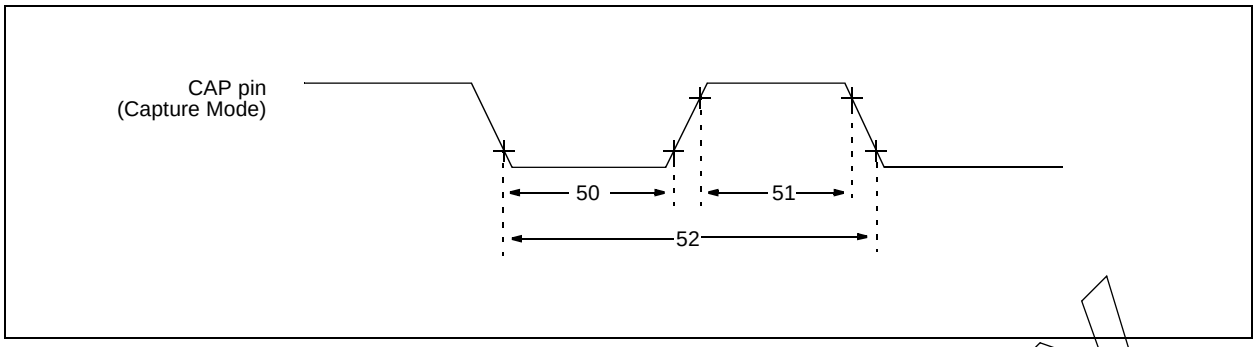


TABLE 3-6: CAPTURE REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
50	TccL	Capture pin input low time	10 *	—	—	ns	
51	TccH	Capture pin input high time	10 *	—	—	ns	
52	TccP	Capture pin input period	$\frac{2T_{CY}}{N}$ §	—	—	ns	N = prescale value (4 or 16)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

FIGURE 3-9: PWM TIMINGS

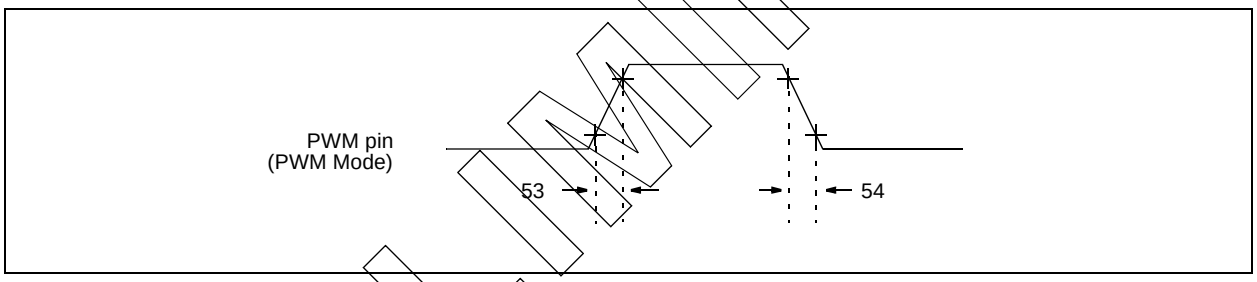


TABLE 3-7: PWM REQUIREMENTS

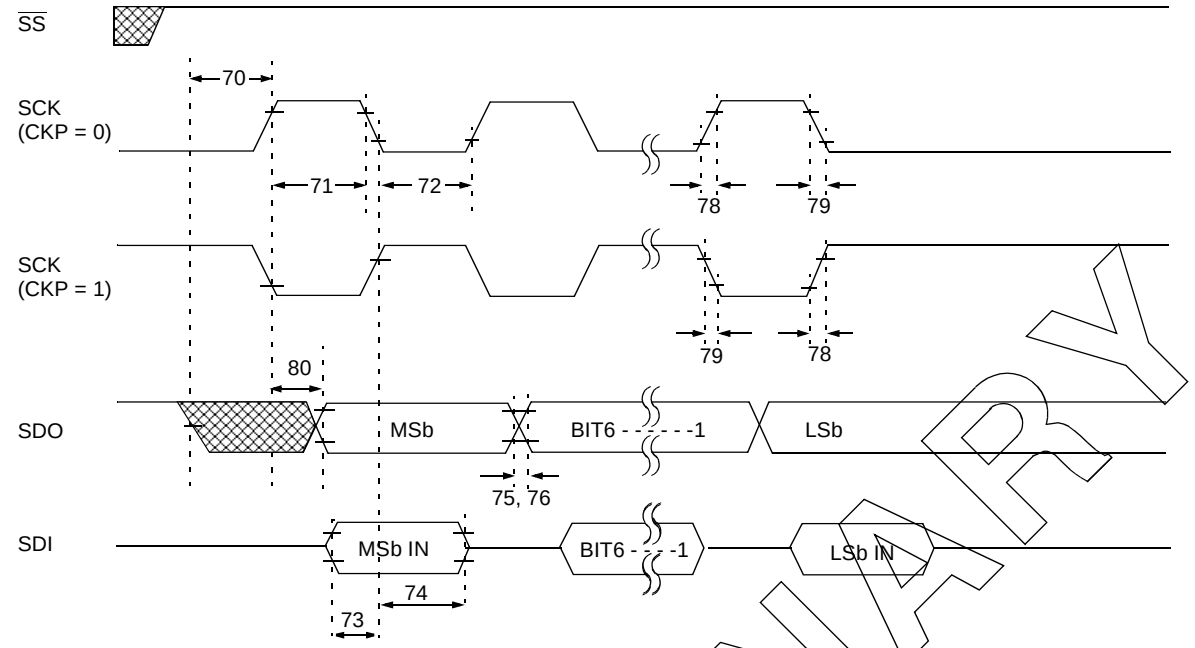
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
53	TccR	PWM pin output rise time	—	10 *	35 *	ns	
54	TccF	PWM pin output fall time	—	10 *	35 *	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

FIGURE 3-10: SPI MASTER MODE TIMING (CKE = 0)



Note: Refer to Figure 3-2 for load conditions.

TABLE 3-8: SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)

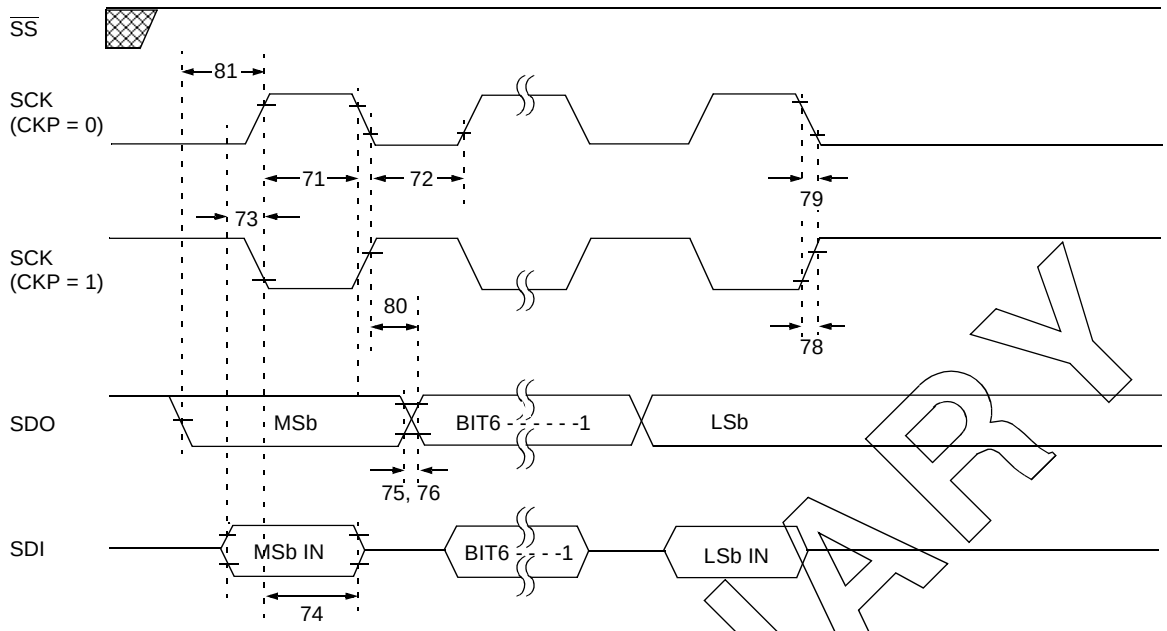
Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK↓ or SCK↑ input		TCY *	—	—	ns	
71	TscH	SCK input high time (slave mode)	Continuous	1.25TCY + 30 *	—	—	ns	
71A			Single Byte	40	—	—	ns	Note 1
72	TscL	SCK input low time (slave mode)	Continuous	1.25TCY + 30 *	—	—	ns	
72A			Single Byte	40	—	—	ns	Note 1
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100 *	—	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40 *	—	—	ns	Note 1
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100 *	—	—	ns	
75	TdoR	SDO data output rise time		—	10	25 *	ns	
76	TdoF	SDO data output fall time		—	10	25 *	ns	
78	TscR	SCK output rise time (master mode)		—	10	25 *	ns	
79	TscF	SCK output fall time (master mode)		—	10	25 *	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge		—	—	50 *	ns	

* Characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

FIGURE 3-11: SPI MASTER MODE TIMING (CKE = 1)



Note: Refer to Figure 3-2 for load conditions.

TABLE 3-9: SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

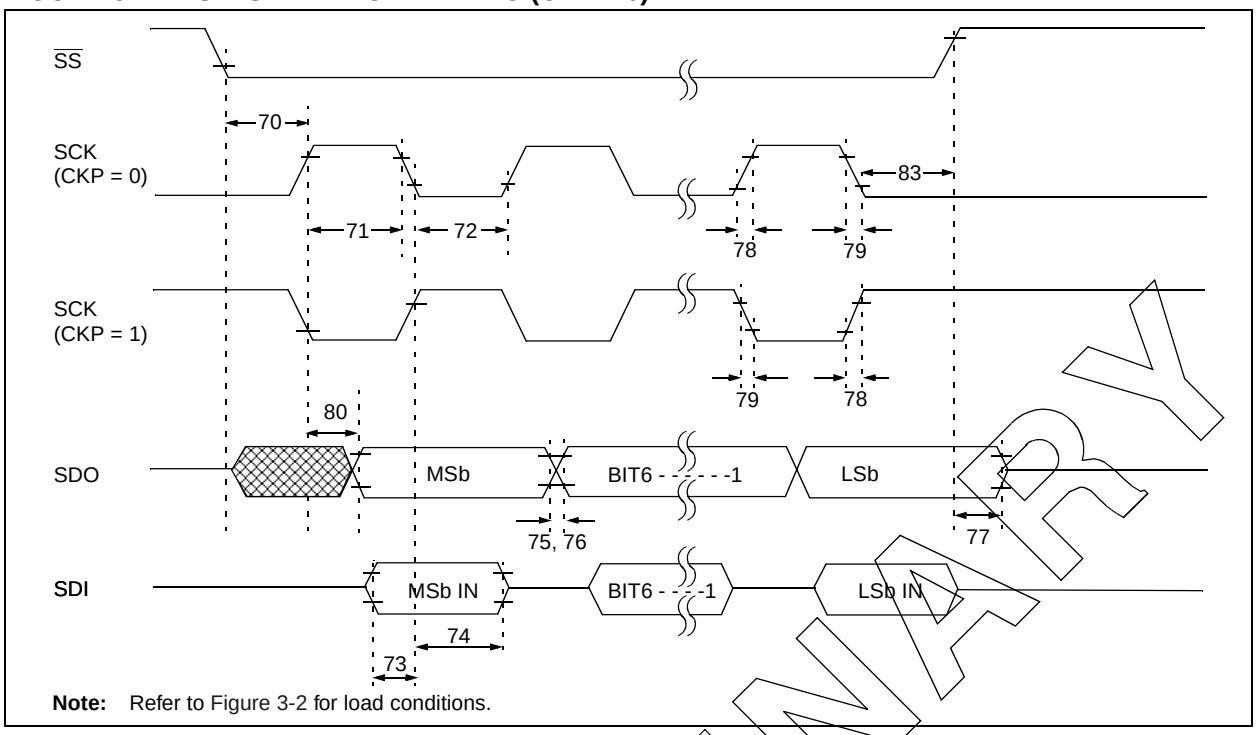
Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
71	TscH	SCK input high time (slave mode)	Continuous	1.25TCY + 30 *	—	—	ns	
71A			Single Byte	40	—	—	ns	Note 1
72	TscL	SCK input low time (slave mode)	Continuous	1.25 TCY + 30 *	—	—	ns	
72A			Single Byte	40	—	—	ns	Note 1
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100 *	—	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40 *	—	—	ns	Note 1
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100 *	—	—	ns	
75	TdoR	SDO data output rise time		—	10	25 *	ns	
76	TdoF	SDO data output fall time		—	10	25 *	ns	
78	TscR	SCK output rise time (master mode)		—	10	25 *	ns	
79	TscF	SCK output fall time (master mode)		—	10	25 *	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge		—	—	50 *	ns	
81	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge		TCY *	—	—	ns	

* Characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

FIGURE 3-12: SPI SLAVE MODE TIMING (CKE = 0)



Note: Refer to Figure 3-2 for load conditions.

TABLE 3-10: SPI MODE REQUIREMENTS (SLAVE MODE TIMING (CKE = 0)

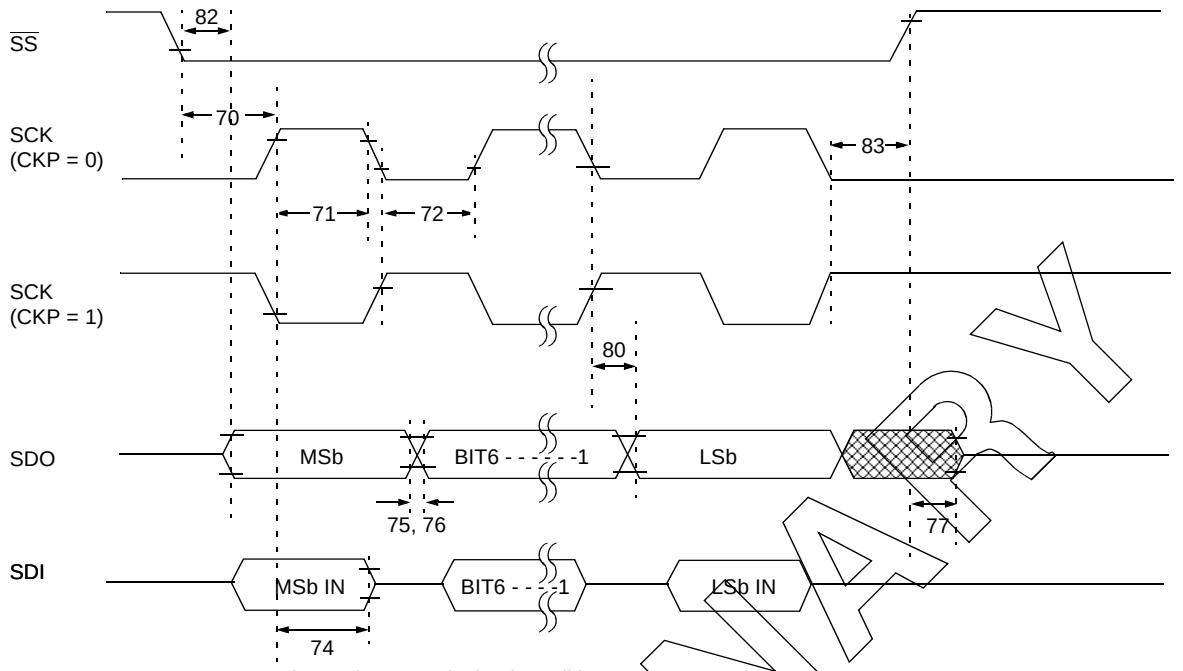
Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK↓ or SCK↑ input		TCY *	—	—	ns	
71	TscH	SCK input high time (slave mode)	Continuous	1.25TCY + 30 *	—	—	ns	
71A			Single Byte	40	—	—	ns	Note 1
72	TscL	SCK input low time (slave mode)	Continuous	1.25TCY + 30 *	—	—	ns	
72A			Single Byte	40	—	—	ns	Note 1
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100 *	—	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40 *	—	—	ns	Note 1
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100 *	—	—	ns	
75	TdoR	SDO data output rise time		—	10	25 *	ns	
76	TdoF	SDO data output fall time		—	10	25 *	ns	
77	TssH2doZ	$\overline{SS}\uparrow$ to SDO output hi-impedance		10 *	—	50 *	ns	
78	TscR	SCK output rise time (master mode)		—	10	25 *	ns	
79	TscF	SCK output fall time (master mode)		—	10	25 *	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge		—	—	50 *	ns	
83	TscH2ssH, TscL2ssH	$\overline{SS}\uparrow$ after SCK edge		1.5TCY + 40 *	—	—	ns	

* Characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

FIGURE 3-13: SPI SLAVE MODE TIMING (CKE = 1)



Note: Refer to Figure 3-2 for load conditions.

TABLE 3-11: SPI MODE REQUIREMENTS (SLAVE MODE, CKE = 1)

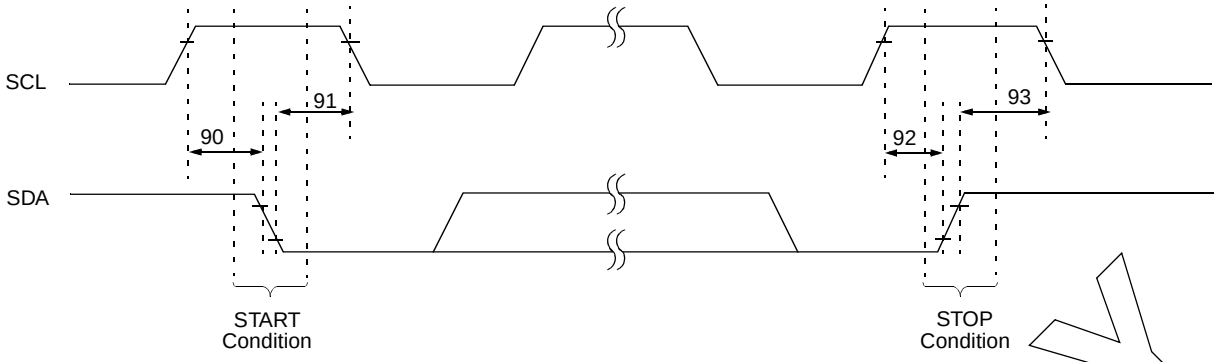
Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input		TCY *	—	—	ns	
71	TscH	SCK input high time (slave mode)	Continuous	1.25TCY + 30 *	—	—	ns	
71A			Single Byte	40	—	—	ns	Note 1
72	TscL	SCK input low time (slave mode)	Continuous	1.25TCY + 30 *	—	—	ns	
72A			Single Byte	40	—	—	ns	Note 1
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40 *	—	—	ns	Note 1
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100 *	—	—	ns	
75	TdoR	SDO data output rise time		—	10	25 *	ns	
76	TdoF	SDO data output fall time		—	10	25 *	ns	
77	TssH2doZ	SS↑ to SDO output hi-impedance		10 *	—	50 *	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge		—	—	50 *	ns	
82	TssL2doV	SDO data output valid after SS↓ edge		—	—	50 *	ns	
83	TscH2ssH, TscL2ssH	SS ↑ after SCK edge		1.5TCY + 40 *	—	—	ns	

* Characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

FIGURE 3-14: I²C BUS START/STOP BITS TIMING



Note: Refer to Figure 3-2 for load conditions.

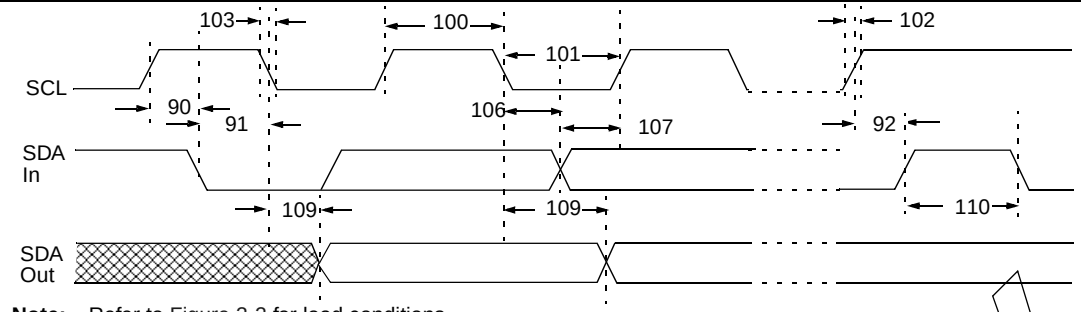
TABLE 3-12: I²C BUS START/STOP BITS REQUIREMENTS

Param. No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition Setup time	100 kHz mode	2(Tosc)(BRG + 1) §	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	2(Tosc)(BRG + 1) §	—	—		
			1 MHz mode (1)	2(Tosc)(BRG + 1) §	—	—		
91	THD:STA	START condition Hold time	100 kHz mode	2(Tosc)(BRG + 1) §	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	2(Tosc)(BRG + 1) §	—	—		
			1 MHz mode (1)	2(Tosc)(BRG + 1) §	—	—		
92	TSU:STO	STOP condition Setup time	100 kHz mode	2(Tosc)(BRG + 1) §	—	—	ns	
			400 kHz mode	2(Tosc)(BRG + 1) §	—	—		
			1 MHz mode (1)	2(Tosc)(BRG + 1) §	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	2(Tosc)(BRG + 1) §	—	—	ns	
			400 kHz mode	2(Tosc)(BRG + 1) §	—	—		
			1 MHz mode (1)	2(Tosc)(BRG + 1) §	—	—		

§ This specification ensured by design.

Note 1: Maximum pin capacitance = 10 pF for all I²C pins.

FIGURE 3-15: I^2C BUS DATA TIMING



Note: Refer to Figure 3-2 for load conditions.

TABLE 3-13: I^2C BUS DATA REQUIREMENTS

Param No.	Sym	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	2(TOSC)(BRG + 1) §	—	µs	
			400 kHz mode	2(TOSC)(BRG + 1) §	—	µs	
			1 MHz mode (1)	2(TOSC)(BRG + 1) §	—	µs	
101	TLOW	Clock low time	100 kHz mode	2(TOSC)(BRG + 1) §	—	µs	
			400 kHz mode	2(TOSC)(BRG + 1) §	—	µs	
			1 MHz mode (1)	2(TOSC)(BRG + 1) §	—	µs	
102	TR	SDA and SCL rise time	100 kHz mode	—	1000 *	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb *	300 *	ns	
			1 MHz mode (1)	—	300 *	ns	
103	TF	SDA and SCL fall time	100 kHz mode	—	300 *	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb *	300 *	ns	
			1 MHz mode (1)	—	100 *	ns	
90	TSU:STA	START condition setup time	100 kHz mode	2(TOSC)(BRG + 1) §	—	µs	Only relevant for repeated START condition
			400 kHz mode	2(TOSC)(BRG + 1) §	—	µs	
			1 MHz mode (1)	2(TOSC)(BRG + 1) §	—	µs	
91	THD:STA	START condition hold time	100 kHz mode	2(TOSC)(BRG + 1) §	—	µs	After this period the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1) §	—	µs	
			1 MHz mode (1)	2(TOSC)(BRG + 1) §	—	µs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9 *	µs	
			1 MHz mode (1)	TBD *	—	ns	
107	TSU:DAT	Data input setup time	100 kHz mode	250 *	—	ns	Note 2
			400 kHz mode	100 *	—	ns	
			1 MHz mode (1)	TBD *	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	2(TOSC)(BRG + 1) §	—	µs	
			400 kHz mode	2(TOSC)(BRG + 1) §	—	µs	
			2 MHz mode (1)	2(TOSC)(BRG + 1) §	—	µs	
109	TAA	Output valid from clock	100 kHz mode	—	3500 *	ns	
			400 kHz mode	—	1000 *	ns	
			1 MHz mode (1)	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7 ‡	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3 ‡	—	µs	
			1 MHz mode (1)	TBD *	—	µs	
D102 ‡	Cb	Bus capacitive loading		—	400 *	pF	Note 3, 4

* Characterized but not tested.

§ This specification ensured by design.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Maximum pin capacitance = 10 pF for all I^2C pins.

2: A fast-mode (400 kHz) I^2C-bus device can be used in a standard-mode I^2C-bus system, but the parameter # 107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line. PARAMETER # 102 + # 107 = 1000 + 250 = 1250 ns (for 100 kHz-mode) before the SCL line is released.

3: C_b is specified to be from 10-400pF. The minimum specifications are characterized with C_b=10pF. The rise time spec (t_r) is characterized with R_p=R_p min. The minimum fall time specification (t_f) is characterized with C_b=10pF, and R_p=R_p max. These are only valid for fast mode operation (V_{DD}=4.5-5.5V) and where the SPM bit (SSPSTAT<7>)=1.)

4: Max specifications for these parameters are valid for falling edge only. Specs are characterized with R_p=R_p min and C_b=400pF for standard mode, 200pF for fast mode, and 10pF for 1MHz mode.

FIGURE 3-16: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

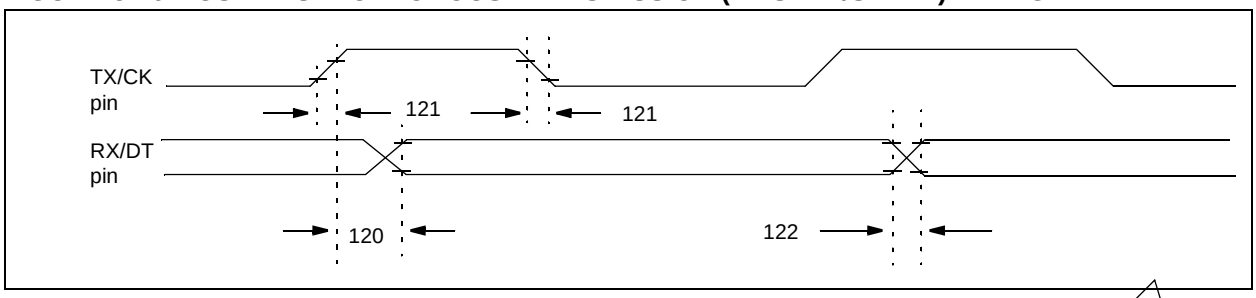


TABLE 3-14: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC17**LC**XXX	—	—	75 *	ns	
121	TckRF	Clock out rise time and fall time (Master Mode)	PIC17**LC**XXX	—	—	40 *	ns	
122	TdtRF	Data out rise time and fall time	PIC17**LC**XXX	—	—	40 *	ns	

* Characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 3-17: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

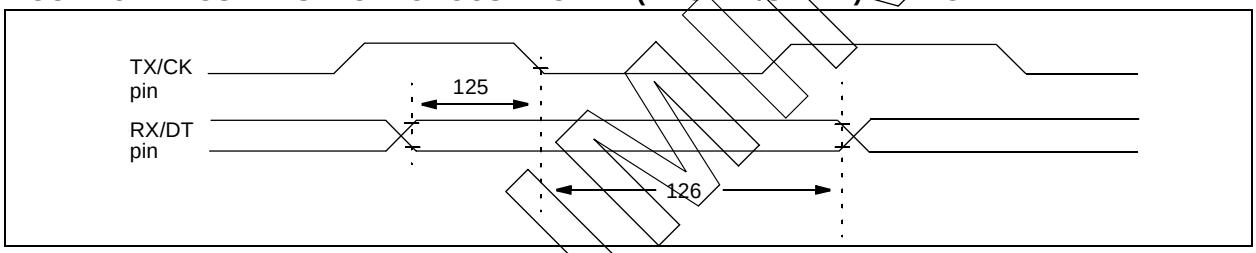


TABLE 3-15: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK↓ (DT setup time)	15	—	—	ns	
126	TckL2dtl	Data hold after CK↓ (DT hold time)	15	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 3-18: USART ASYNCHRONOUS MODE START BIT DETECT

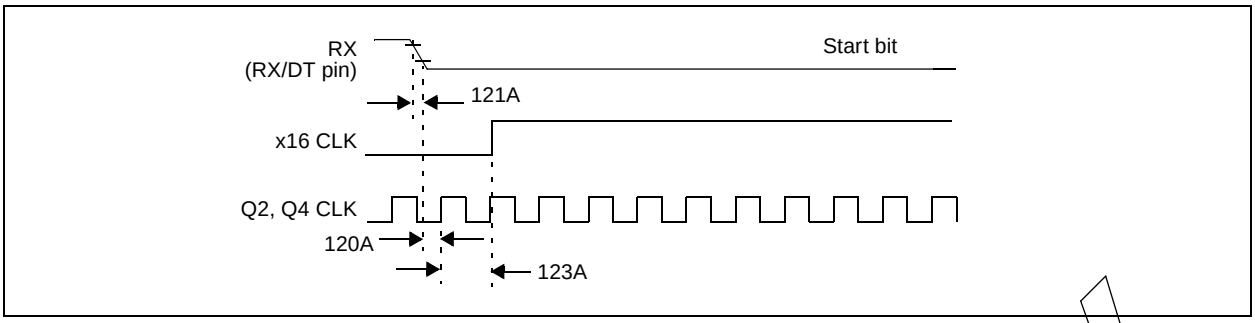


TABLE 3-16: USART ASYNCHRONOUS MODE START BIT DETECT REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120A	TdtL2ckH	Time to ensure that the RX pin is sampled low		—	—	TCY§	ns	
121A	TdtRF	Data rise time and fall time	Receive	—	—	Note 1	ns	
			Transmit	—	—	40 †	ns	
123A	TckH2bckL	Time from RX pin sampled low to first rising edge of x16 clock		—	—	TCY§	ns	

† These parameters are for design guidance only and are not tested.
§ This specification ensured by design.
Note 1: Schmitt trigger will determine logic level.

FIGURE 3-19: USART ASYNCHRONOUS RECEIVE SAMPLING WAVEFORM

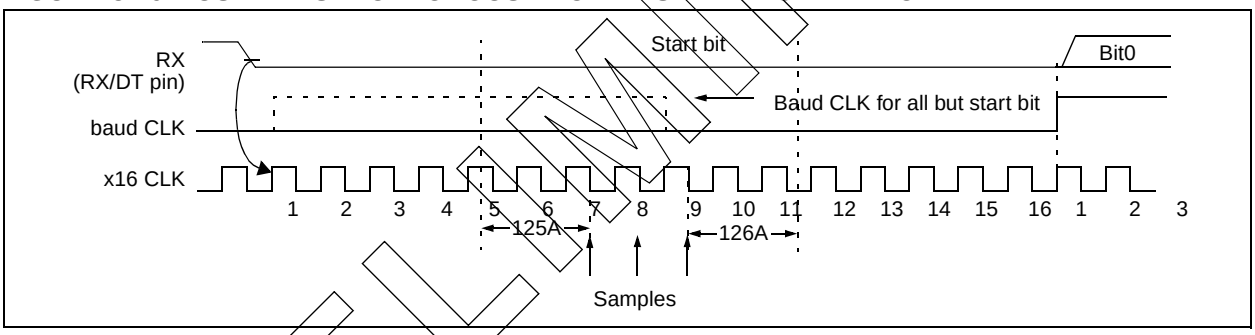


TABLE 3-17: USART ASYNCHRONOUS RECEIVE SAMPLING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125A	TdtL2ckH	Setup time of RX pin to first data sampled	TCY §	—	—	ns	
126A	TdtL2ckH	Hold time of RX pin from last data sampled	TCY §	—	—	ns	

§ This specification ensured by design.

TABLE 3-18: A/D CONVERTER CHARACTERISTICS

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	10	bit	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	10*	bit	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A02	EABS	Absolute error	—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	< ±1*	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A03	EIL	Integral linearity error	—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	< ±1*	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A04	EDL	Differential linearity error	—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	< ±1*	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A05	EFS	Full scale error	—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	< ±1*	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A06	EOFF	Offset error	—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	< ±1*	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A10	—	Monotonicity	—	guaranteed(3)	—	—	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference voltage (VREF+ — VREF-)	0V	—	—	V	VREF delta when changing voltage levels on VREF inputs.
A20A			3V *	—	—	V	Absolute minimum electrical spec. To ensure 10-bit accuracy
A21	VREF+	Reference voltage High	AVSS + 3.0V	—	AVDD + 0.3V	V	
A22	VREF-	Reference voltage Low	AVSS - 0.3V	—	AVDD - 3.0V	V	
A25	VAIN	Analog input voltage	AVSS - 0.3V	—	VREF + 0.3V	V	
A30	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
A40	IAD	A/D conversion current (VDD)	—	90	—	µA	Average current consumption when A/D is on. (Note 1)
A50	IREF	VREF input current (Note 2)	10	—	1000	µA	During VAIN acquisition. Based on differential of VHOLD to VAIN.
			—	—	10	µA	During A/D conversion cycle

* These parameters are characterized but not tested.

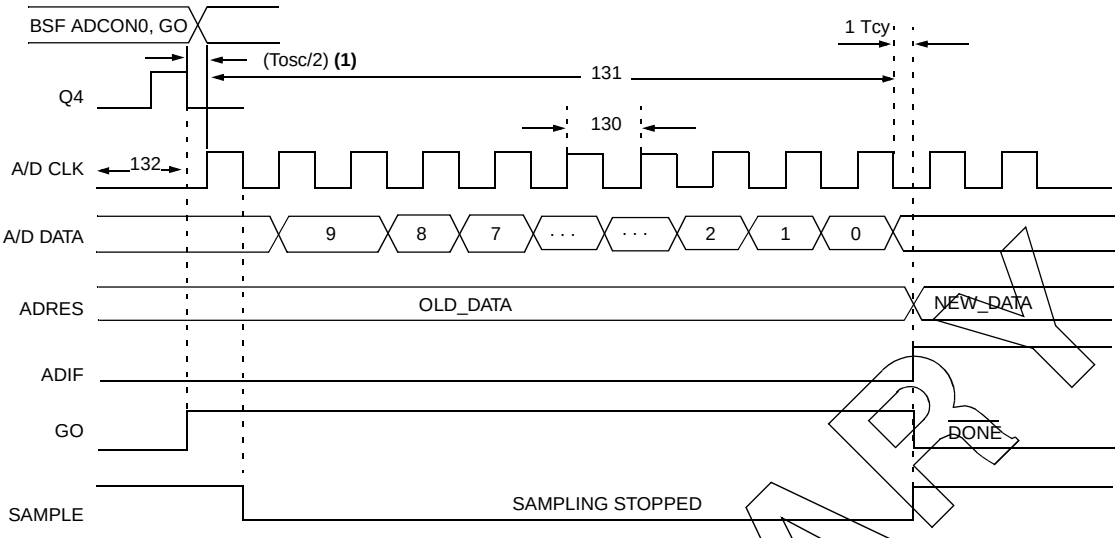
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RG0 and RG1 pins or AVDD and AVSS pins, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the Input Voltage and has no missing codes.

FIGURE 3-20: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 3-19: A/D CONVERSION REQUIREMENTS

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	3.0	—	—	µs	TOSC based, VREF full range
			3.0 *	6.0	9.0 *	µs	A/D RC Mode
131	TCNV	Conversion time (not including acquisition time) (Note 1)	11 §	—	12 §	TAD	
132	TACQ	Acquisition time	(Note 2)	20	—	µs	
			10 *	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e. 5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to ADCLK start	—	Tosc/2 §	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

§ This specification ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 16.1 of the PIC17C7XX Data Sheet (DS30289) for minimum conditions when input voltage has changed more than 1 LSb.

FIGURE 3-21: MEMORY INTERFACE WRITE TIMING

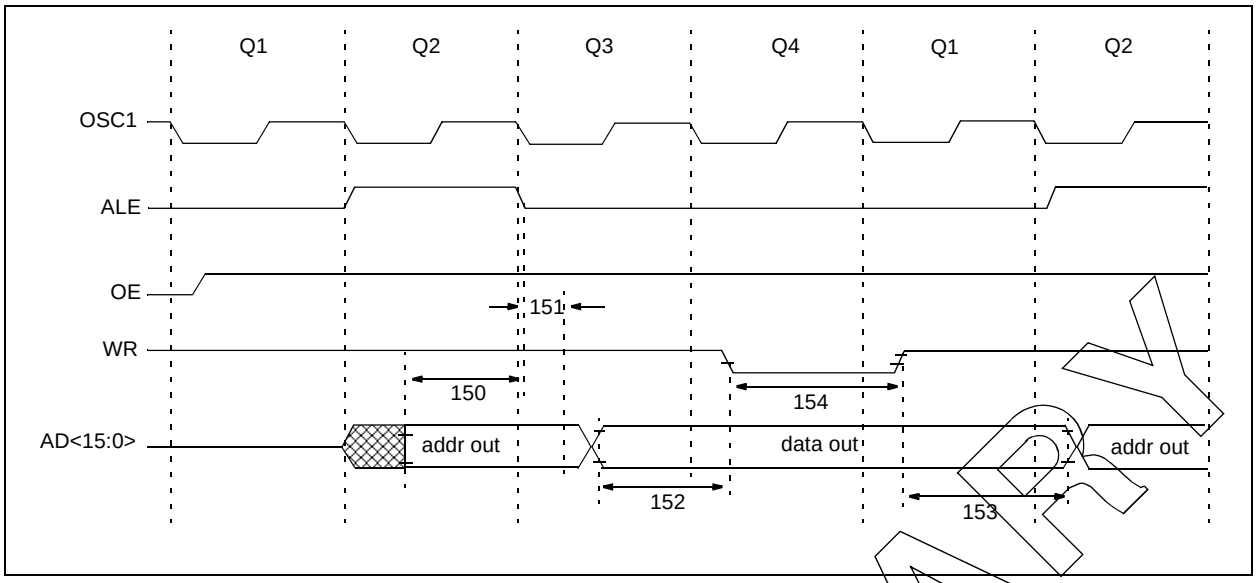


TABLE 3-20: MEMORY INTERFACE WRITE REQUIREMENTS

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
150	TadV2alL	AD<15:0> (address) valid to ALE↓ (address setup time)	0.25TCY - 10*	—	—	ns	
151	TalL2adI	ALE↓ to address out invalid(address hold time)	0*	—	—	ns	
152	TadV2wrL	(data setup time)	0.25TCY - 40*	—	—	ns	
153	TwrH2adI	$\overline{WR}$↑ to data out invalid(data hold time)	—	0.25TCY§	—	ns	
154	TwrL	$\overline{WR}$ pulse width	—	0.25TCY§	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

FIGURE 3-22: MEMORY INTERFACE READ TIMING

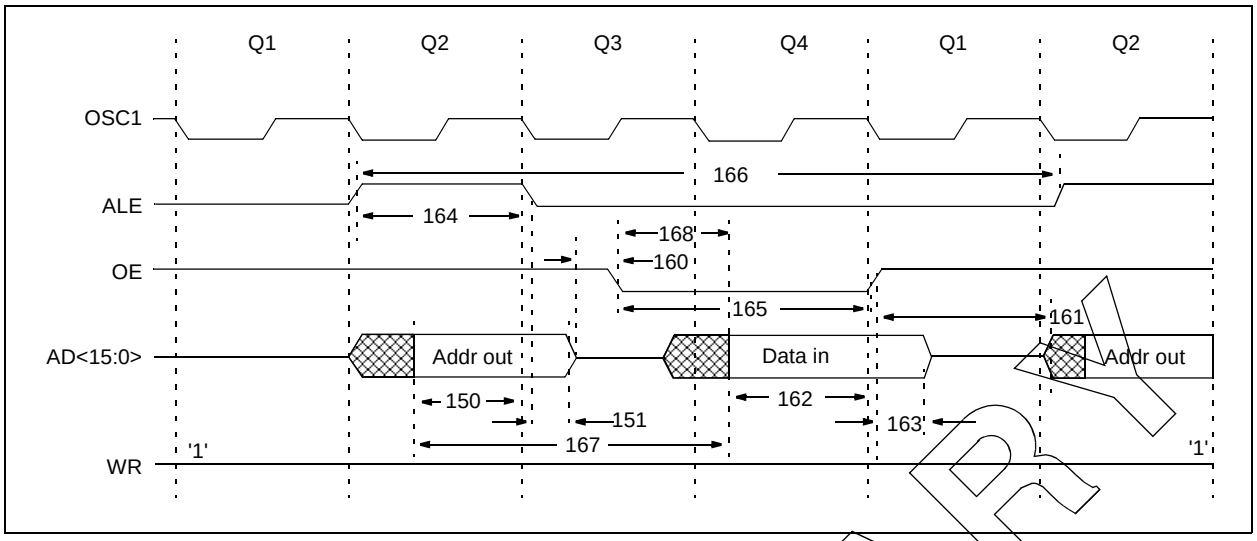


TABLE 3-21: MEMORY INTERFACE READ REQUIREMENTS

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Condi-tions
150	TadV2alL	AD15:AD0 (address) valid to ALE↓ (address setup time)	0.25TCY - 10*	—	—	ns	
151	TalL2adI	ALE↓ to address out invalid(address hold time)	5*	—	—	ns	
160	TadZ2oeL	AD15:AD0 hi-impedance to $\overline{OE}$↓	0*	—	—	ns	
161	ToeH2adD	$\overline{OE}$↑ to AD15:AD0 driven	0.25TCY - 15*	—	—	ns	
162	TadV2oeH	Data in valid before $\overline{OE}$↑ (data setup time)	45*	—	—	ns	
163	ToeH2adI	$\overline{OE}$↑to data in invalid (data hold time)	0*	—	—	ns	
164	TalH	ALE pulse width	—	0.25TCY §	—	ns	
165	ToeL	$\overline{OE}$ pulse width	0.5TCY - 35 §	—	—	ns	
166	TalH2alH	ALE↑ to ALE↑(cycle time)	—	TCY §	—	ns	
167	Tacc	Address access time	—	—	0.75TCY - 45*	ns	
168	Toe	Output enable access time($\overline{OE}$ low to Data Valid)	—	—	0.5TCY - 75*	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

NOTES:

4.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

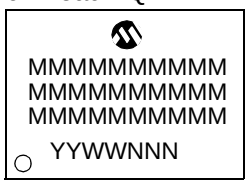
Please refer to the PIC17C7XX Data Sheet (DS30289) for the most current graphs and tables.

NOTES:

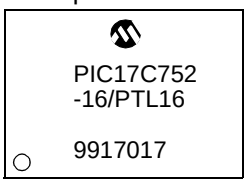
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

64-Lead TQFP



Example

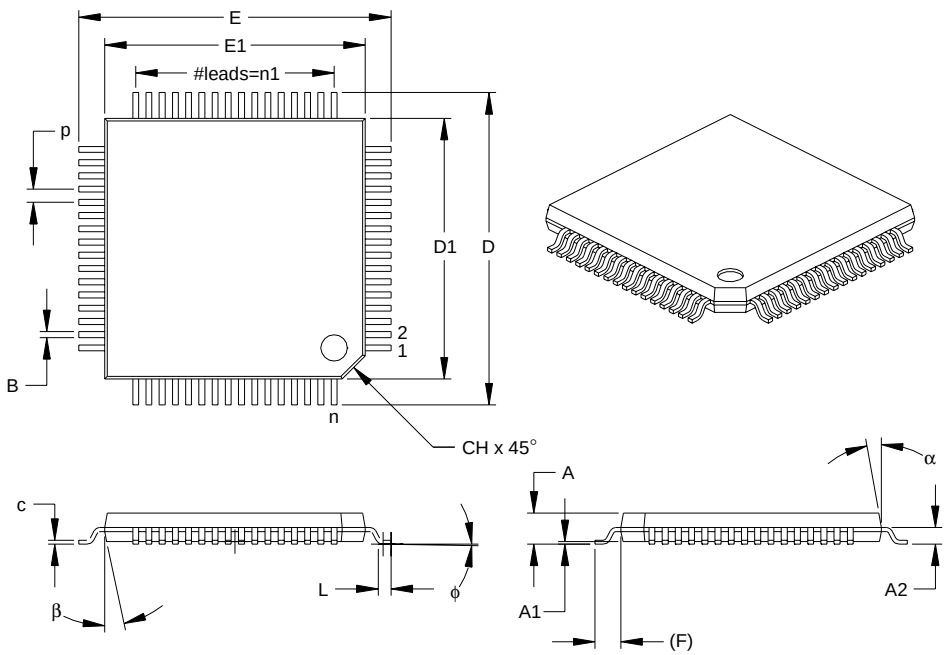


Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		64			64	
Pitch	p		.020			0.50	
Pins per Side	n1		16			16	
Overall Height	A	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff	A1	.002	.006	.010	0.05	0.15	0.25
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	(F)		.039			1.00	
Foot Angle	φ	0	3.5	7	0	3.5	7
Overall Width	E	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	c	.005	.007	.009	0.13	0.18	0.23
Lead Width	B	.007	.009	.011	0.17	0.22	0.27
Pin 1 Corner Chamfer	CH	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

*Controlling Parameter

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.

JEDEC Equivalent: MS-026

Drawing No. C04-085

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NOTES:

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

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ftp://ftp.microchip.com

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
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The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits.The Hot Line Numbers are:

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To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

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Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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