GEC PLESSEY SEMICONDUCTORS

OCTOBER 1996

DS3707 - 4.2

PDSP16116/A

16 BY 16 BIT COMPLEX MULTIPLIER

(Supersedes version October 1995 verison, DS3707 - 3.0)

The PDSP16116A will multiply two complex (16 + 16) bit words every 50ns and can be configured to output the complete complex (32 + 32) bit result within a single cycle. The data format is fractional two's complement.

The PDSP16116/A contains four 16 x 16 Array Multipliers, two 32 bit Adder/Subtractors and all the control logic required to support Block Floating Point Arithmetic as used in FFT applications. In combination with a PDSP16318, the PDSP16116A forms a two chip 10MHz Complex Multiplier Accumulator with 20 bit accumulator registers and output shifters. The PDSP16116 in combination with two PDSP16318s and two PDSP1601s forms a complete 10MHz Radix 2 DIT FFT Butterfly solution which fully supports Block Floating Point Arithmetic. The PDSP16116/A has an extremely high throughput that is suited to recursive algorithms as all calculations are performed with a single pipeline delay (two cycle fall-through).

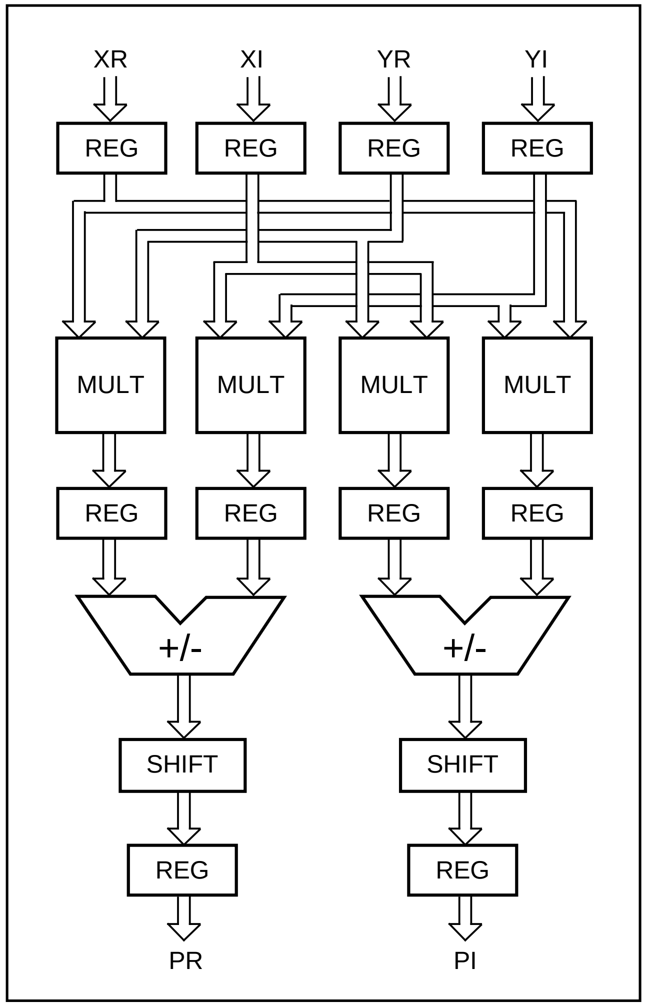


Fig.1 Simplified Block Diagram

FEATURES

- Complex Number (16 + 16) X (16 + 16) Multiplication
- Full 32 bit Result
- 20MHz Clock Rate
- Block Floating Point FFT Butterfly Support
- -1 times -1 Trap
- Two's Complement Fractional Arithmetic
- TTL Compatible I/O
- Complex Conjugation
- 2 Cycle Fall Through
- 144 pin PGA or QFP packages

APPLICATION

- Fast Fourier Transforms
- Digital Filtering
- Radar and Sonar Processing
- Instrumentation
- Image Processing

ASSOCIATED PRODUCTS

PDSP16318/A	Complex Accumulator
PDSP16112/A	(16 + 16) X (12 + 12) Complex Multiplier
PDSP16330/A	Pythagoras Processor
PDSP1601/A	ALU and Barrel Shifter
PDSP16350	Precision Digital Modulator
PDSP16256	Programmable FIR Filter
PDSP16510	Single Chip FFT Processor

The PDSP16116 has a number of features tailored for System applications.

-1 x -1 Trap

In multiply operations utilising Twos Complement Fractional notation, the -1 x -1 operation forms an invalid result as +1 is not representable in the fractional number range. The PDSP16116/A eliminates this problem by trapping the -1 x -1 operation and forcing the Multiplier result to become the most positive representable number.

Complex Conjugation

Many algorithms utilising complex arithmetic require conjugation of complex data stream. This operation has traditionally required an adiditional ALU to multiply the imaginary component by -1. The PDSP16116 eliminates the requirement for the extra ALU by offering on chip complex conjugation of either of the two incoming complex data words with no loss in throughput.

Easy Interfacing

As with all PDSP family members the PDSP16116 has registered I/O for data and control. Data inputs have independent clock enables and data outputs have independent three state output enables.

Signal	Type	Description	Normal mode Configuration
XR15:0	INPUT	16 bit input for real x data	
XI15:0	INPUT	16 bit input for imag x data	
YR15:0	INPUT	16 bit input for reaal y data	
YI15:0	INPUT	16 bit input for imag y data	
PR15:0	OUTPUT	16 bit output for real p data	
PI15:0	OUTPUT	16 bit output for img p data	
CLK	INPUT	Clock, new data is loaded on rising edge of CLK	
CEX	INPUT	Clock, enable X-port input register	
CEY	INPUT	Clock, enable Y-port input register	
CONX	INPUT	Conjugate X data	
CONY	INPUT	Conjugate Y data	
ROUND	INPUT	Rounds the real & imag results	
MBFP	INPUT	Mode select (BFP/Normal)	Tie Low
SOBFP	INPUT	Start of BFP operations **	Tie Low
EOPSS	INPUT	End of pass **	Tie Low
AR15:13	INPUT	3 MSB's from real part of A-word **	Tie Low
AI15:13	INPUT	3 MSB's from imag part of A-word **	Tie Low
WTA1:0	INPUT	Word tag from A-word	Tie Low
WTB1:0	INPUT	Word tag from B-word / shift control *	
WTOUT1:0	OUTPUT	Word tag output **	
SFTA1:0	OUTPUT	Shift control for A-word / overflow flag *	
SFTR2:0	OUTPUT	Shift control for accumulator resul **	
GWR4:0	OUTPUT	Global weighting register contents **	
OSEL1:0	INPUT	Selects the desired output configuration	
OER, OEI	INPUT	Output enables	
VDD	POWER	+5V Supply All supply pins	
GND	POWER	0V Supply must be connected	

* Indicates pin performs different functions in BFP / Normal modes.
** Indicates pin is used only in BFP mode

Table.1 Signal Descriptions

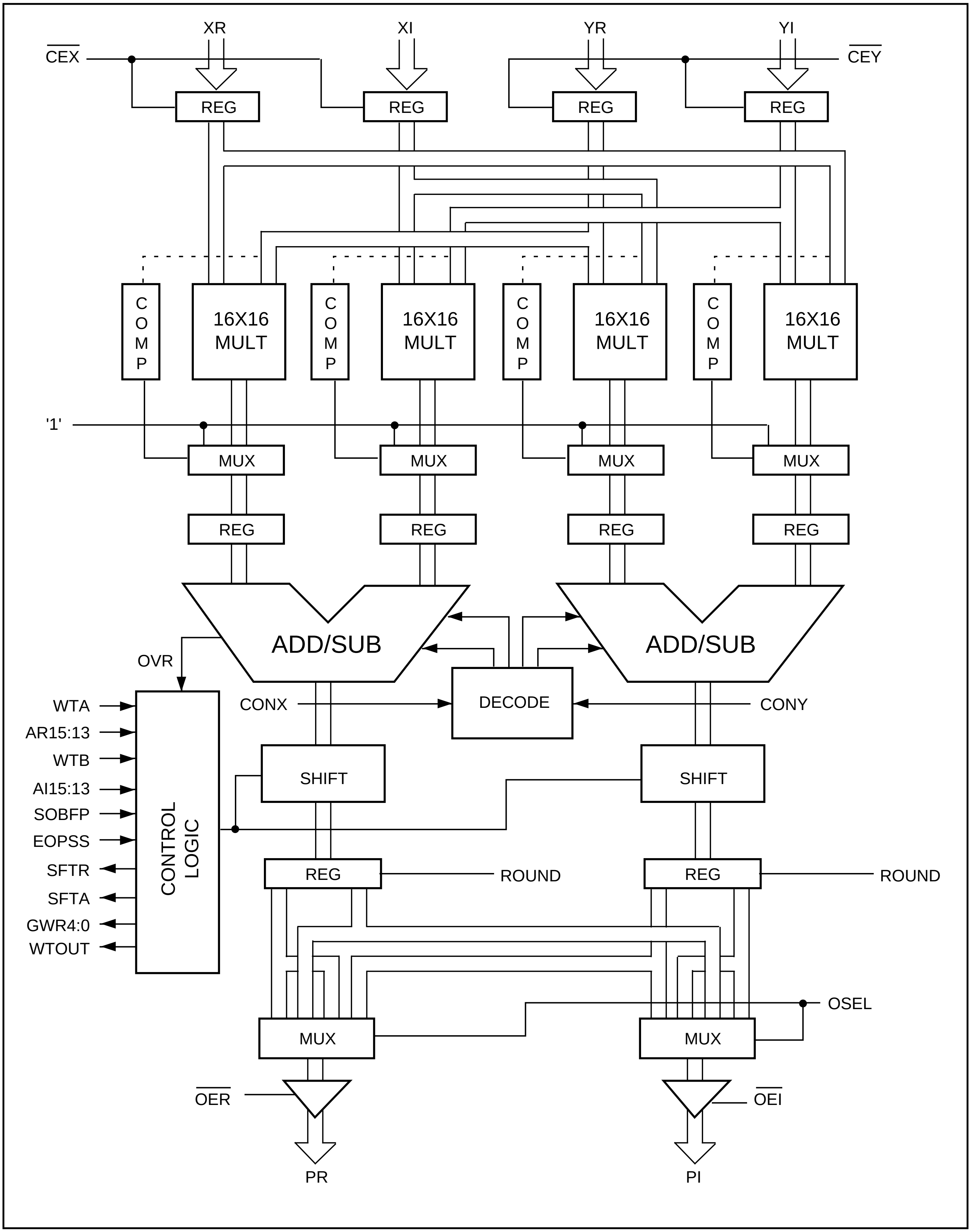


Fig.2 Block Diagram

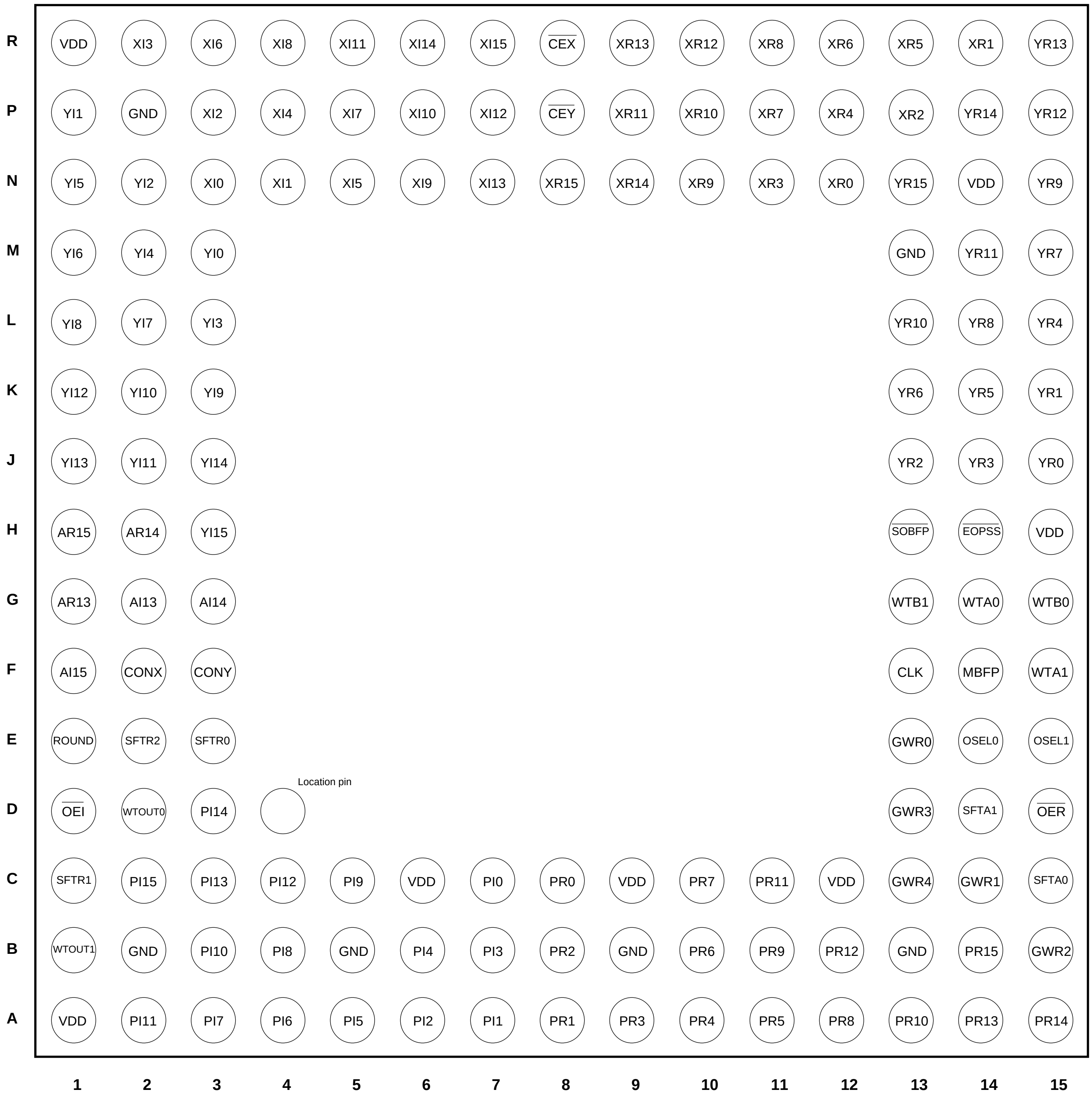


Fig.3 Pin Allocation Diagram (Bottom View)
144 pin PGA - AC144

GG	SIG	GG	SIG	GG	SIG	GG	SIG
1	PI14	37	XI1	73	GND	109	VDD
2	PI15	38	XI2	74	VDD	110	GND
3	WTOUT1	39	XI3	75	YR12	111	PR13
4	WTOUT0	40	XI4	76	YR11	112	PR12
5	SFTR0	41	XI5	77	YR10	113	PR11
6	SFTR1	42	XI6	78	YR9	114	PR10
7	SFTR2	43	XI7	79	YR8	115	PR9
8	OEI	44	XI8	80	YR7	116	PR8
9	CONX	45	XI9	81	YR6	117	PR7
10	CONY	46	XI10	82	YR5	118	PR6
11	ROUND	47	XI11	83	YR4	119	PR5
12	AI13	48	XI12	84	YR3	120	GND
13	AI14	49	XI13	85	YR2	121	VDD
14	AI15	50	XI14	86	YR1	122	PR4
15	AR13	51	XI15	87	YR0	123	PR3
16	AR14	52	CEY	88	EOPSS	124	PR2
17	AR15	53	CEX	89	VDD	125	PR1
18	YI15	54	XR15	90	SOBFP	126	PR0
19	YI14	55	XR14	91	WTB1	127	PI0
20	YI13	56	XR13	92	WTB0	128	PI1
21	YI12	57	XR12	93	WTA1	129	PI2
22	YI11	58	XR11	94	WTA0	130	PI3
23	YI10	59	XR10	95	MBFP	131	PI4
24	YI9	60	XR9	96	CLK	132	VDD
25	YI8	61	XR8	97	OSEL1	133	PI5
26	YI7	62	XR7	98	OSEL0	134	GND
27	YI6	63	XR6	99	OER	135	PI6
28	YI5	64	XR5	100	SFTA0	136	PI7
29	YI4	65	XR4	101	SFTA1	137	PI8
30	YI3	66	XR3	102	GWR0	138	PI9
31	YI2	67	XR2	103	GWR1	139	PI10
32	YI1	68	XR1	104	GWR2	140	PI11
33	YI0	69	XR0	105	GWR3	141	PI12
34	XI0	70	YR15	106	GWR4	142	PI13
35	GND	71	YR14	107	PR15	143	GND
36	VDD	72	YR13	108	PR14	144	VDD

All GND and VDD pins must be used.

Fig.3A Pin Allocation Diagram - 144 pin ceramic QFP - GG144

NORMAL MODE OPERATION

When the MBFP mode select input is held low the 'Normal' mode of operation is selected. This mode supports all Complex Multiply operations that do not require Block Floating Point arithmetic.

Multiplier Stage

Complex two's complement fractional data is loaded into the X and Y input registers via the X and Y Ports on the rising edge of CLK. The Real and Imaginary components of the fractional data are each assumed to have the following format

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Where S = sign bit which has an effective weighting -2^{0}

The value of the 16 bit two's complement word is

Value = $(-1xS)+(bit14x2^{-1})+(bit13x2^{-2})+(bit12x2^{-3})$. . .

The X & Y port registers are individually enabled by the CEX & CEY signals respectvely. If the registers are required to be permanently enabled, then these signals may be tied to ground. On each clock cycle the contents of the input registers are passed to the four multipliers to start a new Complex Multiply operation. Each Complex Multiply operation requires four partial products (Xr x Yr), (Xr x Yi), (Xi x Yr), (Xi x Yi), all of which are calculated in parallel by the four 16 x 16 Multipliers. Only one clock cycle is required to complete the multiply stage before the Mutliplier results are loaded into the Multiplier output registers for passing on to the Adder/ Subtractors in the next cycle. Each multiplier produces a 31 bit result with the duplicate sign bit eliminated. The format of the output data from the Multipliers is

BIT NUMBER	30	29	28	27	26	25	24	. . .	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	. . .	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

The effective weighting of the sign bit is -2^{0}

Result Correction

Due to the nature of the fraction twos complement representation it is possible to represent -1 exactly but not 1. With conventional multipliers this causes a problem when -1 is multiplied by -1 as the multiplier produces an incorrect result. The PDSP16116 includes a trap to ensure that the most positive number (value = 1.2^{-30}), (hex = 7FFFFFFF) is subsituted for the incorrect result. The multiplier result is therefore always a (correct) fractional value.

Complex Conjugation

Either the X or Y input data may be complex conjugated by asserting the CONX or CONY signals respectively. Asserting either of these signals has the effect of inverting (multiplying by -1) the imaginary component of the respective input. Table 3 shows the effect of CONX and CONY on the X and Y inputs.

FUNCTION	OPERATION	CONX	CONY
X x Y	(XR+XI)x(YR+YI)	low	low
X x Conj Y	(XR+XI)x(YR-YI)	high	low
Conj X x Y	(XR-XI)x(YR+YI)	low	high
Invalid	Invalid	high	high

Table 3 Conjugate Functions

Adder / Subtractor Stage

The 31 bit Real and Imaginary results from the Multipliers are passed to two 32 bit Adder/Subtractors. The Adder calculates the imaginary result ((Xr x Yi) + (Xi x Yr)) and the Subtractor calculates the Real result ((Xr x Yr) = (Xi x Yi)). Each Adder/Subtractor produces a 32 bit result with the following format.

BIT NUMBER	31	30	29	28	27	26	. . .	8	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	. . .	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

The effective weighting of the sign bit is -2^{1}

Rounding

The ROUND control when asserted rounds the most significant 16 bits of the full 32 bit result from the shifter. If the ROUND signal is active (High), then bit 16 is set to a one, rounding the most significant 16 bits of the shifted result. (The least siginificant 16 bits are unaffected). Inserting a one ensures that the rounding error is never greater than 1LSB, and that no DC bias is introduced as a result of the rounding processes.

The format of the Rounded result is;

BIT NUMBER	31	30	29	28	27	. . .	18	17	16	15	14	13	. . .	2	1	0
WEIGHTING	S	2^{0}	2^{-1}	2^{-2}	2^{-3}	. . .	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{16}	2^{-17}	. . .	2^{-28}	2^{-29}	2^{-30}
	← ROUNDED VALUE								→	← LBS's						→

The effective weighting of the sign is -2^{1}

Shifter

Each of the two Adder/Subtractors are followed by Shifters controlled via the WTB control input. These shifters can each apply two different shifts, however the same shift is applied to both real and imaginary components. The two shift options are:

i) WTB1:0 = 11 Shift complex product one place to the left.

The effective weighting of the sign bit is -2^{0}

ii) WTB1:0 = 00, 01 or 10 Shift complex product three place to the right. The effective weighting of the sign bit is -2^{4}.

Overflow

If the left shift option is selected and the Adder/Subtractor contain a 32 bit word, then an invalid result will be passed to the output. An invalid output arising from this combination of events will be flagged by the SFTA0 flag output. The SFTA0 Flag will go high if either the real or imaginary reslut is invalid.

Output Select

The output from the Shifters is passed to the Output Select Mux, which is controlled via the OSEL inputs. These inputs are not registered and hence allow the output combination to be changed within each cycle. The full complex 64 bit result from the multiplier may therefore be output within a single cycle. The OSEL control selects four different output combinations as as summarised in Table 4.

OSEL1	OSEL0	PR	PI
0	0	MSR	MSI
0	1	LSR	LSI
1	0	MSR	LSR
1	1	MSI	LSI

Table 3 Output Selection

(Where MSR and LSR are the most and least siginificant 16 bit words of the Real Shifter output, MSI and LSI are the most and least significant 16 bit words of the imaginary Shifter output).

The output select options allow two different modes for extracting the full 32 bit result from the PDSP16116. The first mode treats the two 16 bit outputs as real and imaginary ports allowing the real and imaginary results to be output in two halves on the real and imaginary output ports. The second mode treats the two 16 bit outputs as one 32 bit output and allows the real and imaginary results to be output as 32 bit words.

PIN DESCRIPTIONS

XR, XI, YR, YI

Data inputs 16 bits: Data is loaded into the input registers from these ports on the rising edge of CLK. The data format is Twos Complement Fractional, where the MSB (sign bit) is bit 15. In normal mode the weighting of the MSB is -20 ie -1.

PR, PI

Data outputs 16 bits: Data is clocked into the output registers and passed to the PR and PI outputs on the rising edge of CLK. The data format is Twos Complement Fractional. The field of the internal result selected for output via PR and PI is controlled by signals OSEL1:0 (see Table 4).

CLK

Common Clock to all internal register.

CEX, CEY

Clock enables for X and Y input ports: When low these inputs enable the CLK signal to the X or Y input registers allowing new data to be clocked into the Multiplier.

CONX, CONY

If either of these inputs are high on the rising edge of CLK, then the data in the associated input has its imaginary component inverted (multiplied by -1), see Table 3. CONX and CONY affect data input on the same clock rising edge.

ROUND

The ROUND control is used to round the most siginficant 16 bits of the output register. The rounding operation takes place one cycle after the ROUND input is taken high. The ROUND input is not latched and is intended to be tied high or low depending upon the application.

MBFP

Mode select: When high, Block Floating Point (BFP) mode is selected. This allows the device to maintain the dynamic range of the data using a series of word tags. This is especially useful in FFT appllications. When low, the chip operates in normal mode for more general applications. This pin is intended to be tied high or low, depending on application.

SOBFP (BFP MODE ONLY)

Start of BFP: This input should be held low for the first cycle of the first pass of the BFP calculations (see Fig.7). It serves to reset the internal registers associated with BFP control. When operating in normal mode this input should be tied low.

EOPSS (BFP MODE ONLY)

End of pass: This input should be held low for the last cycle of each pass and for the lay time between passes. It instructs the control logic to update the value of the global weighting register and prepare the BFP circuitry for the next pass. When operating in normal mode this input should be tied low.

AR15:13 (BFP MODE ONLY)

Three Msbs of the real part of the A-word : These are used in the FFT butterfly application to deteremine the magnitude of the real part of the A-word and, hence, to determine if there will be any chage of word growth in the PDSP16318 Complex Accumulator. When operating in normal mode, these inputs are not used and may be tied low.

AI15:13 (BFP MODE ONLY)

Three Msbs of the imaginary part of the A-word : used in the same fashion as AR.

SFTR2:0 (BFP MODE ONLY)

Accumulator result shift control. These pins should be linked directly to the S2:0 pins on the PDSP16318 Complex Accumulator. They control the accumulator's barrel shifter (see Table 5). The purpose of this shift is to minimise sign extension in the multiplier or accumulator ALU's. When operating in normal mode, these output are superfluous.

SFTR2:0	FUNCTION
0 0 0	Reserved
0 0 1	Reserved
0 1 0	Reserved
0 1 1	Shift right by one
1 0 0	No shift
1 0 1	Shift left by one
1 1 0	Shift left by two
1 1 1	Reserved

Table 5 Auccumulator Shifts (BFP mode)

GWR4:0 (BFP MODE ONLY)

Contents of the global weighting register: This stores the weighting of the largest word present with respect to the weighting of the original input words. Hence, if the contents of the GWR are 00010, this indicates that the largest word currently being processed has its binary point two bits to the right of the original data at the start of the BFP calculations. The contents of this register are updated at the end of each pass, according to the largest value of WTOUT occuring during that pass. (i.e. If WTOUT = 11, then GWR will be increased by 2). The GWR is presented in two's complement format. These outputs are superfluous in normal mode.

WTOUT1:0 (BFP MODE ONLY)

Word tag output. This tag records the weighting of the output words from the current cycle relative to the current global weighting register (see Table 6). It should be stored along with the A' and B' words as it will form the input word tags, WTA and WTB, for each complex word during the next pass. These outputs are superfluous in normal mode.

WTOUT1:0	Weighting of the output relative to the current global weighting register
0 0	One less
0 1	The same
1 0	One more
1 1	Two more

Table 6 Word Tag Weightings

WTA1:0 (BFP MODE ONLY)

Word tag from the A-word. This word records the weighting of the A-word relative to the global weighting register on the previous pass. Although the A-word inself is not processed in the PDSP16116, this information is required by the control logic for the radix-2 butterfly FFT application. These inputs should be tied low in normal mode.

WTB1:0 (BFP & NORMAL MODES)

In BFP mode, this is the word tag from the B-word. This is operated in the same manner as WTA but for the B-word. The value of the word tags are used to ensure that the binary weighting of the A word and the product of the complex multiplier are the same at the inputs to the complex accumulator. Depending on which word is the larger, the weighting adjustment is performed using either the internal shifter or an external shifter controlled by SFTA. The word tags are also used to maintain the weighting of the final result to within plus two and minus one binary points relative to the new GWR. (On the first pass all word tags will be ignored).

In normal mode, these inputs perform a different function. They directly control the internal shifter at the output port as shown in Table 7.

WTB1:0	FUNCTION
11	shift complex product one place to the left
00 01 10	shift complex product three places to the right

Table 7 Normal Mode Shift Control

SFTA1:0 (BFP & NORMAL MODES)

In BFP mode, these signals act as as the A-word shift control. They allow shifting from one to four places to the right, see Table 8. Depending on the relative weightings of the A-words and the complex product, the A-word may have to be shifted to the right to ensure compatible weightings at the inputs to the PDSP16318 complex accumulator. (The two words must have the same weighting if they are to be added).

In normal mode, SFTA0 performs a different a different function. If WTB1:0 is set to implement a left shift, then overflow will occur if the data is fully 32 bits wide. This pin is used to flag such an overflow. SFTA1 is not used in normal mode.

WTB1:0	FUNCTION
0 0	Shift A-word 1 places to the right
0 1	Shift A-word 2 places to the right
1 0	Shift A-word 3 places to the right
1 1	Shift A-word 4 places to the right

Table 8 External A-word shift control

OSEL1:0

The outputs from the device are selected by the OSEL0 & OSEL1 instruction bits. These controls allow selection of the output combination during the current cycle. (They are not registered). These are four possible output configurations that allow either complex outputs of the most or least significant bytes, or real or imaginary outputs of the full 32 bit word (see Table 4). OSEL0 and OSEL1 should both be tied low when in BFP mode.

BFP MODE FFT APPLICATION

The PDSP16116 may be used as the main arithmetic unit of the butterfly processor which will allow the following FFT benchmarks:

1024 point complex radix-2 transform in 517us
512 point complex radix-2 transform in 235us
256 point complex radix-2 transform in 106us

In addition, with pin MBFP tied high, the BFP circuitry within the PDSP16116 can be used to adaptively rescale data throughout the course of the FFT so as to give high-resolution results.

The BFP system on the PDSP16116 can be used with any variation of the Radix-2 Decimation-In-Time FFT - e.g. the Constant Geometry algorithm, the In-Place algorithm etc. An N-point Radix-2 DIT FFT is split into log (N) passes. Each pass consists of N/2 'butterflies', each performing the operation:

A' = A + B.W
B' = A - B.W

Where W is the complex coefficient and A & B are the complex data.

Fig.4 illustrates how a single PDSP16116 may be combined with two PDSP1601's and two PDSP16318's to form a complete BFP butterfly processor. The PDSP16318's are used to perform the complex addition and subtraction of the butterfly operation, while the PDSP1601's are used to match the data path of the A-word to the pipelining and shifting operations within the PDSP16116.

For more information on the theory and construction of this butterfly processor, refer to application note AN59.

BFP MODE OPERATION

The BFP mode on the PDSP16116 is intended for use in the FFT application described above. i.e. it is intended to prevent data degredation during the course of an FFT calculation. The operation of the PDSP16116 based BFP butterfly processor (see Fig.4) is described below.

The Block Floating Point System

A block floating point system is essentially an ordinary integer arithmetic system with some clever logic bolted on. The object of the extra logic is to lend the system some of the enormous dynamic range afforded by a true floating point system without suffering the corresponding loss in performance.

The initial data used by the FFT should all have the same binary arithmetic weighting. i.e. the binary point should occupy the same position in every data word, as is normal in integer arithmetic. However, during the course of the FFT, a variety of weightings are used in the data words to increase the dynamic range available. This situation is similar to that within a true floating point system, though the range of numbers representable is more limited. In the BFP system used in the PDSP16116, there are, within any one pass of the FFT, four possible positions of the binary point wihin the integer words. To record the position of its binary point, each word has a 2-bit word tag associated with it. By way of example, in a particular pass we may have the following four positions of binary point avaiable, each denoted by a certain value of word tag:

XX.XXXXXXXXXXXX	word tag = 00
XXX.XXXXXXXXXXX	word tag = 01
XXXX.XXXXXXXXXX	word tag = 10
XXXXX.XXXXXXXXX	word tag = 11

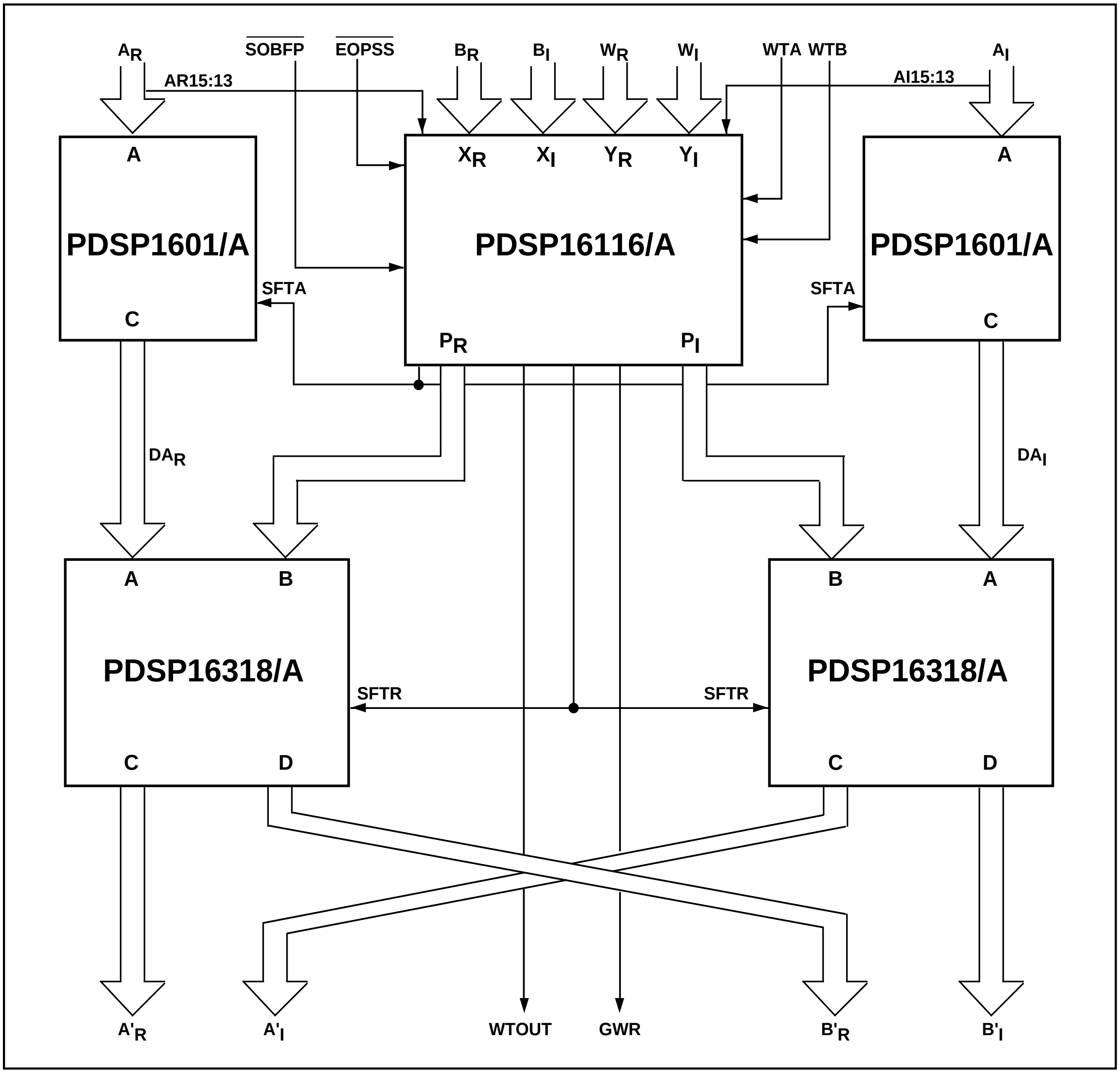


Fig.4 FFT Butterfly Processor

At the end of each constituent pass of the FFT, the positions of the binary point supported may change to reflect the trend of data increase or decreases in magnitude. Hence, in the pass following that of the above example, the four positions of binary point supported may be change to:

XX.XXXXXXXXXXXX	word tag = 00
XXX.XXXXXXXXXXX	word tag = 01
XXXX.XXXXXXXXXX	word tag = 10
XXXXX.XXXXXXXXX	word tag = 11

This variation in the range of binary points supported from pass to pass (i.e. the movement of the binary point relative to its position in the original data) is recorded in the GWR.

Thus we can determine the position of the binary point relative to its initial position by modifying the value of GWR by WTOUT for a given word as shown in Table 6.

As an example, if GWR=01001 and WTOUT=10 then the binary point has moved 10 places to the right of its original position.

The butterfly operation

The butterfly operation is the arithmetic operation which is repeated many times to produce an FFT. The PDSP16116A based butterfly processor performs this operation in a low power high accuracy chip set.

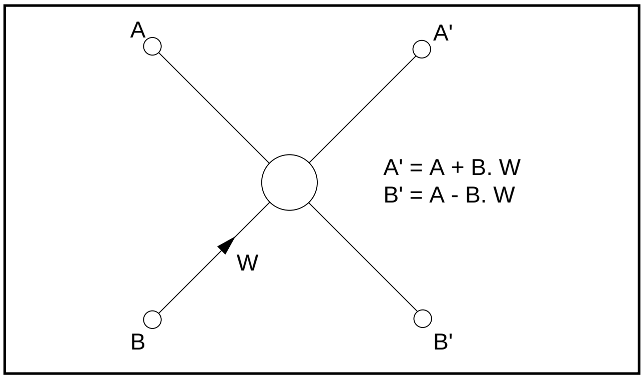


Fig.5 Butterfly Operation

A new butterfly operation is commenced each cycle, requiring a new set of data for , B, W, WTA and WTB. Five cycles later, the corresponding results A' and B' are produced along with their associated WTOUT. In between, the signals SFTA and SFTR are produced and acted upon by the shifters in the PDSP1601/A and PDSP16318/A. The timing of the data and control signals is shown in Fig.6.

The results (A' and B') of each butterfly calculation in a pass must be stored away to be used later as the input data (A and B) in the next pass. Each result must be stored together with its associated word tag, WTOUT. Although WTOUT is common to both A' and B', it must be stored separately with each word as the words are used on different cycles during the next pass. At the inputs, the word tag associated with the A word is known as WTA and the word tag associated with the B word is known as WTB. Hence, the WTOUTs from one pass will become the WTAs and WTBs for the following pass. It should be noted that the first pass is unique in that word tags need not be input into the butterfly as all data initially has the same weighting. Hence, during the first pass alone, the inputs WTA and WTB are ignored.

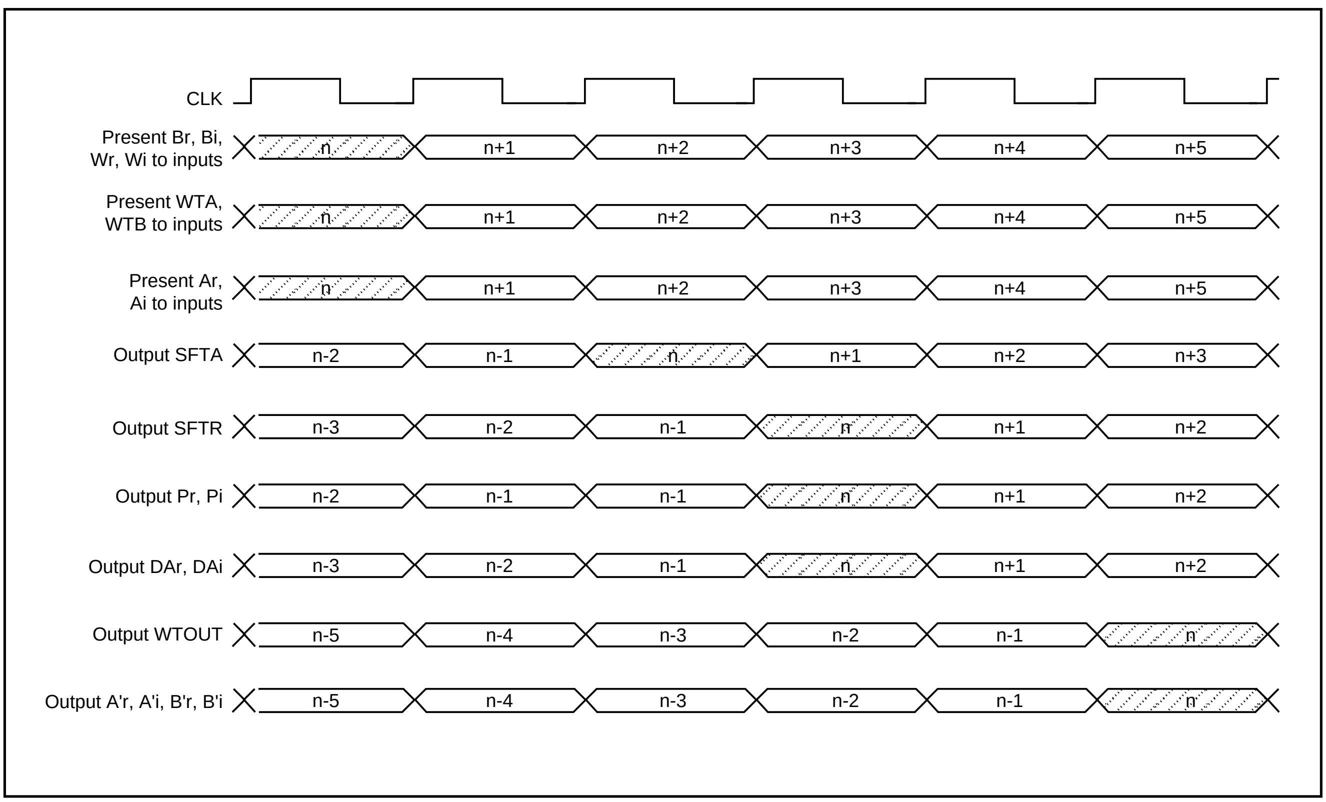


Fig.6 Butterfly Data and Control Signals

Control of the FFT

To enable the block floating point hardware to keep track of the data, the following signals are provided :

SOBFP - start of the FFT
EOPSS - end of current pass

These inform the PDSP16116/A when an FFT is starting and when each pass is complete. Fig.7 shows how these signals should be used and a commentary is provided below.

To commence the FFT, the signal EOPSS should be set high (where it will remain for the duration of the pass). SOBFP should be pulled low during the initial cycle when the first data words A and B are presented to the inputs of the butterfly processor. The following cycle SOBFP must be pulled high where it should remain for the duration of the FFT. New data is presented to the processor each successive cycle until the end of the first pass of the FFT. On the last cycle of the pass, the signal EOPSS should be pulled low and remain low for a minimum of five cycles *, the time required to clear the pipeline of the butterfly processor so that all the results from one pass are obtained before commencing the following pass. On the initial cycle of each new pass, the signal EOPSS should be pulled high and it should remain high until the final cycle of that pass, when it is pulled low again.

* Should a longer pause be required between passes - to arrange the data for the next pass, for example, then EOPSS may be kept low as long as necessary - the next pass cannot commence until it is brought high again.

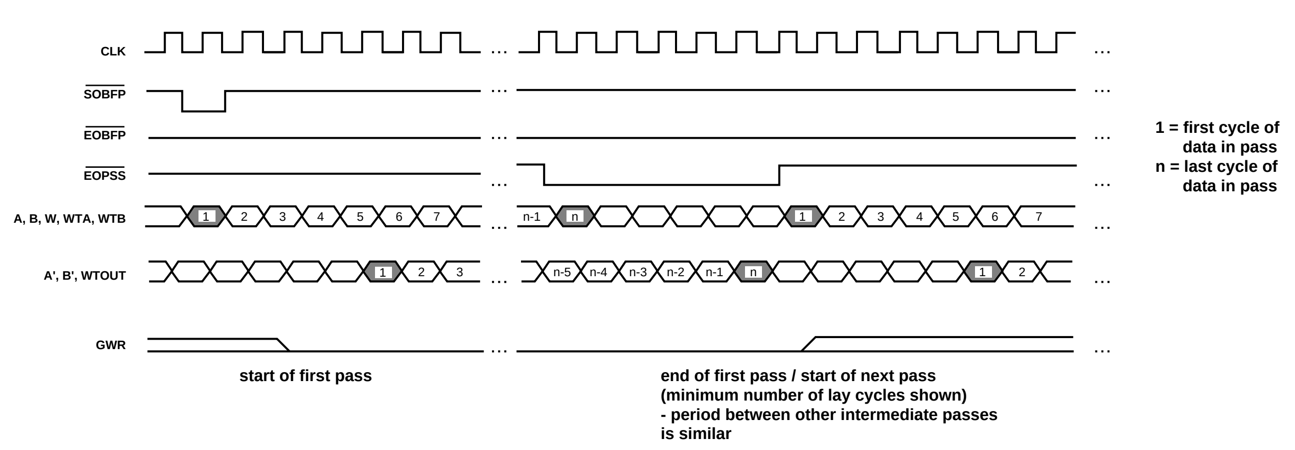


Fig.7 Use of the BFP Control Signals

FFT Output Normalisation

When an FFT system outputs a series of FFT results for display, storage or transmission, it is essential that all results are compatible, i.e. with the binary point in the same position. However, in order to preserve the dynamic range of the data in the FFT calculation, the PDSP1601/A employs a range of different weightings. Therefore, data must be re-formatted at the end of the FFT to be pre-determined common weighting. This can be done by comparing the exponent of given data word with the pre-determined unversial exponent and then shifting the data word by the difference. The PDSP1601/A, with its multifunction 16 bit barrel shifter, is ideally suited to this task.

What value should the Unversal Exponent take? Well, according to theory, the largest possible data result from an FFT is N times the largest input data. This means that the binary point can move a maximum of log2(N) places to the right. Hence, if we choose the Unverisal Exponent to be log2(N) this should give us sufficient range to represent all data points faithfully.

In practice, data output may never approach the theoretical maximum. Hence, it may be worthwhile to try various Unverisal Exponents and choose the one best suited to the particular application.

Data is output from the butterfly processor with a two-part exponent: the 5-bit GWR applicable to all data words from a given FFT and a 2-bit WTOUT associated with each individual data word. To find the complete exponent for a given word, the GWR for that FFT must be modified by its WTOUT as shown in Table 6. The result is the number of places the binary point has shifted to the right during the course of the FFT.

This value must be compared with the Unversial Exponent to determine the shift required. This is done by subtracting it from the Unversial Exponent. The number of places to be shifted is equal to the difference between the two exponents. The shift can be implemented in a PDSP1601/A. The shift value is fed into the SV port.

As FFT data consists of real and imaginary parts, either two PDSP1601As must be used (controlled by the same logic) or a single PDSP1601/A could be used handling real and imaginary data on alternate cycles (using the same instructions for both cycles).

An example of an output normalisation circuit is shown in Fig.8. Only 4 bit data paths are used in calculating the shift. This means that we must be able to trap very small values negative of GWR and force a 15-bit right shift in such cases.

N.B.

It is easier to simply add the word tag to the exponent for the purpose of determing the shift required, instead of modifying it according to Table.6. To compensate for this, the Universal Exponent may be increased by one.

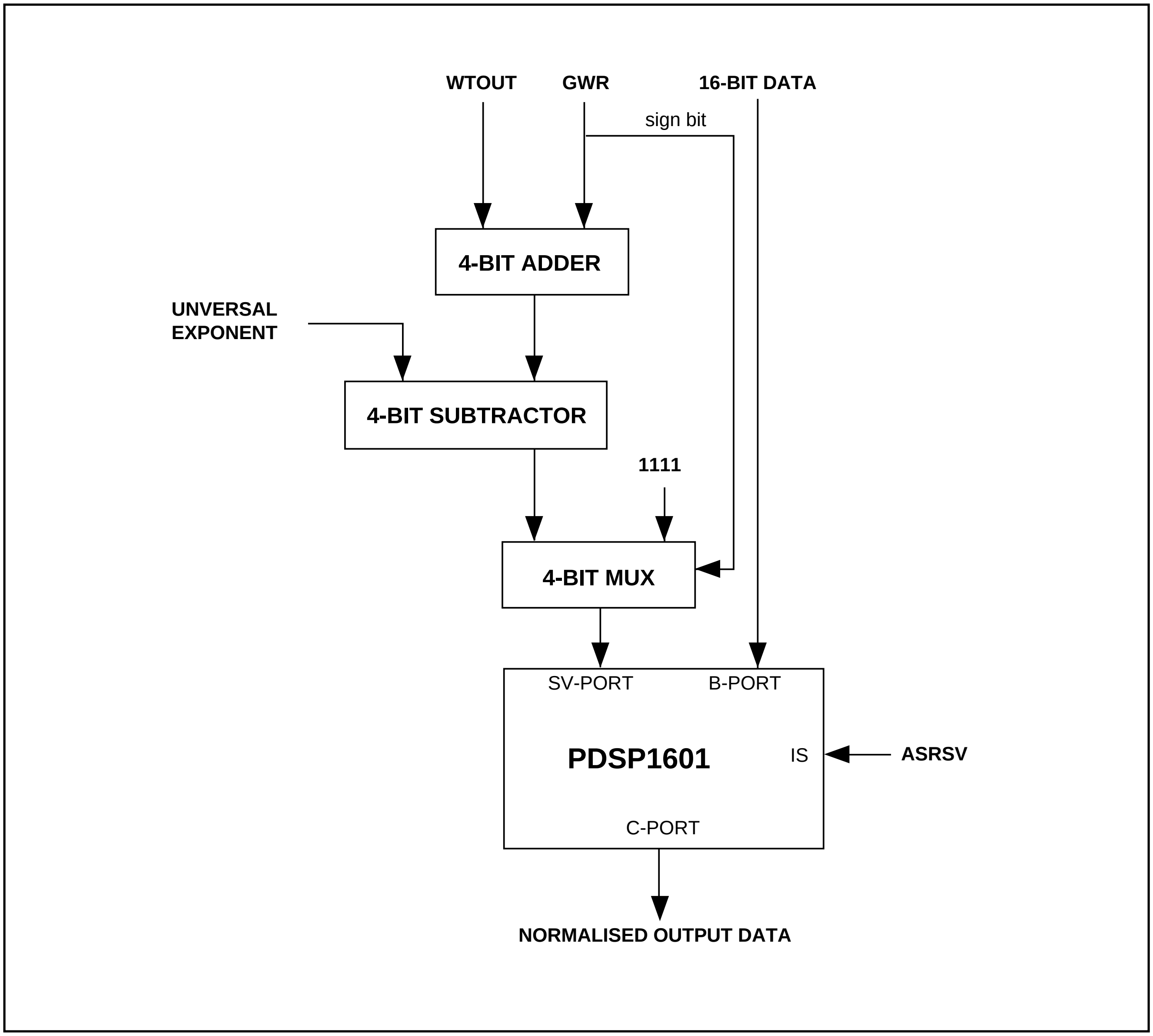


Fig.8 Output Normalisation Circuitry

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to V_{CC} +0.5V
Output voltage V_{OUT}	-0.5V to V_{CC} +0.5V
Clamp diode current per I_k (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature range T_S	-65°C to +150°C
Ambient temperature with power applied T_{AMB}	
Military	-55°C to +125°C
Industrial	-40°C to +85°C
Junction temperature	150°C
Package power dissipation	1000mW
Thermal resistances	
Junction to case $ø_{JC}$	12°C/W
Junction to case $ø_{JA}$	29°C/W

NOTES

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceedeed, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Operating conditions (unless otherwise stated):

Industrial: T_{AMB} = -40°C to +85°C, V_{CC} = 5.0V ± 10%, GND = 0V

Military: T_{AMB} = -55°C to +125°C, V_{CC} = 5.0V ± 10%, GND = 0V

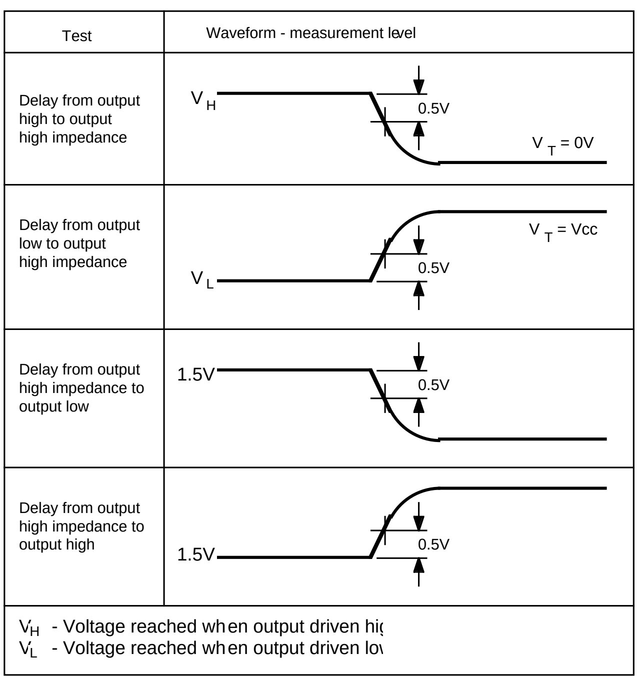
Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Min.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 8mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -8mA
Input high voltage	V_{IH}	3.0		-	V	CLK input only
Input high voltage	V_{IH}	2.2		-	V	All other inputs
Input low voltage	V_{IL}	-		0.8	V	GND <V_{IN}<V_{CC}
Input leakage current	I_{IN}	-10		+10	µA	
Input capacitance	C_{IN}		10		pF	GND <V_{IN}<V_{CC}
Output leakage current	I_{OZ}	-50		+50	µA	V_{CC} = Max
Output S/C current	I_{OS}	10		300	mA	

Switching Characteristics

Characteristic	PDSP16116 Min.	PDSP16116 Max.	PDSP16116A Min.	PDSP16116A Max.	Units	Conditions
CLK rising edge to P-PORTS	5	45	5	23	ns	2 x LSTTL + 20pF
CLK rising edge to WTOUT1:0	5	30	5	20	ns	2 x LSTTL + 20pF
CLK rising edge to GWR4:0	5	30	5	20	ns	2 x LSTTL + 20pF
CLK rising edge to SFTA1:0	5	60	5	30	ns	2 x LSTTL + 20pF
CLK rising edge to SFTR2:0	5	50	5	28	ns	2 x LSTTL + 20pF
Setup CEX or CEY to CLK rising edge	11	-	8	-	ns	
Hold CEX or CEY to CLK rising edge	-	0	-	0	ns	
Setup X or Y port inputs to CLK rising edge	11	-	8	-	ns	
Hold X or Y port inputs to CLK rising edge	-	2	-	0	ns	
Setup WTA1:0, WTB1:0, SOBFP or EOPSS inputs to CLK rising edge	14	-	8	-	ns	
Hold WTA1:0, WTB1:0, SOBFP or EOPSS inputs to CLK rising edge	-	0	-	0	ns	
Setup CONX or CONY inputs to CLK rising edge	14	-	8	-	ns	
Hold CONX or CONY inputs to CLK rising edge	-	0	-	0	ns	
Setup AR15:13 or AI15:13 to CLK rising edge	14	-	-	-	ns	
Hold AR15:13 or AI15:13 to CLK rising edge	-	0	-	0	ns	
OPSEL to valid P-PORTS	-	35	-	20	ns	2 x LSTTL + 20pF
OER or OEI rising PR-PORT or PI-PORT high to Z	-	35	-	25	ns	see Fig.9
OER or OEI rising PR-PORT or PI-PORT low to Z	-	45	-	25	ns	see Fig.9
OER or OEI falling PR-PORT or PI-PORT Z to high	-	22	-	18	ns	see Fig.9
OER or OEI falling PR-PORT or PI-PORT Z to low	-	24	-	18	ns	see Fig.9
Clock period	100	-	50	-	ns	
Clock high time	30	-	12	-	ns	
Clock low time	20	-	12	-	ns	
Vcc Current (CMOS input levels)	-	60	-	80	mA	see Note 4
Vcc Current (TTL input levels)	-	100	-	130	mA	see Note 4

NOTE 4 :- V_{CC} = Max Outputs unloaded, clock freq = Max



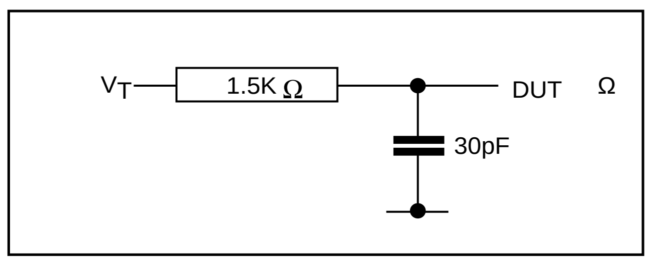


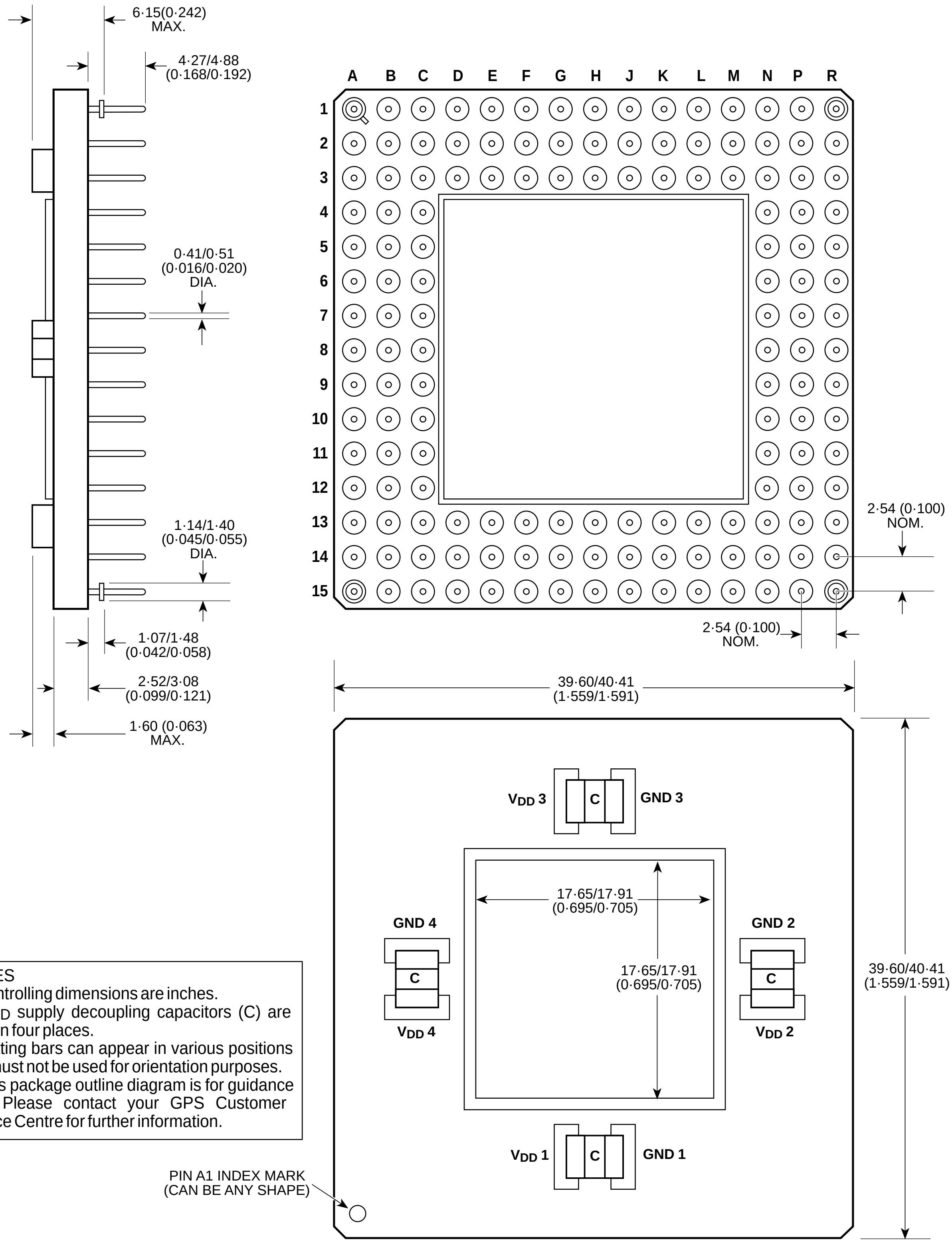
Fig.9 Three state delay measurement load

ORDERING INFORMATION

PDSP16116 MC GGDR	**10MHz**	**MIL-883 screened**
PDSP16116A B0 AC	**20MHz**	**Industrial**
PDSP16116A A0 AC	**20MHz**	**Military**
PDSP16116A B0 GG	**20MHz**	**Industrial**
PDSP16116A A0 GG	**20MHz**	**Military**
PDSP16116A MC GGDR	**20MHz**	**MIL-883 screened**
PDSP16116B B0 AC	**25MHz**	**Industrial**

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.

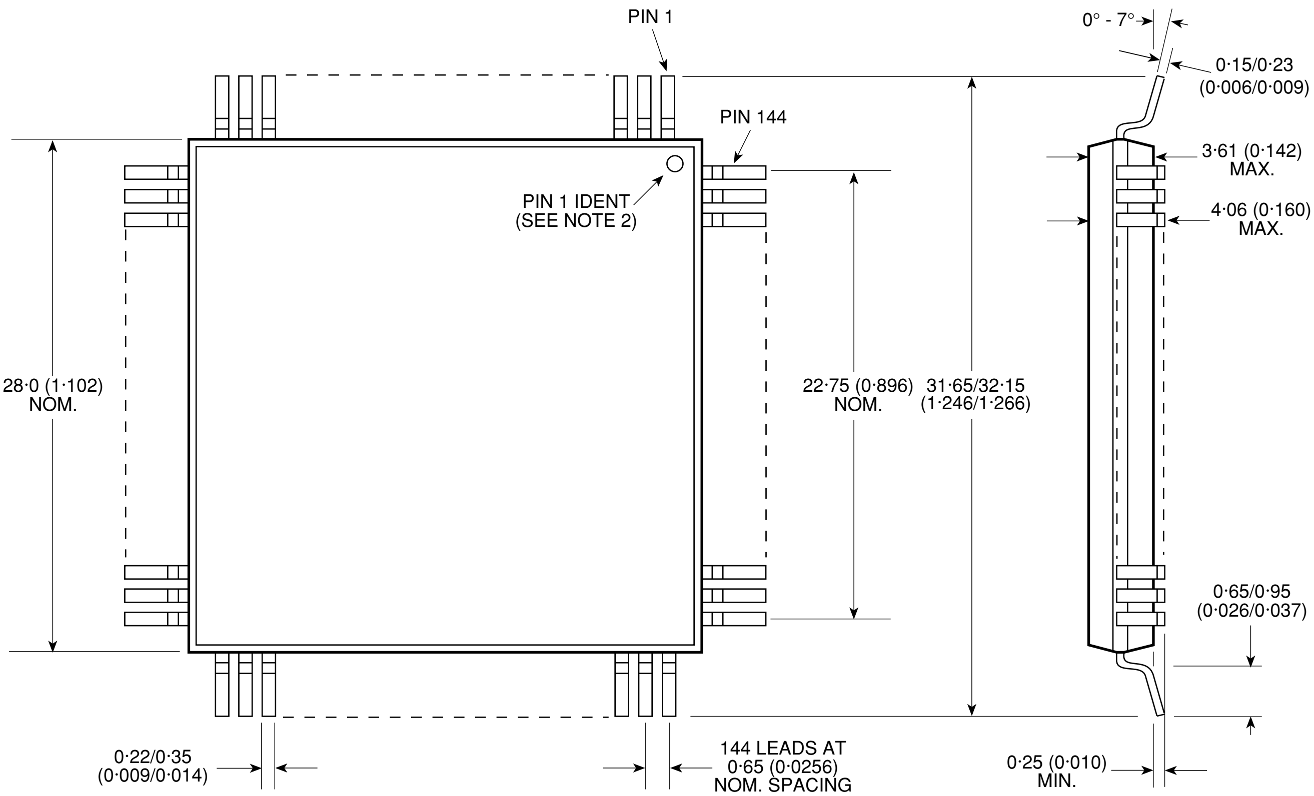


NOTES
1. Controlling dimensions are inches.
2. V_{DD} supply decoupling capacitors (C) are fitted in four places.
3. Plating bars can appear in various positions and must not be used for orientation purposes.
4. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

144-I/O PIN GRID ARRAY – AC144 (POWER)

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are millimetres.
2 Pin 1 identification can be either a dot or a cut-out.
3. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

144-LEAD CERAMIC QUAD FLATPACK – GG144

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