

3.3V 8M x 64/72-Bit 1 BANK SDRAM Module
3.3V 16M x 64/72-Bit 2 BANK SDRAM Module

HYS64/72V8200GU-8
HYS64/72V16220GU-8

PC100-168 pin unbuffered DIMM Modules

Advanced Information

- 168 Pin PC100-compatible unbuffered 8 Byte Dual-In-Line SDRAM Modules
- 1 bank 8M x 64, 8M x 72 and 2 bank 16M x 64, 16M x 72 organisation
- Optimized for byte-write non-parity or ECC applications
- JEDEC standard Synchronous DRAMs (SDRAM)
- Fully PC board layout compatible to INTEL's Rev. 1.0 module specification
- SDRAM Performance:

		PC100	Units
f _{CK}	Clock frequency (max.)	100	MHz
t _{AC}	Clock access time CAS latency = 2 & 3	6	ns

- Supported Latencies at 100 Mhz operation:

CL	tRCD	tRP	tRC	
3	2	2	8	CLK
2	2	2	7	CLK

- Single +3.3V(± 0.3V) power supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTTL compatible
- Serial Presence Detect with E²PROM
- Utilizes 8M x 8 SDRAMs in TSOPII-54 packages
- 4096 refresh cycles every 64 ms
- Gold contact pad
- Card Size: 133,35 mm x 31.75 mm x 4,00 mm

The HYS64(72)8200 and HYS64(72)16220 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organised as 8M x 64, 8M x 72 in 1 bank and 16M x 64 and 16M x 72 in two banks high speed memory arrays designed with 64M Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use -8 speed sort 9M x 8 SDRAM devices in TSOP54 packages to meet the PC100 requirement. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTEL's PC 100 module specification.

The DIMMs have a serial presence detect, implemented with a serial E²PROM using the two pin I²C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long footprint, with 1,25" (31,75 mm) height.

Ordering Information

Type	Ordering Code	Package	Descriptions	Module Height
HYS 64V8200GU-8	PC100-222-620	L-DIM-168-30	100 Mhz 8M x 64 1 bank SDRAM module	1,25"
HYS 72V8200GU-8	PC100-222-620	L-DIM-168-30	100 MHz 8M x 72 1 bank SDRAM module	1,25"
HYS 64V16220GU-8	PC100-222-620	L-DIM-168-30	100 Mhz 16M x 64 2 bank SDRAM module	1,25"
HYS 72V16220GU-8	PC100-222-620	L-DIM-168-30	100 Mhz 16M x 72 2 bank SDRAM module	1,25"

Pin Names

A0-A11	Address Inputs(RA0 ~ RA10 / CA0 ~ CA8)
BA0, BA1	Bank Selects
DQ0 - DQ63	Data Input/Output
CB0-CB7	Check Bits (x72 organisation only)
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Input
CKE0, CKE1	Clock Enable
CLK0 - CLK3	Clock Input
DQMB0 - DQMB7	Data Mask
CS0 - CS3	Chip Select
Vcc	Power (+3.3 Volt)
Vss	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
N.C.	No Connection

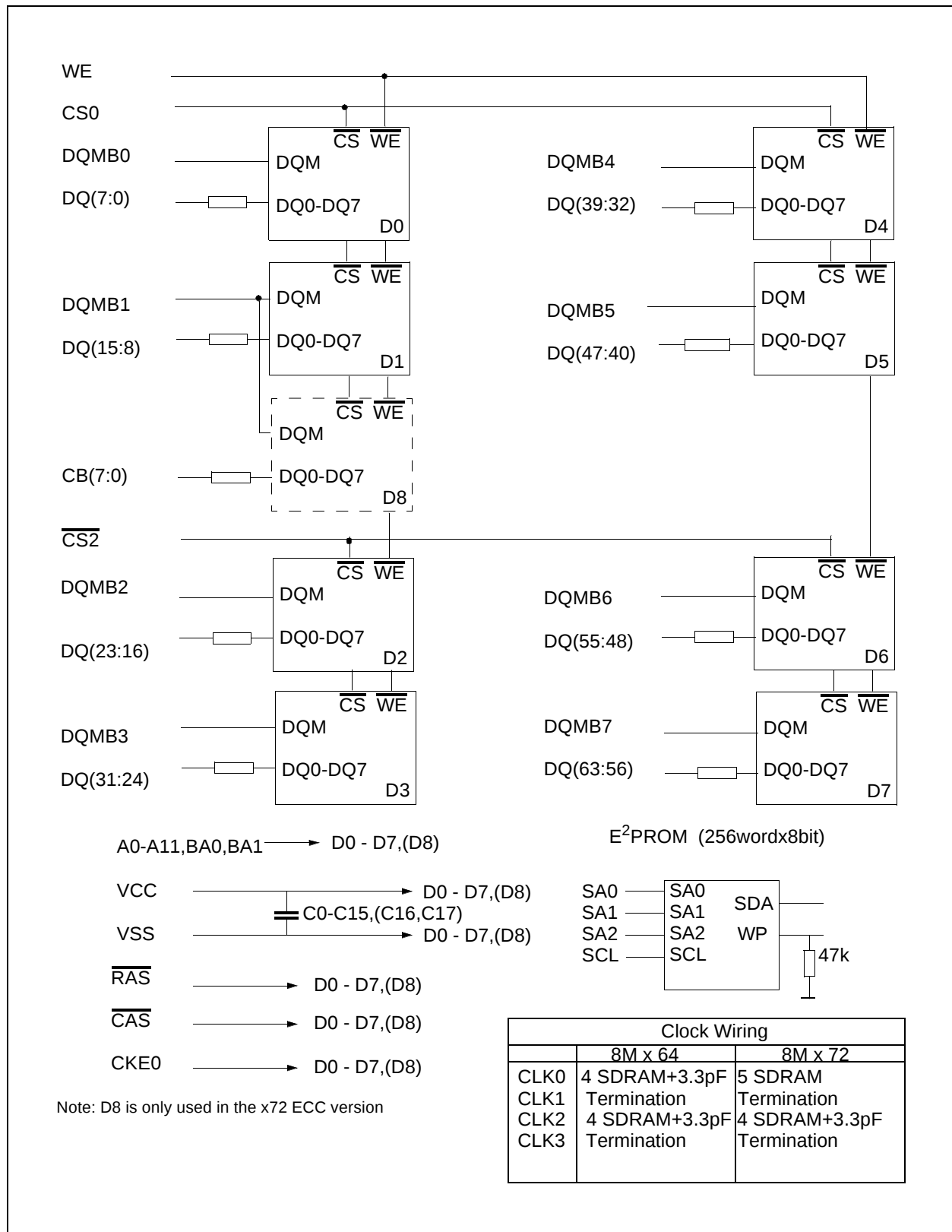
Address Format:

	Part Number	Rows	Columns	Bank Select	Refresh	Period	Interval
8M x 64	HYS 64V8200GU	12	9	2	4k	64 ms	15,6 µs
8M x 72	HYS 72V8200GU	12	9	2	4k	64 ms	15,6 µs
16M x 64	HYS 64V16220GU	12	9	2	4k	64 ms	15,6 µs
16M x 72	HYS 72V16220GU	12	9	2	4k	64 ms	15,6 µs

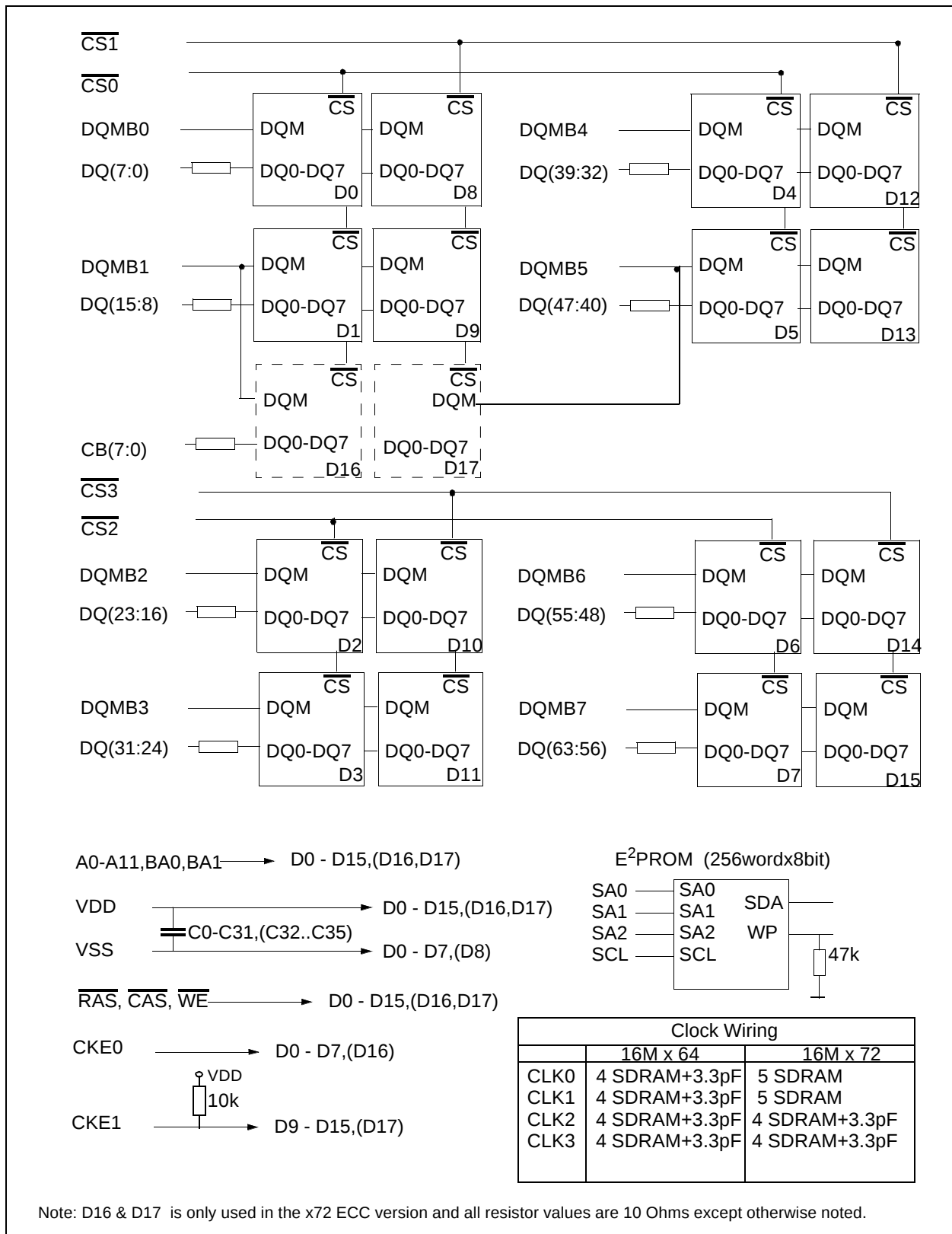
Pin Configuration

PIN #	Symbol	PIN #	Symbol	PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	CS2	87	DQ33	129	CS3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VCC	48	DU	90	VCC	132	NC
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC (CB2)	94	DQ39	136	CB6
11	DQ8	53	NC (CB3)	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	NC (CB0)	63	CKE1	105	NC (CB4)	147	NC
22	NC (CB1)	64	VSS	106	NC (CB5)	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS
27	WE	69	DQ24	111	CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	CS0	72	DQ27	114	CS1	156	DQ59
31	DU	73	VCC	115	RAS	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CLK2	121	A9	163	CLK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	CLK1	167	SA2
42	CLK0	84	VCC	126	NC	168	VCC

Note : Pinnames in brackets are for the x72 ECC versions



Block Diagram for 8M x 64/72 SDRAM DIMM modules (HYS64/72V8200GU)



Block Diagram for 16M x 64/72 SDRAM DIMM modules (HYS64/72V1620GU)

DC Characteristics
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{SS} = 0 \text{ V}; V_{DD}, V_{DDQ} = 3.3 \text{ V} \pm 0.3 \text{ V}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	$V_{CC}+0.3$	V
Input low voltage	V_{IL}	- 0.5	0.8	V
Output high voltage ($I_{OUT} = - 2.0 \text{ mA}$)	V_{OH}	2.4	-	V
Output low voltage ($I_{OUT} = 2.0 \text{ mA}$)	V_{OL}	-	0.4	V
Input leakage current, any input ($0 \text{ V} < V_{IN} < 3.6 \text{ V}$, all other inputs = 0 V)	$I_{I(L)}$	- 40	40	μA
Output leakage current (DQ is disabled, $0 \text{ V} < V_{OUT} < V_{CC}$)	$I_{O(L)}$	- 40	40	μA

Capacitance
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}, f = 1 \text{ MHz}$

Parameter	Symbol	Limit Values				Unit
		max. 8Mx64	max. 8Mx72	max. 16Mx64	max. 16Mx72	
Input capacitance (A0 to A11, BA0, BA1, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C_{I1}	45	55	80	90	pF
Input capacitance (CS0 -CS3,)	C_{I2}	20	25	30	35	pF
Input capacitance (CLK0 - CLK3)	C_{I3}	22	38	22	38	pF
Input capacitance (CKE0, CKE1)	C_{I4}	22	38	50	55	pF
Input capacitance (DQMB0 - DQMB7)	C_{I5}	13	13	20	20	pF
Input / Output capacitance (DQ0-DQ63, CB0-CB7)	C_{IO}	13	12	20	20	pF
Input Capacitance (SCL,SA0-2)	C_{SC}	8	8	8	8	pF
Input/Output Capacitance	C_{SD}	10	10	10	10	pF

Standby and Refresh Currents ($T_a = 0$ to 70°C , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$) ¹⁾

Parameter	Symbol	Test Condition	X64	X72		Note
			max.			
Operating Current	Icc1	Burst length = 4, CL=3 trc>=trc(min.), tck>=tck(min.), Io=0 mA 2 bank interleave operation	800	900	mA	1,2
Precharged Standby Current in Power Down Mode	Icc2P	CKE<=VIL(max), tck>=tck(min.)	24	27	mA	
	Icc2PS	CKE<=VIL(max), tck=infinite	16	18	mA	
Precharged Standby Current in Non-power Down Mode	Icc2N	CKE>=VIH(min), tck>=tck (min.), input changed once in 3 cycles	160	180	mA	$\overline{\text{CS}}$ = High
	Icc2NS	CKE>=VIH(min), tck=infinite, no input change	80	90	mA	
Active Standby Current in Power Down Mode	Icc3P	CKE<=VIL(max), tck>=tck(min.)	24	27	mA	
	Icc3PS	CKE<=VIL(max), tck=infinite	16	18	mA	
Active Standby Current in Non-power Down Mode	Icc3N	CKE>=VIH(min), tck>=tck (min.) input changed one time	200	225	mA	$\overline{\text{CS}}$ = High
	Icc3NS	CKE>=VIH(min), tck=infinite, no input change	120	135	mA	
Burst Operating Current	Icc4	Burst length = full page, trc = infinite, CL = 3, tck>=tck (min.), Io = 0 mA 2 banks activated	760	855	mA	1,2
Auto (CBR) Refresh Current	Icc5	trc>=trc(min)	720	810	mA	1,2
Self Refresh Current	Icc6	CKE=<0,2V	8	9	mA	1,2

AC Characteristics 3)4)

$T_A = 0$ to $70\text{ }^{\circ}\text{C}$; $V_{SS} = 0\text{ V}$; $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $t_T = 1\text{ ns}$

Parameter	Symbol	Limit Values		Unit	Note
		-PC100			
		min.	max.		

Clock and Clock Enable

Clock Cycle Time	t_{CK}				
		$\overline{CAS}$ Latency = 3	10	ns	
		$\overline{CAS}$ Latency = 2	10	ns	
System Frequency	f_{CK}	$\overline{CAS}$ Latency = 3	–	100	MHz
		$\overline{CAS}$ Latency = 2	–	100	MHz
Clock Access Time	t_{AC}	$\overline{CAS}$ Latency = 3	–	6	ns
		$\overline{CAS}$ Latency = 2	–	6	ns
Clock High Pulse Width	t_{CH}		3	–	ns
Clock Low Pulse Width	t_{CL}		3	–	ns
Input Setup time	t_{CS}		2	–	ns
Input Hold Time	t_{CH}		1	–	ns
CKE Setup Time (Power down mode)	t_{CKSP}		2.5	–	ns
CKE Setup Time (Self Refresh Exit)	t_{CKSR}		8	–	ns
Transition time (rise and fall)	t_T		1	–	ns

Common Parameters

RAS to $\overline{CAS}$ delay	t_{RCD}	20	–	ns	2 CLK
Cycle Time	t_{RC}	70	120k	ns	7 CLK
Active Command Period	t_{RAS}	45	–	ns	5 CLK
Precharge Time	t_{RP}	20	–	ns	2 CLK
Bank to Bank Delay Time	t_{RRD}	16	–	ns	2 CLK
$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	t_{CCD}	1	–	CLK	

Refresh Cycle

Self Refresh Exit Time	t_{SREX}	10	–	ns	9)
Refresh Period (4096 cycles)	t_{REF}	64	–	ms	8)

Parameter	Symbol	Limit Values		Unit	Note
		-PC100			
		min.	max.		

Read Cycle

Data Out Hold Time	t_{OH}	3	–	ns	4)
Data Out to Low Impedance Time	t_{LZ}	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	9	ns	10)
DQM Data Out Disable Latency	t_{DQZ}	2	–	CLK	

Write Cycle

Data input to Precharge (write recovery)	t_{DPL}	2	–	CLK	
Data In to Active/refresh	t_{DAL}	5	–	CLK	11)
DQM Write Mask Latency	t_{DQW}	0	–	CLK	

Notes:

1. The specified values are valid when addresses are changed no more than once during $t_{CK}(\min.)$ and when No Operation commands are registered on every rising clock edge during $t_{RC}(\min.)$. Values are shown per module bank.
2. The specified values are valid when data inputs (DQs) are stable during $t_{RC}(\min.)$.
3. All AC characteristics are shown for device level.
An initial pause of $100\mu s$ is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have $V_{il} = 0.4 V$ and $V_{ih} = 2.4 V$ with the timing referenced to the $1.4 V$ crossover point. The transition time is measured between V_{ih} and V_{il} . All AC measurements assume $t_T = 1 ns$ with the AC output load circuit show. Specified t_{AC} and t_{OH} parameters are measured with a $50 pF$ only, without any resistive termination and with a input signal of $1V / ns$ edge rate between $0.8V$ and $2.0 V$.

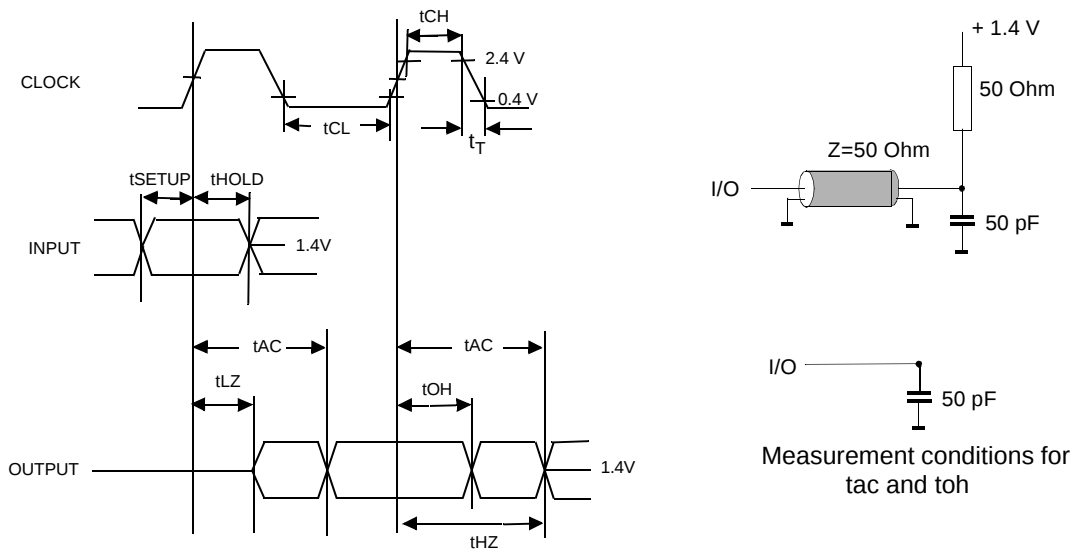


fig.1

5. If clock rising time is longer than $1 ns$, a time $(t_T/2 - 0.5) ns$ has to be added to this parameter.
6. Rated at $1.5 V$
7. If t_T is longer than $1 ns$, a time $(t_T - 1) ns$ has to be added to this parameter.
8. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
11. t_{DAL} is equivalent to $t_{DPL} + t_{RP}$.

A serial presence detect storage device - E²PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E²PROM device during module production using a serial presence detect protocol (I²C synchronous 2-wire bus).

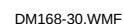
PD-Table:

Byte#	Description	SPD Entry Value	Hex			
			8Mx64	8Mx72	16Mx64	16Mx72
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	12	0C	0C	0C	0C
4	Number of Column Addresses (for x8 SDRAM)	9	09	09	09	09
5	Number of DIMM Banks	2	01	01	02	02
6	Module Data Width	64 / 72	40	48	40	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL=3	6.0 ns	60	60	60	60
11	Dimm Config (Error Det/Corr.)	none / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80	80	80
13	SDRAM width, Primary	x8	08	08	08	08
14	Error Checking SDRAM data width	n/a / x8	00	08	00	08
15	Minimum clock delay for back-to-back random column address	t _{ccd} = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	4	04	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 3	06	06	06	06
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/non reg.	00	00	00	00
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06	06	06
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 ns	A0	A0	A0	A0
24	Max. data access time from Clock for CL=2	6.0 ns	60	60	60	60
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	Maximum Data Access Time from Clock at CL=1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	20 ns	14	14	14	14
28	Minimum Row Active to Row Active delay tRRD	16 ns	10	10	10	10

SPD-Table (cont'd):

Byte#	Description	SPD Entry Value	Hex			
			8Mx64	8Mx72	16Mx64	16Mx72
29	Minimum RAS to CAS delay tRCD	20 ns	14	14	14	14
30	Minimum RAS pulse width tRAS	45 ns	2D	2D	2D	2D
31	Module Bank Density (per bank)	64 MByte	10	10	10	10
32	SDRAM input setup time	2 ns	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input hold time	2 ns	20	20	20	20
35	SDRAM data input setup time	1 ns	10	10	10	10
62-61	Superset information (may be used in future)		FF	FF	FF	FF
62	SPD Revision	Revision 1	D8	EA	D9	EB
63	Checksum for bytes 0 - 62		63	6D	64	76
64-125	Manufacturers information (optional) (FFh if not used)		XX	XX	XX	XX
126	Frequency Specification	100 MHz	64	64	64	64
127	100 MHz support details		AF	AF	FF	FF
128+	Unused storage locations		FF	FF	FF	FF

L-DIM-168-30



x) on ECC modules only