T-46-13-27

National Semiconductor

# NMC93CS06/CS46 256-Bit/1024-Bit Serial Electrically Erasable Programmable Memories

## General Description

The NMC93CS06/NMC93CS46 are 256/1024 bits of read/write memory divided into 16/64 registers of 16 bits each. N registers ($N \leq 16$ or $N \leq 64$) can be protected against data modification by programming into a special on-chip register called the memory protect register the address of the first register to be protected. This address can be locked into the device, so that these registers can be permanently protected. Thereafter, all attempts to alter data in a register whose address is equal to or greater than the address stored in the protect register will be aborted.

The read instruction loads the address of the first register to be read into a 6-bit address pointer. Then the data is clocked out serially on the DO pin and automatically cycles to the next register to produce a serial data stream. In this way the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 256/1024 bits. Thus, the NMC93CS06/NMC93CS46 can be viewed as a non-volatile shift register.

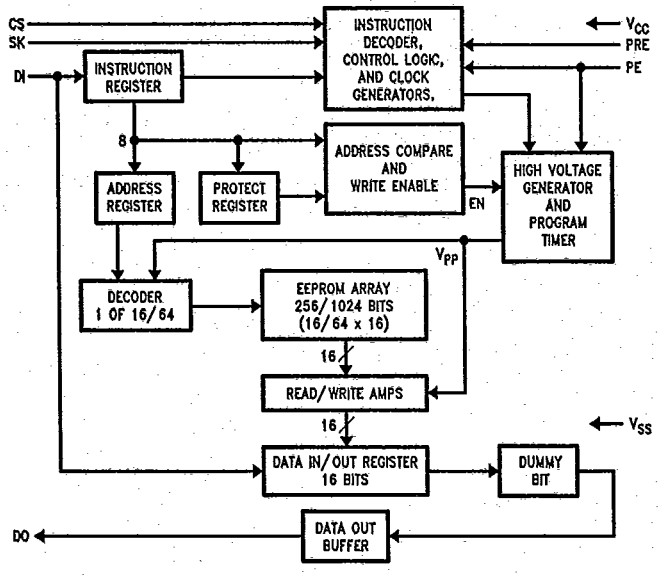
The write cycle is completely self-timed. No separate erase cycle is required before write. The write cycle is only enabled when pin 6 (program enable) is held high. If the address of the register to be written is less than the address in the protect register then the data is written 16 bits at a time into one of the 16/64 data registers. If CS is brought high following the initiation of a write cycle the DO pin indicates the ready/busy status of the chip.

National Semiconductor's EEPROMs are designed and tested for applications requiring extended endurance. Refer to device operation for further endurance information. Data retention is specified to be greater than 40 years.

## Features

- Write protection in user defined section of memory
- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5 volt only operation in all modes
- Microwire compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential register read
- Over 40 years data retention
- Designed for 100,000 write cycles

## Block Diagram

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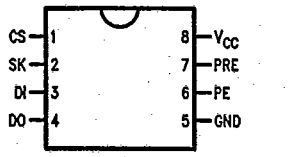
## Connection Diagrams

**PIN OUT:**

**Dual-In-Line Package (N)**

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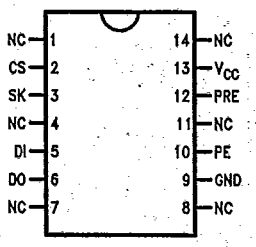
**Top View**

**See NS Package Number N08E**

| Pin Names | |
|---|---|
| CS | Chip Select |
| SK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| GND | Ground |
| PE | Program Enable |
| PRE | Protect Register Enable |
| $V_{CC}$ | Power Supply |

**PIN OUT:**

**SO Package (M)**

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**Top View**

**See NS Package Number M14A**

## Ordering Information

**Commercial Temp. Range (0°C to +70°C)**
$V_{CC}$ = 5V ± 10%

| Order Number |
|---|
| NMC93CS06N/NMC93CS46N |
| NMC93CS06M/NMC93CS46M |

**Extended Temp. Range (−40°C to +85°C)**
$V_{CC}$ = 5V ± 10%

| Order Number |
|---|
| NMC93CS06EN/NMC93CS46EN |
| NMC93CS06EM/NMC93CS46EM |

**Military Temp. Range (−55°C to +125°C)**

| Order Number |
|---|
| NMC93CS06MN/NMC93CS46MN |
| NMC93CS06MM/NMC93CS46MM |

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Ambient Storage Temperature | −65°C to +150°C |
| All Input or Output Voltages with Respect to Ground | +6.5V to −0.3V |
| Lead Temperature (Soldering, 10 sec.) | +300°C |
| ESD rating | 2000V |

## Operating Conditions

| | |
|---|---|
| Ambient Operating Temperature | |
| NMC93CS06/NMC93CS46 | 0°C to +70°C |
| NMC93CS06E/NMC93CS46E | −40°C to +85°C |
| NMC93CS06M/NMC93CS46M (Mil. Temp.) | −55°C to +125°C |
| Positive Power Supply | 4.5V to 5.5V |

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## DC and AC Electrical Characteristics $V_{CC}$ = 5V ±10% unless otherwise specified

| Symbol | Parameter | Part Number | Conditions | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | Operating Current CMOS Input Levels | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M* | CS = $V_{IH}$, SK = 1 MHz<br>SK = 0.5 MHz<br>SK = 0.5 MHz | | 2<br>2<br>2 | mA |
| $I_{CC2}$ | Operating Current TTL Input Levels | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | CS = $V_{IH}$, SK = 1 MHz<br>SK = 0.5 MHz<br>SK = 0.5 MHz | | 3<br>3<br>4 | mA |
| $I_{CC3}$ | Standby Current | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | CS = 0V | | 50<br>100<br>100 | µA |
| $I_{IL}$ | Input Leakage | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | $V_{IN}$ = 0V to $V_{CC}$ | −2.5<br>−10<br>−10 | 2.5<br>10<br>10 | µA |
| $I_{OL}$ | Output Leakage | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | $V_{OUT}$ = 0V to $V_{CC}$ | −2.5<br>−10<br>−10 | 2.5<br>10<br>10 | µA |
| $V_{IL}$<br>$V_{IH}$ | Input Low Voltage<br>Input High Voltage | | | −0.1<br>2 | 0.8<br>$V_{CC}$ + 1 | V |
| $V_{OL1}$ | Output Low Voltage | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | $I_{OL}$ = 2.1 mA<br>$I_{OL}$ = 2.1 mA<br>$I_{OL}$ = 1.8 mA | | 0.4<br>0.4<br>0.4 | V |
| $V_{OH1}$ | Output High Voltage | | $I_{OH}$ = −400 µA | 2.4 | | |
| $V_{OL2}$<br>$V_{OH2}$ | Output Low Voltage<br>Output High Voltage | | $I_{OL}$ = 10 µA<br>$I_{OH}$ = −10 µA | <br>$V_{CC}$ − 0.2 | 0.2 | V |
| $f_{SK}$ | SK Clock Frequency | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | | 0<br>0<br>0 | 1<br>0.5<br>0.5 | MHz |
| $t_{SKH}$ | SK High Time | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | (Note 2)<br>(Note 3)<br>(Note 3) | 250<br>500<br>500 | | ns |
| $t_{SKL}$ | SK Low Time | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | (Note 2)<br>(Note 3)<br>(Note 3) | 250<br>500<br>500 | | ns |
| $t_{CS}$ | Minimum CS Low Time | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | (Note 4)<br>(Note 5)<br>(Note 5) | 250<br>500<br>500 | | ns |
| $t_{CSS}$ | CS Setup Time | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | Relative to SK | 50<br>100<br>100 | | ns |
| $t_{PRES}$ | PRE Setup Time | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | Relative to SK | 50<br>100<br>100 | | ns |

*Throughout this table "M" refers to temperature range (−55°C to +125°C), not package.

## DC and AC Electrical Characteristics $V_{CC}$ = 5V ±10% unless otherwise specified (Continued)

| Symbol | Parameter | Part Number | Conditions | Min | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PES}$ | PE Setup Time | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | Relative to SK | 50<br>100<br>100 | | ns |
| $t_{DIS}$ | DI Setup Time | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | Relative to SK | 100<br>200<br>200 | | ns |
| $t_{CSH}$ | CS Hold Time | | Relative to SK | 0 | | ns |
| $t_{PEH}$ | PE Hold Time | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | Relative to CS<br>Relative to CS<br>Relative to CS | 250<br>500<br>500 | | ns |
| $t_{PREH}$ | PRE Hold Time | | Relative to SK | 0 | | ns |
| $t_{DIH}$ | DI Hold Time | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | Relative to SK | 100<br>200<br>200 | | ns |
| $t_{PD1}$ | Output Delay to "1" | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | AC Test | | 500<br>1000<br>1000 | ns |
| $t_{PD0}$ | Output Delay to "0" | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | AC Test | | 500<br>1000<br>1000 | ns |
| $t_{SV}$ | CS to Status Valid | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | AC Test | | 500<br>1000<br>1000 | ns |
| $t_{DF}$ | CS to DO in TRI-STATE® | NMC93CS06/NMC93CS46<br>NMC93CS06E/NMC93CS46E<br>NMC93CS06M/NMC93CS46M | $CS = V_{IL}$<br>AC Test | | 100<br>200<br>200 | ns |
| $t_{WP}$ | Write Cycle Time | | | | 10 | ms |

**Note 1:** Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 microsecond. For example if $t_{SKL}$ = 250 ns then the minimum $t_{SKH}$ = 750 ns in order to meet the SK frequency specification.

**Note 3:** The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 microseconds. For example, if $t_{SKL}$ = 500 ns then the minimum $t_{SKH}$ = 1.5 microseconds in order to meet the SK frequency specification.

**Note 4:** For Commercial parts CS must be brought low for a minimum of 250 ns ($t_{CS}$) between consecutive instruction cycles.

**Note 5:** For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns ($t_{CS}$) between consecutive instruction cycles.

**Note 6:** This parameter is periodically sampled and not 100% tested.

## Capacitance (Note 6)

$T_A$ = 25°C, f = 1MHz

| Symbol | Test | Typ | Max | Units |
|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance | | 5 | pF |
| $C_{IN}$ | Input Capacitance | | 5 | pF |

## AC Test Conditions

| | |
|---|---|
| Output Load | 1 TTL Gate and $C_L$ = 100 pF |
| Input Pulse Levels | 0.4V to 2.4V |
| Timing Measurement Reference Level | |
| Input | 1V and 2V |
| Output | 0.8V and 2V |

## Functional Description

The NMC93CS06 and NMC93CS46 have 10 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8-bits carry the op code and the 6-bit address for selection of 1 of 16 or 64 16-bit registers.

**Read (READ):**

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the NONVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

**Write Enable (WEN):**

When $V_{CC}$ is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or $V_{CC}$ is removed from the part.

**Write (WRITE):**

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns ($t_{CS}$). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

**Write All (WRALL):**

The Write All (WRALL) instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns ($t_{CS}$).

**Write Disable (WDS):**

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

**Protect Register Read (PRREAD):**

The Protect Register Read (PRREAD) instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction. Following the PRREAD instruction the 6-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6-bit address string.

**Protect Register Enable (PREN):**

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

## Instruction Set for the NMC93CS06 and NMC93CS46

| Instruction | SB | Op Code | Address | Data | PRE | PE | Comments |
|---|---|---|---|---|---|---|---|
| READ | 1 | 10 | A5–A0 | | 0 | X | Reads data stored in memory, starting at specified address. |
| WEN | 1 | 00 | 11XXXX | | 0 | 1 | Write enable must precede all programming modes. |
| WRITE | 1 | 01 | A5–A0 | D15–D0 | 0 | 1 | Writes register if address is unprotected. |
| WRALL | 1 | 00 | 01XXXX | D15–D0 | 0 | 1 | Writes all registers. Valid only when Protect Register is cleared. |
| WDS | 1 | 00 | 00XXXX | | 0 | X | Disables all programming instructions. |
| PRREAD | 1 | 10 | XXXXXX | | 1 | X | Reads address stored in Protect Register. |
| PREN | 1 | 00 | 11XXXX | | 1 | 1 | Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions. |
| PRCLEAR | 1 | 11 | 111111 | | 1 | 1 | Clears the Protect Register so that no registers are protected from WRITE. |
| PRWRITE | 1 | 01 | A5–A0 | | 1 | 1 | Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE. |
| PRDS | 1 | 00 | 000000 | | 1 | 1 | One time only instruction after which the address in the Protect Register cannot be altered. |

## Functional Description (Continued)

**Protect Register Clear (PRCLEAR):**

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

**Protect Register Write (PRWRITE):**

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

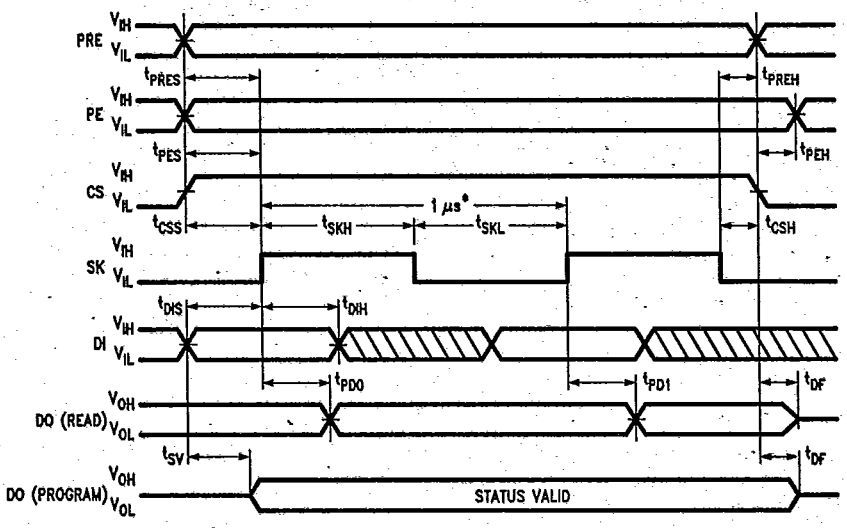
**Protect Register Disable (PRDS):**

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

## Timing Diagrams

**Synchronous Data Timing**

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*This is the minimum SK period (See Note 2).

## Timing Diagrams (Continued)

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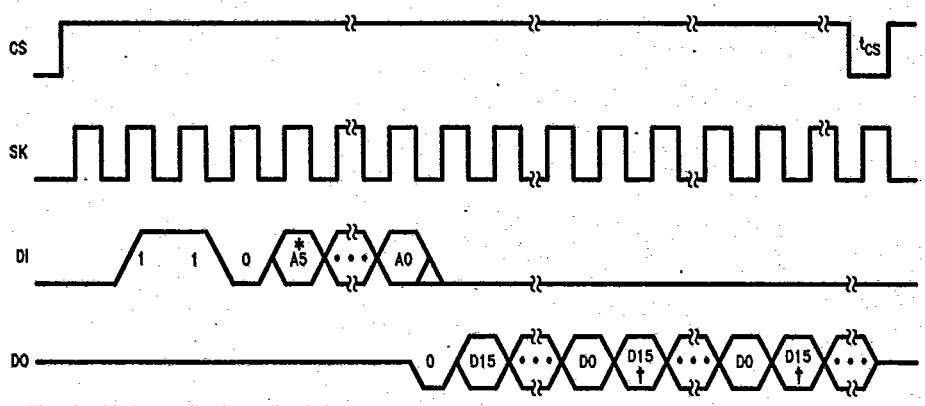
**READ:**
**PRE = 0, PE = X**




*Address bits A5 and A4 become "don't cares" for NMC93CS06
†The memory automatically cycles to the next register.

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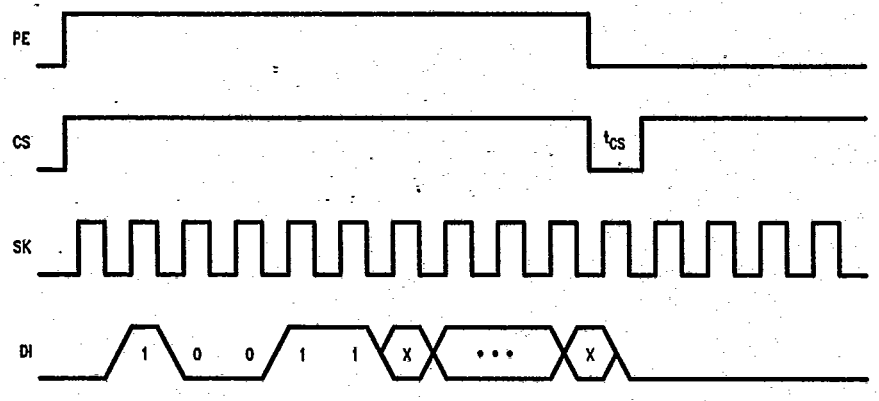
**WEN:**
**PRE = 0, D0 = TRI-STATE**

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## Timing Diagrams (Continued)

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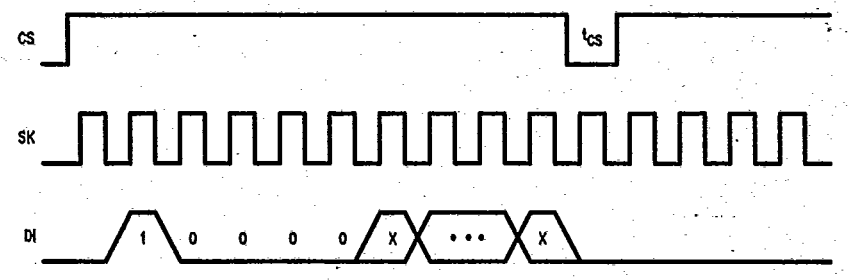
**WDS:**
**PRE = 0, PE = X, DO = TRI-STATE**

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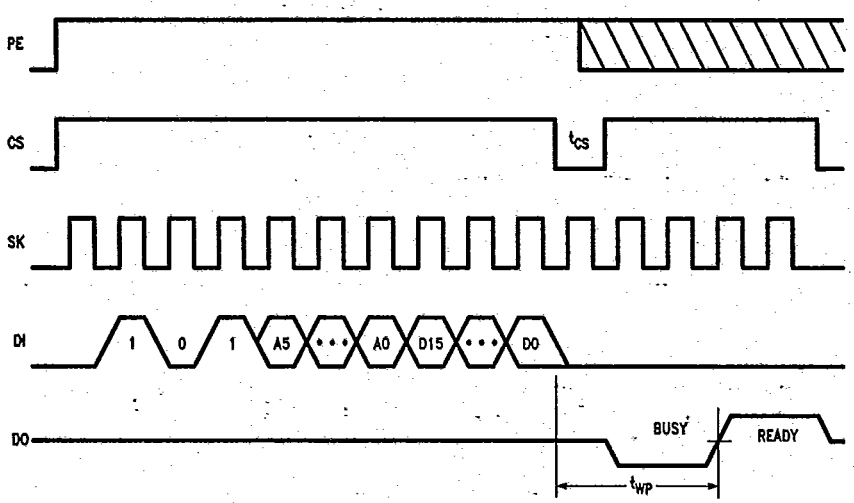
**WRITE:**
**PRE = 0**

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• Address bits A5 and A4 become "don't cares" for NMC93CS06

## Timing Diagrams (Continued)

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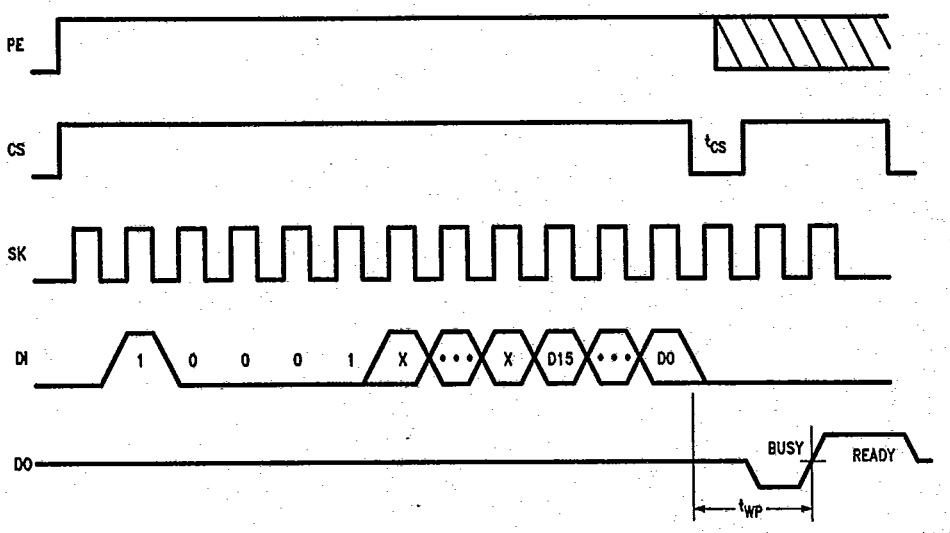
**WRALL*:**
**PRE = 0**




*Protect Register MUST be cleared.

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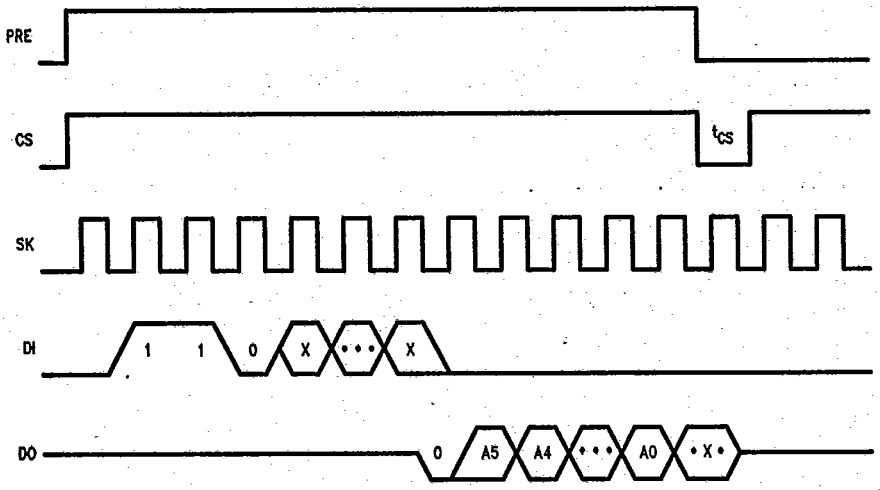
**PRREAD:**
**PE = X**

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*Address bits A5 and A4 become "don't cares" for NMC93CS06

## Timing Diagrams (Continued)

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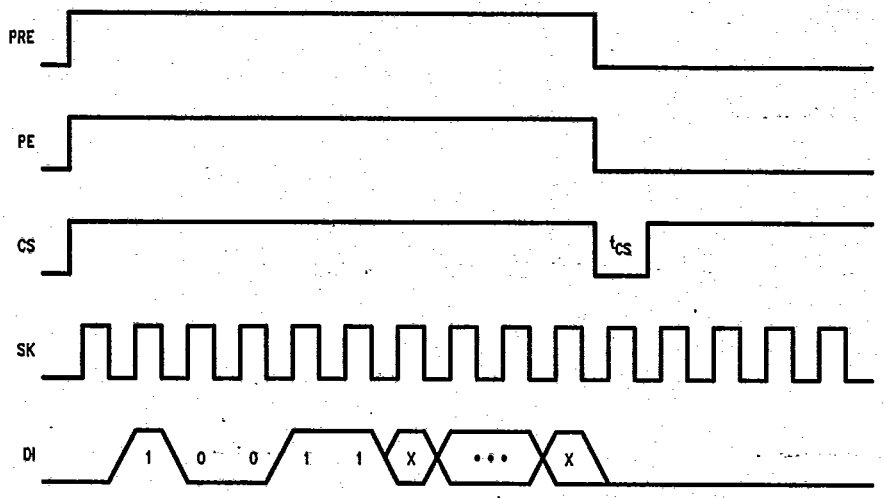
**PREN*:**
**DO = TRI-STATE**

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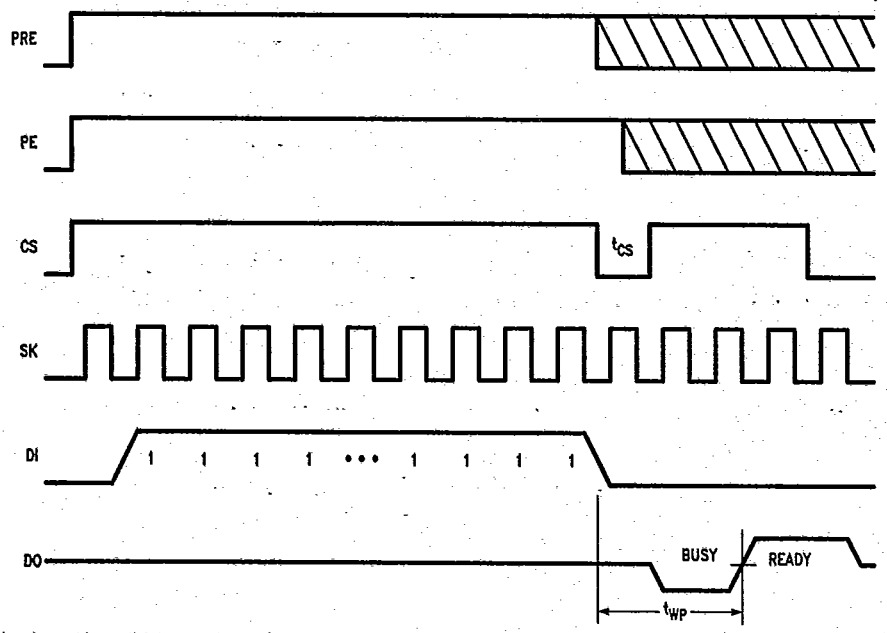
*A WEN cycle must precede a PREN cycle.

**PRCLEAR*:**




*A PREN cycle must immediately precede a PRCLEAR cycle.

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## Timing Diagrams (Continued)

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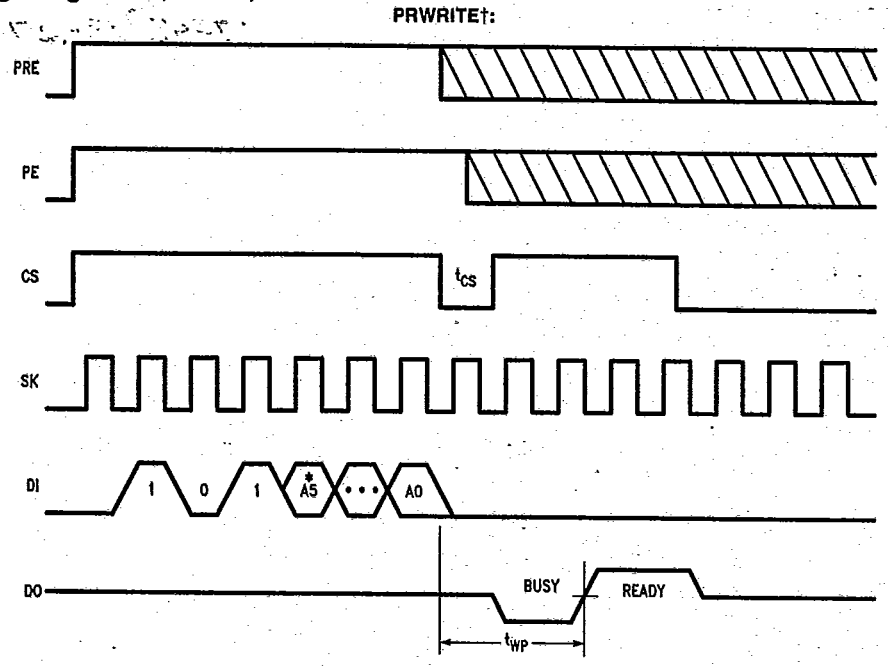
**PRWRITE†:**

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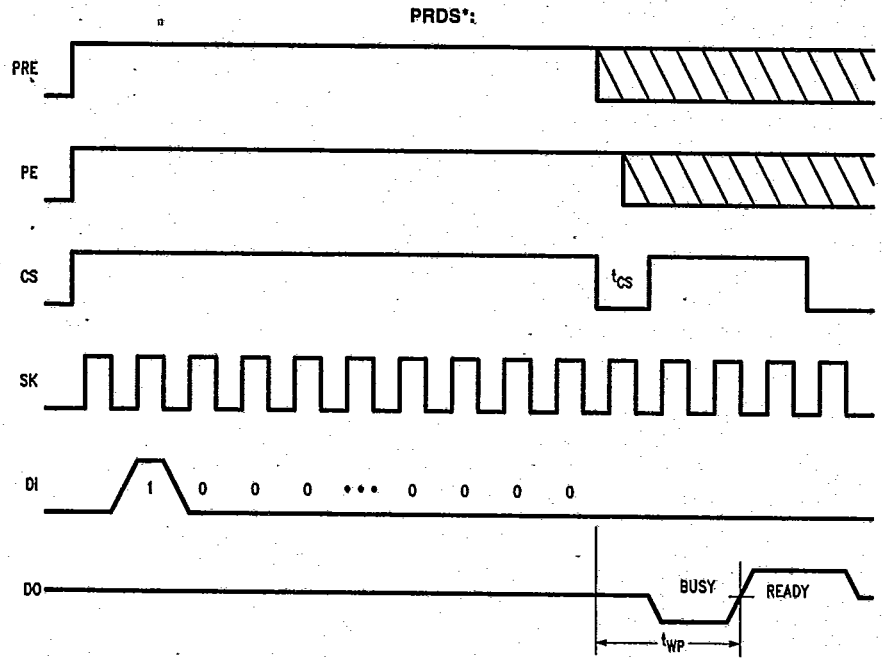
*Address bits A5 and A4 become "don't cares" for NMC93CS06

†Protect Register MUST be cleared before a PRWRITE cycle. A PREN cycle must immediately precede a PRWRITE cycle.

**PRDS*:**

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*ONE TIME ONLY Instruction. A PREN cycle must immediately precede a PRDS cycle.

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