FAIRCHILD SEMICONDUCTOR™

February 1999

# NM93C86A
# 16,384-Bit Serial EEPROM (MICROWIRE™ Bus Interface)

## General Description

The NM93C86A is 16,384 bits of CMOS nonvolatile, electrically erasable memory available in user organized as either 1024 16-bit registers or 2048 8-bit registers. The user organization is determined by the status of the ORG input. The memory device is fabricated using Fairchild Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM93C86A is available in 8-pin SO and TSSOP packages for space considerations.

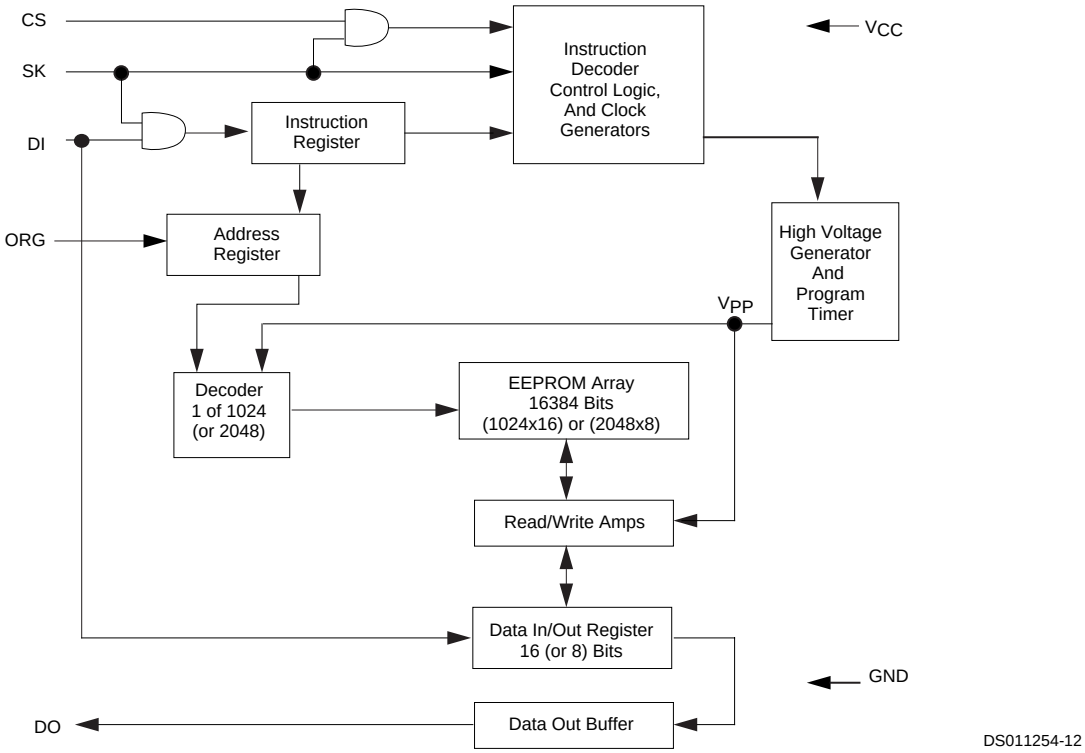
The EEPROM is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C86A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C86A defaults to the 1024 x 16 configuration if the ORG pin (Pin 6) is left floating, as it is internally pulled up to $V_{CC}$.

## Features

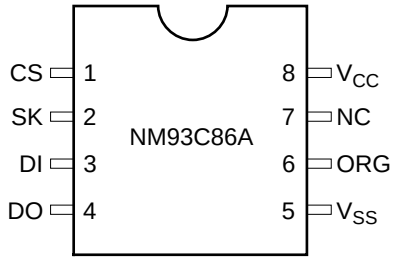
- 2.7V to 5.5V operation in all modes
- Typical active current of 200μA
  10μA standby current typical
  1μA standby current typical (L)
  0.1μA standby current typical (LZ)
- Device status indication during programming mode
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE™ compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP

## Block Diagram



## Connection Diagram

**Dual-In-Line Package (N)**
**and 8-Pin SO Package (M8)**

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**Top View**
**See Package Number**
**N08E and M08A**

## Pin Names

| Pin | Description |
|---|---|
| CS | Chip Select |
| SK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| $V_{SS}$ | Ground |
| ORG | Memory Organization Select |
| NC | No Connect |
| $V_{CC}$ | Positive Power Supply |

## Ordering Information

**NM** 93 C XX A LZ E XX

| | | Letter | Description |
|---|---|---|---|
| **Package** | | N | 8-Pin DIP |
| | | M8 | 8-Pin SO8 |
| **Temp. Range** | | None | 0 to 70°C |
| | | V | -40 to +125°C |
| | | E | -40 to +85°C |
| **Voltage Operating Range** | | Blank | 4.5V to 5.5V |
| | | L | 2.7V to 5.5V |
| | | LZ | 2.7V to 5.5V and <1µA Standby Current |
| | | A | x8 or x16 Configuration |
| **Density** | | 86 | 16K |
| | | C | CMOS |
| **Interface** | | 93 | MICROWIRE - 3 or 4 Wire Interface |
| **NM** | | | **Fairchild Non-Volatile Memory** |

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Ambient Storage Temperature | -65°C to +150°C |
| All Input or Output Voltage with Respect to Ground | $V_{CC}$ + 1 to -0.3V |
| Lead Temperature (Soldering, 10 seconds) | +300°C |
| ESD Rating | 2000V |

## Operating Range

| | |
|---|---|
| Ambient Operating Temperature | |
| NM93C86A | 0°C to +70°C |
| NM93C86AE | -40°C to +85°C |
| NM93C86AV | -40°C to +125°C |
| Power Supply ($V_{CC}$) Range | 4.5V to 5.5V |

## DC and AC Electrical Characteristics $4.5V \le V_{CC} \le 5.5V$

| Symbol | Parameter | Part Number | Conditions | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CCA}$ | Operating Current | | CS = $V_{IH}$, SK=1 MHz | | 1 | mA |
| $I_{CCS}$ | Standby Current | | CS = 0V ORG = $V_{CC}$ or NC | | 50 | µA |
| $I_{IL}$ | Input Leakage | | $V_{IN}$ = 0V to $V_{CC}$ (Note 2) | -1 | 1 | µA |
| $I_{ILO}$ | Input Leakage ORG Pin | | ORG tied to $V_{CC}$<br>ORG tied to $V_{SS}$<br>(Note 3) | -1<br>-2.5 | 1<br>2.5 | µA |
| $I_{OL}$ | Output Leakage | | $V_{IN}$ = 0V to $V_{CC}$ | -1 | 1 | µA |
| $V_{IL}$ | Input Low Voltage | | | -0.1 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | 2 | $V_{CC}$ +1 | V |
| $V_{OL1}$ | Output Low Voltage | | $I_{OL}$ = 2.1 mA | | 0.4 | V |
| $V_{OH1}$ | Output High Voltage | | $I_{OH}$ = -400 µA | 2.4 | | V |
| $V_{OL2}$ | Output Low Voltage | | $I_{OL}$ = 10 µA | | 0.2 | V |
| $V_{OH2}$ | Output High Voltage | | $I_{OL}$ = -10 µA | $V_{CC}$ - 0.2 | | V |
| $f_{SK}$ | SK Clock Frequency | | (Note 4) | 0 | 1 | MHz |
| $t_{SKH}$ | SK High Time | NM93C86A<br>NM93C86AE/V | | 250<br>300 | | ns |
| $t_{SKL}$ | SK Low Time | | | 250 | | ns |
| $t_{CS}$ | Minimum CS Low Time | | (Note 5) | 250 | | ns |
| $t_{CSS}$ | CS Set-up Time | | | 50 | | ns |
| $t_{DH}$ | DO Hold Time | | | 70 | | ns |
| $t_{DIS}$ | DI Set-up Time | NM93C86A<br>NM93C86AE/V | | 100<br>200 | | ns |
| $t_{CSH}$ | CS Hold Time | | | 0 | | ns |
| $t_{DIH}$ | DI Hold Time | | | 20 | | ns |
| $t_{PD1}$ | Output Delay to “1” | | | | 500 | ns |
| $t_{PD0}$ | Output Delay to “0” | | | | 500 | ns |
| $t_{SV}$ | CS to Status Valid | | | | 500 | ns |
| $t_{DF}$ | CS to DO in TRI-STATE® | | | | 100 | ns |
| $t_{WP}$ | Write Cycle Time | | | | 10 | ms |

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Ambient Storage Temperature | –65°C to +150°C |
| All Input or Output Voltage with Respect to Ground | +6.5V to -0.3V |
| Lead Temperature (Soldering, 10 sec.) | +300°C |
| ESD Rating | 2000V |

## Operating Range

| | |
|---|---|
| Ambient Operating Temperature | |
| NM93C86AL/LZ | 0°C to +70°C |
| NM93C86ALE/LZE | -40°C to +85°C |
| NM93C86ALV/LZV | -40°C to +125°C |
| Power Supply ($V_{CC}$) | 2.7V to 4.5V |

## Low $V_{CC}$ (2.7V to 4.5V) DC and AC Electrical Characteristics

| Symbol | Parameter | Part Number | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{CCA}$ | Operating Current | | CS = $V_{IH}$, SK = 250KHz | | 1 | mA |
| $I_{CCS}$ | Standby Current<br>L<br>LZ | | CS = $V_{IL}$ | | <br>10<br>1 | <br>µA<br>µA |
| $I_{IL}$ | Input Leakage | | $V_{IN}$ = 0V to $V_{CC}$ (Note 2) | | ±1 | µA |
| $I_{ILO}$ | Input Leakage<br>ORG Pin | | ORG tied to $V_{CC}$<br>ORG tied to $V_{SS}$ (Note 3) | -1<br>-2.5 | 1<br>2.5 | µA |
| $I_{OL}$ | Output Leakage | | $V_{IN}$ = 0V to $V_{CC}$ | | ±1 | µA |
| $V_{IL}$<br>$V_{IH}$ | Input Low Voltage<br>Input High Voltage | | | -0.1<br>0.8 $V_{CC}$ | 0.15 $V_{CC}$<br>$V_{CC}$ +1 | V |
| $V_{OL}$<br>$V_{OH}$ | Output Low Voltage<br>Output High Voltage | | $I_{OL}$ = 10 µA<br>$I_{OH}$ = -10 µA | <br>0.9 $V_{CC}$ | 0.1 $V_{CC}$ | V<br>V |
| $f_{SK}$ | SK Clock Frequency | | (Note 4) | 0 | 250 | KHz |
| $t_{SKH}$ | SK High Time | | | 1 | | µs |
| $t_{SKL}$ | SK Low Time | | | 1 | | µs |
| $t_{SKS}$ | SK Setup Time | | SK must be at $V_{IL}$ for $t_{SKS}$ before CS goes high | 0.2 | | µs |
| $t_{CS}$ | Minimum CS Low Time | | (Note 5) | 1 | | µs |
| $t_{CSS}$ | CS Setup Time | | | 0.2 | | µs |
| $t_{DH}$ | DO Hold Time | | | 70 | | ns |
| $t_{DIS}$ | DI Setup Time | | | 0.4 | | µs |
| $t_{CSH}$ | CS Hold Time | | | 0 | | µs |
| $t_{DIH}$ | DI Hold Time | | | 0.4 | | µs |
| $t_{PD1}$ | Output Delay to "1" | | | | 2 | µs |
| $t_{PD0}$ | Output Delay to "0" | | | | 2 | µs |
| $t_{SV}$ | CS to Status Valid | | | | 1 | µs |
| $t_{DF}$ | CS to DO in TRI-STATE | | CS = $V_{IL}$ | | 0.4 | µs |
| $t_{WP}$ | Write Cycle Time | | | | 15 | ms |

## Capacitance $T_A$ = 25°C, f = 1 MHz

| Symbol | Test | Typ | Max | Units |
|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance | | 5 | pF |
| $C_{IN}$ | Input Capacitance | | 5 | pF |

**Note 1**: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2**: Typical leakage values are in the 20 nA range.

**Note 3**: The ORG pin may draw > 1 µA when in the x8 mode ude to an internal pull-up transistor.

**Note 4**: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the $f_{SK}$ $f_{SK}$ parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both $t_{SKH}$ and $t_{SKL}$ limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

**Note 5**: CS (Chip Select) must be brought low (to $V_{IL}$) for an interval of $t_{CS}$ in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

## AC Test Conditions

| $V_{CC}$ Range | $V_{IL}/V_{IH}$ Input Levels | $V_{IL}/V_{IH}$ Timing Level | $V_{OL}/V_{OH}$ Timing Level | $I_{OL}/I_{OH}$ |
|---|---|---|---|---|
| 2.7V ≤ $V_{CC}$ ≤ 5.5V (Extended Voltage Levels) | .03V/1.8V | 1.0V | 0.8V/1.5V | ±10µA |
| 4.5V ≤ $V_{CC}$ ≤ 5.5V (TTL Levels) | 0.4V/2.4V | 1.0V/2.0V | 0.4V/2.4V | -2.1mA/0.4mA |
| Output Load: 1 TTL Gate ($C_L$ = 100 pF) | | | | |

## MICROWIRE I/O Pin Description

### Chip Select (CS):

This pin enables and disables the MICROWIRE device and performs 3 general functions:

1. When in the low state, the MICROWIRE device is disabled and the output tri-stated (high impedance). If this pin is brought high (rising edge active), all internal registers are reset and the device is enabled, allowing MICROWIRE communication via DI/DO pins. To restate, the CS pin must be held high during all device communication and opcode functions. If the CS pin is brought low, all functions will be disabled and reset when CS is brought high again. The exception to this is when a programming cycle is initiated (see 2 and 3). Again, all activity on the CS, DI and DO pins is ignored until CS is brought high.
2. After entering all required opcode and address data, bringing CS low initiates the (asynchronous) programming cycle.
3. When programming is in progress, the Data-Out pin will display the programming status as either BUSY (DO low) or READY (DO high) when CS is brought high. (Again, the output will be tri-stated when CS is low.) To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affect the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits.

### Serial Clock (SK):

This pin is the clock input (rising edge active) for clocking in all opcodes and data on the DI pin and clocking out all data on the DO pin.However, this pin has no effect on the asynchronous programming cycle (see the CS pin section) as the BUSY/READY status is a function of the CS pin only.

### Data-In (DI):

All serial communication into the device is performed using this input pin (rising edge active). In order to avoid false Start Bits, or related issues, it is advised to keep the DI pin in the low state unless actually clocking in data bits (Start Bit, Opcode, Address or incoming data bits to be programmed). Please note that the first '1' clocked into the device (after CS is brought high) is seen as a Start Bit and the beginning of a serial command string, so caution must be observed when bringing CS high.

### Data-Out (DO):

All serial communication out of the device (READ opcode) is performed using this output pin (rising edge active) as well as indicating the READY/BUSY status duting the asynchronous programming cycle. Note that, during READ operations, the output data is clocked out after the last address bit (A0) is clocked in. If a 3-wire application is required (where DI and DO are tied together), sections in AN-758, or related application notes, must be followed for correct operation.

### Organization (ORG):

This pin controls the device architecture (8-bit data word vs. 16-bit data word). If the ORG pin is brought to $V_{CC}$, the device is configured with a 16-bit data word and if the ORG pin is brought to $V_{SS}$ (Ground), the device is configured with an 8-bit data word (refer to other sections for details of both configurations). If the ORG pin is left floating, the device will default to a 16-bit data word.

## Instruction Set for the NM93C86A

| Device | ORG Pin Logic | Memory | |
|---|---|---|---|
| | | Configuration | # of Address Bits |
| NM93CC86A | 0 | 2048 x 8 | 11 bits |
| | 1 | 1024 x 16 | 10 Bits |

## 1024 by 16-Bit Organization (NM93C86A when ORG = $V_{CC}$ or NC)

| Instruction | SB | Op Code 2 Bits | Address 10 Bits | Data 16 Bits | Function |
|---|---|---|---|---|---|
| READ | 1 | 10 | A9–A0 | | Read data stored in selected registers. |
| EWEN | 1 | 00 | 11XXXXXXXX | | Enables programming modes. |
| EWDS | 1 | 00 | 00XXXXXXXX | | Disables all programming modes. |
| ERASE | 1 | 11 | A9–A0 | | Erases selected register. |
| WRITE | 1 | 01 | A9–A0 | D15–D0 | Writes data pattern D15–D0 into selected registers. |
| ERAL | 1 | 00 | 10XXXXXXXX | | Erases all registers. |
| WRAL | 1 | 00 | 01XXXXXXXX | D15–D0 | Writes data pattern D15–D0 into all registers. |

## 2048 by 8-Bit Organization (NM93C86A when ORG = GND)

| Instruction | SB | Op Code 2 Bits | Address 11 Bits | Data 8 Bits | Function |
|---|---|---|---|---|---|
| READ | 1 | 10 | A10–A0 | | Read data stored in selected registers. |
| EWEN | 1 | 00 | 11XXXXXXXXX | | Enables programming modes. |
| EWDS | 1 | 00 | 00XXXXXXXXX | | Disables all programming modes. |
| ERASE | 1 | 11 | A10–A0 | | Erases selected register. |
| WRITE | 1 | 01 | A10–A0 | D7–D0 | Writes data pattern D7–D0 into selected registers. |
| ERAL | 1 | 00 | 10XXXXXXXXX | | Erases all registers. |
| WRAL | 1 | 00 | 01XXXXXXXXX | D7–D0 | Writes data pattern D7–D0 into all registers. |

# Functional Description

## Programming

The programming cycle for both devices is automatically started after entering the D0 data bit; independent of the status of the CS input pin. This feature allows a programming instruction (ERASE/WRITE/ERAL/WRAL) to be cancelled at any time before entering the last data bit (D0). This is accomplished by forcing the CS input pin low (for $t_{CS}$) at any time before the D0 data bit is clocked in. Note that the CS input pin can be brought low after the D0 bit is clocked in, to maintain compatibility with the other family members, but is not necessary to start a programming cycle.

In all programming modes the READY/BUSY status of the device can be determined by polling the DO pin. After clocking in the last bit of the instruction sequence and with the CS held "high", the DO pin will exit the high impedance state and indicate the READY/BUSY status of the device. DO = logical "0" indicates that programming is still in progress and no other instruction can be executed. DO = logical "1" indicates that the device is READY for another instruction. If CS is forced "low" the DO pin will return to the high impedance state. After the programming cycle has been completed and DO = logical "1", the DO pin can be reset back to the high impedance state by clocking a logical "1" into the DI pin. (This is also performed with the start bit on all op codes, thus clocking an instruction has the same effect.)

## Read (READ)

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the serial data output string. Output data changes are initiated by a low to high transition of SK clock after the last address bit (A0) is clocked in.

## Erase/Write Enable (EWEN)

When $V_{CC}$ is applied to the part, it "powers up" in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or $V_{CC}$ is removed from the part.

## Functional Description (Continued)

### Erase/Write Disable (EWDS)

To protect against accidental data overwrites, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

### Erase (ERASE)

The ERASE instruction will program all bits in the specified register to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last address bit (A0) is clocked in. At this point CS, SK and DI become don't care states. After starting an Erase cycle the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased.

### Write (WRITE)

The WRITE instruction is followed by 16 bits of data (or 8 bits of data when using the NM93C86A in the x8 organization) to be written into the specified address. Note that if the CS is brought "low" before clocking in all of the data bits, then the WRITE instruction will be aborted. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last data bit (D0) is clocked in. At this point, CS, SK and DI become don't care states. No separate ERASE cycle is required before a WRITE instruction.

As in the ERASE instruction, after starting a WRITE cycle, the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been written and that the part is ready for another instruction.

### Erase All (ERAL)

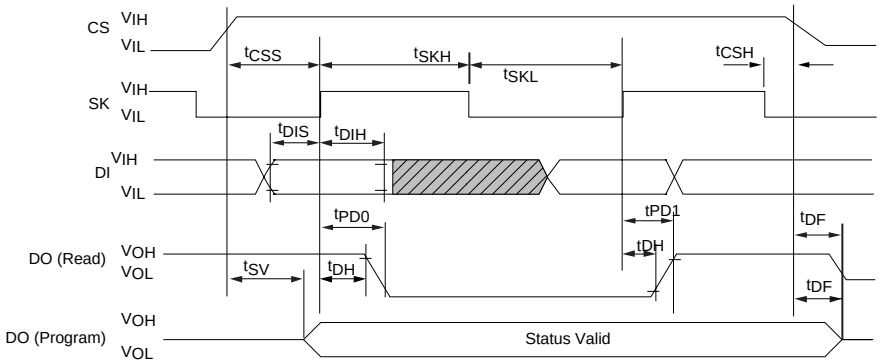
The ERAL instruction will simultaneously program all registers in the memory array to the logical "1" state.

### Write All (WRAL)

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

## Timing Diagrams for the NM93C86A

### Synchronous Data Timing

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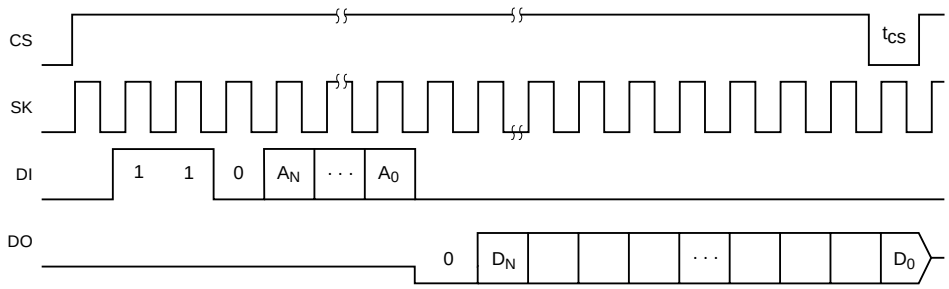
## Organization of Address and Data Fields for the NM93C86A

| ORG | Organization | $A_N$ | $D_N$ |
|---|---|---|---|
| $V_{CC}$ or NC | 1024 x 16 | A9 | D15 |
| $V_{SS}$ | 2048 x 8 | A10 | D7 |

### READ

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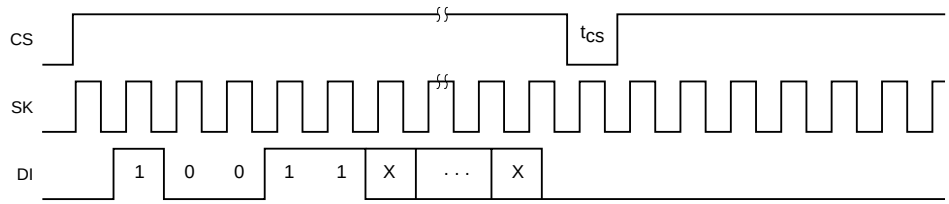
## Timing Diagrams for the NM93C86A (Continued)

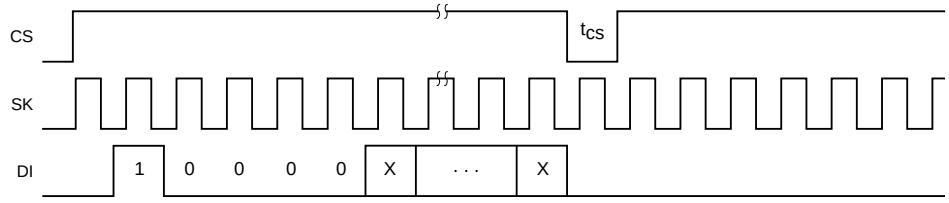
### EWEN
### DO = TRI-STATE




ORG = $V_{CC}$, 8 X's
ORG = $V_{SS}$, 9 X's

DS011254-5

### EWDS
### DO = TRI-STATE




ORG = $V_{CC}$, 8 X's
ORG = $V_{SS}$, 9 X's

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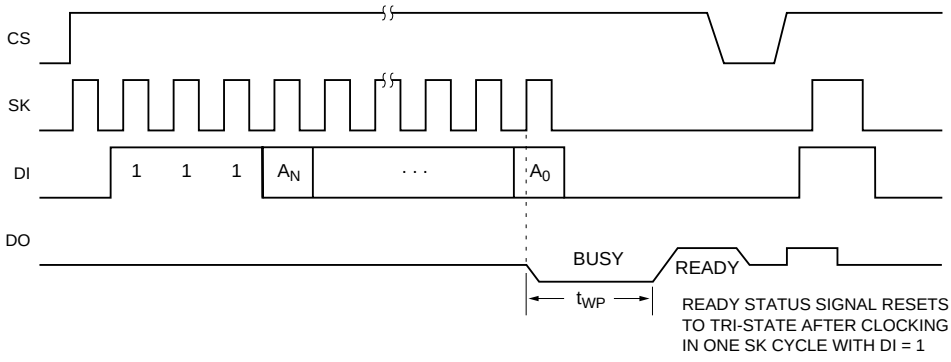
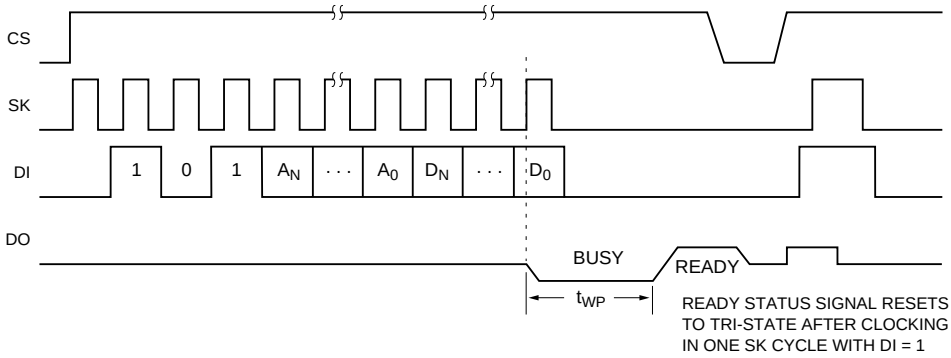
### ERASE




READY STATUS SIGNAL RESETS
TO TRI-STATE AFTER CLOCKING
IN ONE SK CYCLE WITH DI = 1

DS011254-7

### WRITE

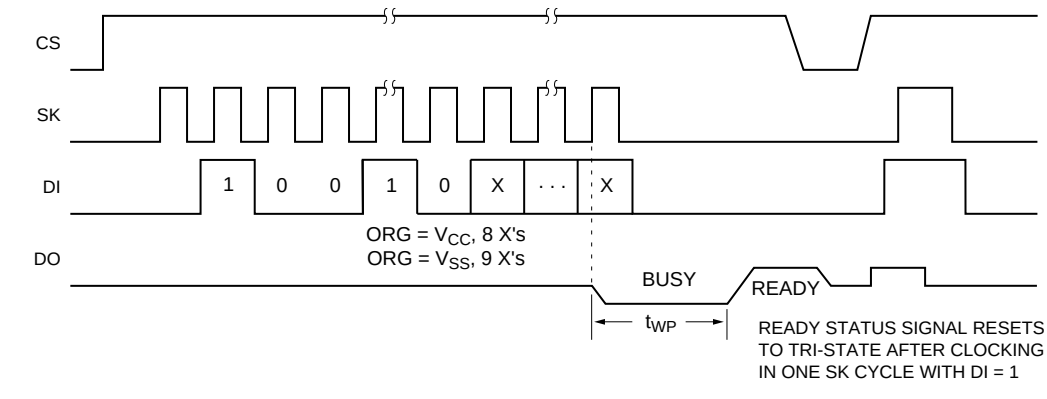



READY STATUS SIGNAL RESETS
TO TRI-STATE AFTER CLOCKING
IN ONE SK CYCLE WITH DI = 1

DS011254-8

## Timing Diagrams for the NM93C86A (Continued)

### ERAL

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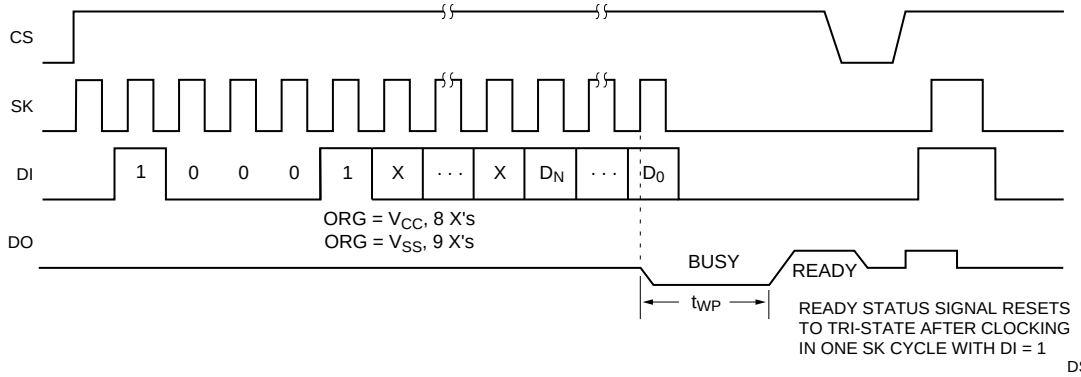
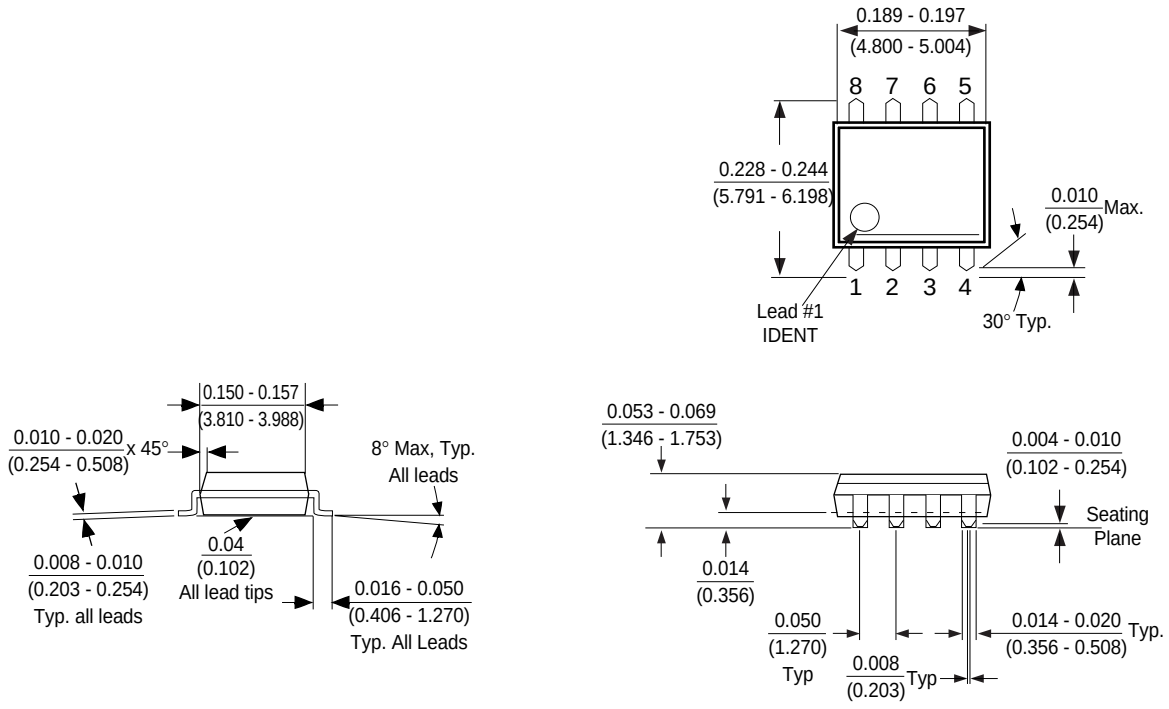
### WRAL



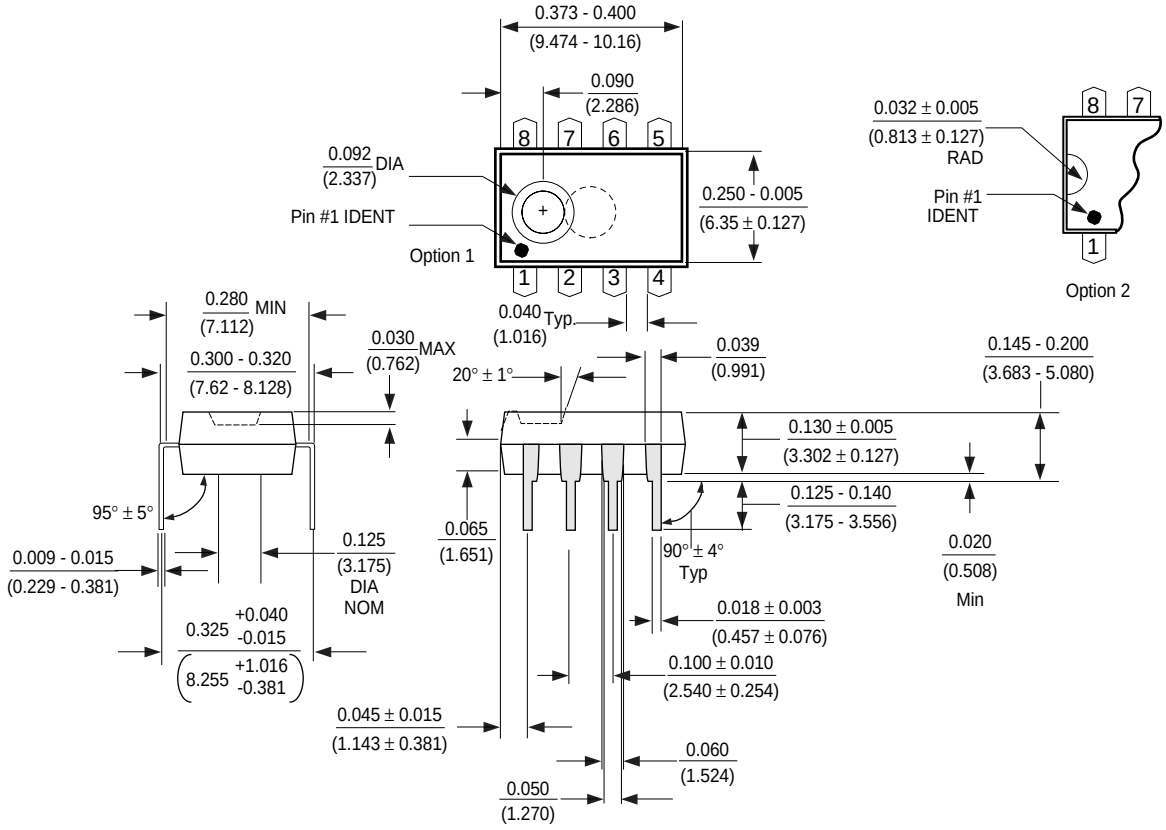

DS011254-10

**Physical Dimensions** inches (millimeters) unless otherwise noted




**Molded Small Outline Package (M8)**
**Package Number M08A**

## Physical Dimensions inches (millimeters) unless otherwise noted




**Molded Dual-in-Line Package (N)**
**Package Number N08E**

## Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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