FAIRCHILD SEMICONDUCTOR™

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NM93C56
2048-Bit Serial EEPROM (MICROWIRE™ Bus Interface)

General Description

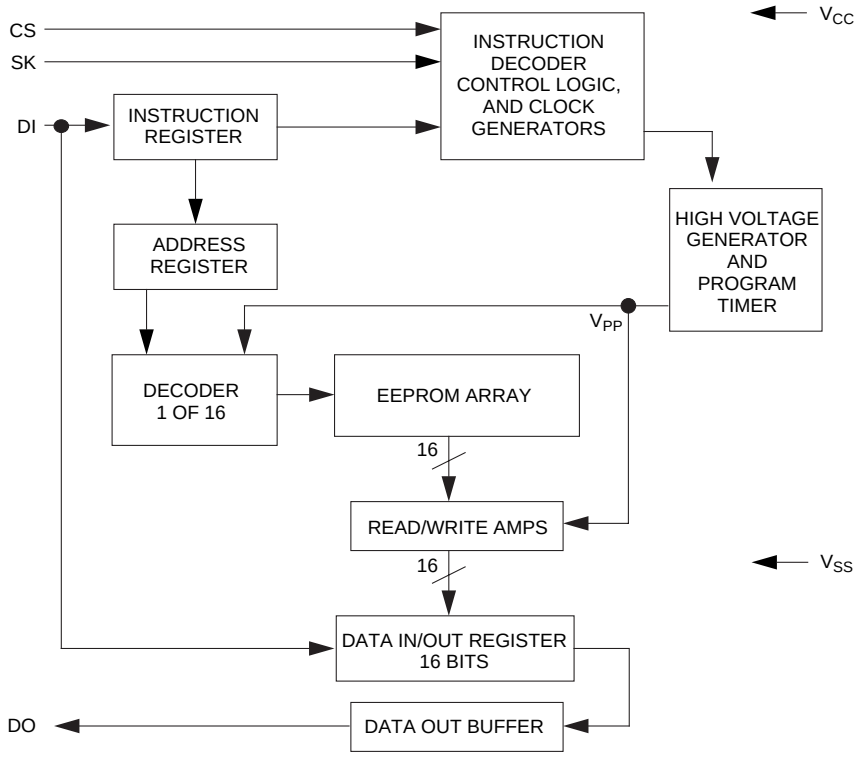
The NM93C56 devices are 2048 bits of CMOS non-volatile electrically erasable memory divided into 128 16-bit registers. They are fabricated using Fairchild Semiconductor's floating-gate CMOS process for high reliability, high endurance and low power consumption. These memory devices are available in an 8-pin SOIC or 8-pin TSSOP package for small space considerations.

The serial interface that operates this EEPROM is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions which control this device: Read, Write Enable, Erase, Erase All, Write, Write All, and Write Disable. The ready/busy status is available on the DO pin to indicate the completion of a programming cycle.

Features

- Device status during programming mode
- Typical active current of 200µA
  10µA standby current typical
  1µA standby current typical (L)
  0.1µA standby current typical (LZ)
- No erase required before write
- Reliable CMOS floating gate technology
- 2.7V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP
- Schmitt Trigger inputs and V_{CC} lock-out to prevent data corruption.

Block Diagram



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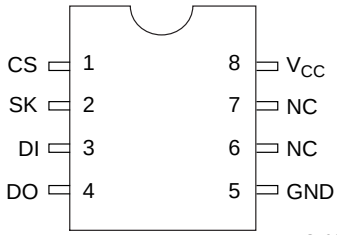
Connection Diagrams

Dual-In-Line Package (N), 8-Pin SO (M8) and 8-Pin TSSOP (MT8)



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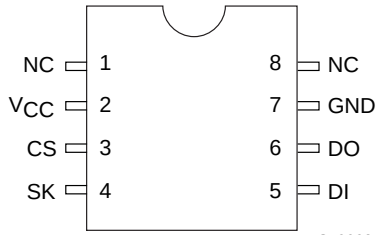
Top View
See Package Number
N08E, M08A and MTC08

Rotated Die (93C56T)



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Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

NM 93 C XX T LZ E XX

	Letter	Description
Package	N	8-Pin DIP
	M8	8-Pin SO8
	MT8	8-Pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
	Blank	Normal Pin Out
	T	Rotated Die Pin Out
Density	56	2K
	C	CMOS
	CS	Data protect and sequential read
Interface	93	MICROWIRE - 3 or 4 Wire Interface
	NM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C56	0°C to +70°C
NM93C56E	-40°C to +85°C
NM93C56V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 1MHz		1	mA
I_{CCS}	Standby Current		CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1mA I_{OH} = -400 µA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} -0.2	0.2	V V
f_{SK}	SK Clock Frequency		(Note 3)	0	1	MHz
t_{SKH}	SK High Time	NM93C56 NM93C56E/V		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 4)	250		ns
t_{CSS}	CS Setup Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time	NM93C56 NM93C56E/V		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"				500	ns
t_{PD0}	Output Delay to "0"				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C56L/LZ	0°C to +70°C
NM93C56LE/LZE	-40°C to +85°C
NM93C56LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency		(Note 3)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 4)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		µs
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Functional Description

The NM93C56 device has 7 instructions as described below. Note that the MSB of any instruction is a “1” and is viewed as a start bit in the interface sequence. The next 10 bits carry the op code and the 8-bit address for register selection.

Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Write Enable (WEN):

When V_{CC} is applied to the part, it 'powers-up' in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until aWrite Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical “1” state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum time of t_{CS}. DO = logical “0” indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by the 16 bits of data to be written into the specified address. After the last bit of data is put in the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical “1” state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: The Fairchild CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" and "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

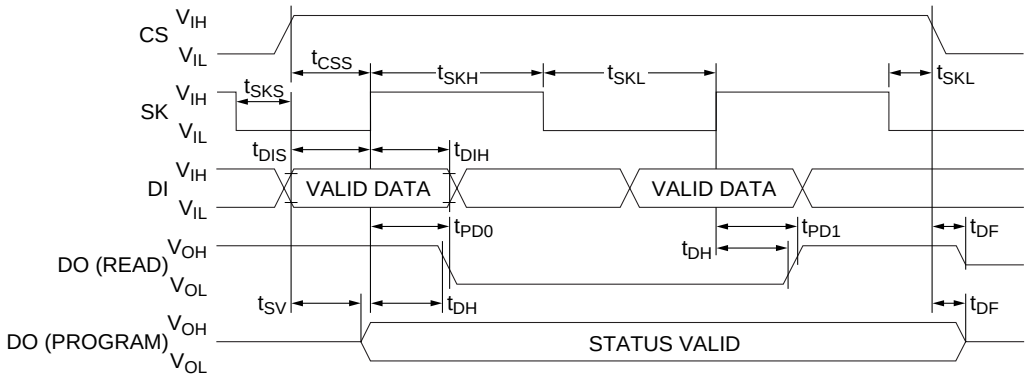
Instruction Set for the NM93C56

Instruction	SB	Op. Code	Address	Data	Comments
READ	1	10	A7-A0		Reads data stored in memory, at specified address.
WEN	1	00	11xxxxxx		Write enable must precede all programming modes.
ERASE	1	11	A7-A0		Erase selected register.
WRITE	1	01	A7-A0	D15-D0	Writes selected register.
ERAL	1	00	10xxxxxx		Erases all registers.
WRALL	1	00	01xxxxxx	D15-D0	Writes all registers.
WDS	1	00	00xxxxxx		Disables all programming instructions.

Note: A7 is "don't care."

Timing Diagrams

Synchronous Data Timing



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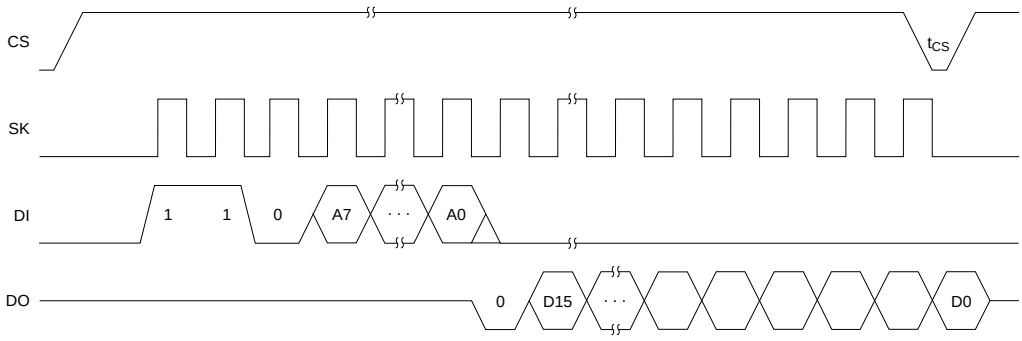
READ



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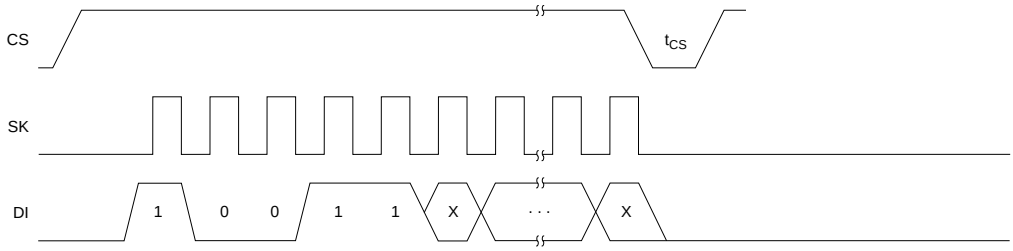
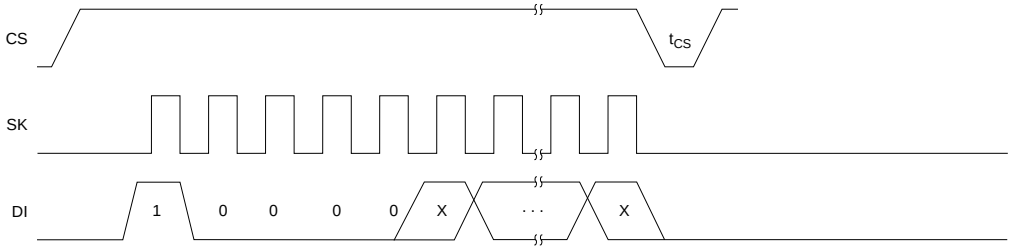
WEN



DS500081-6

WDS



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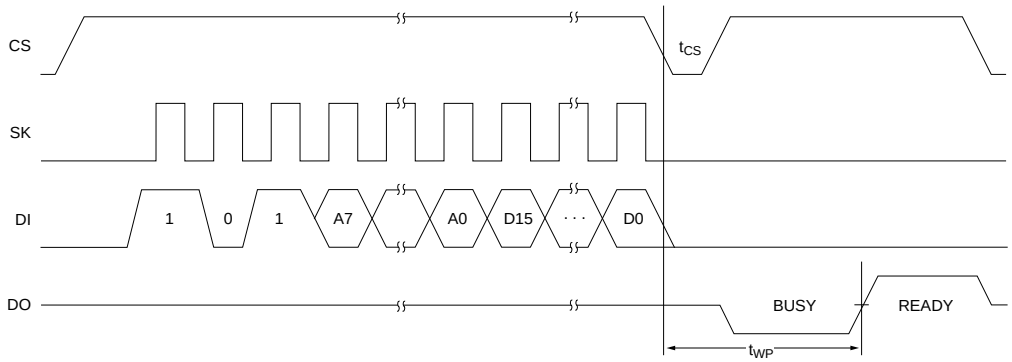
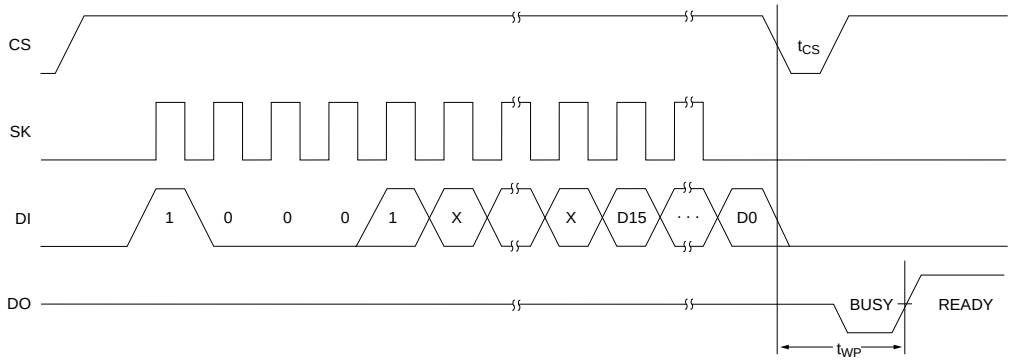
Timing Diagrams (Continued)

WRITE



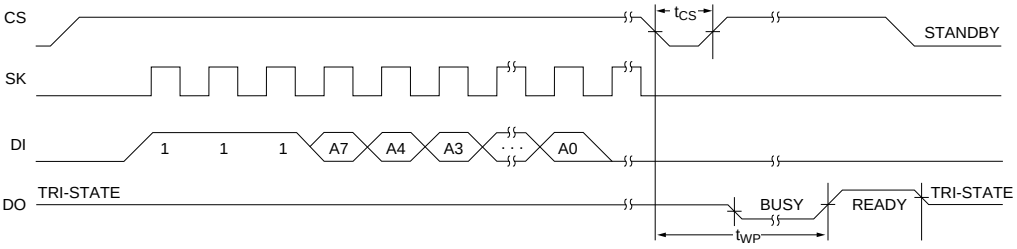
DS500081-8

WRALL



DS500081-9

ERASE



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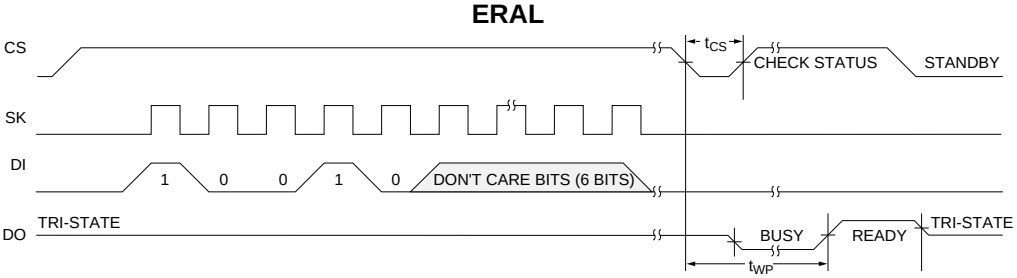
ERAL



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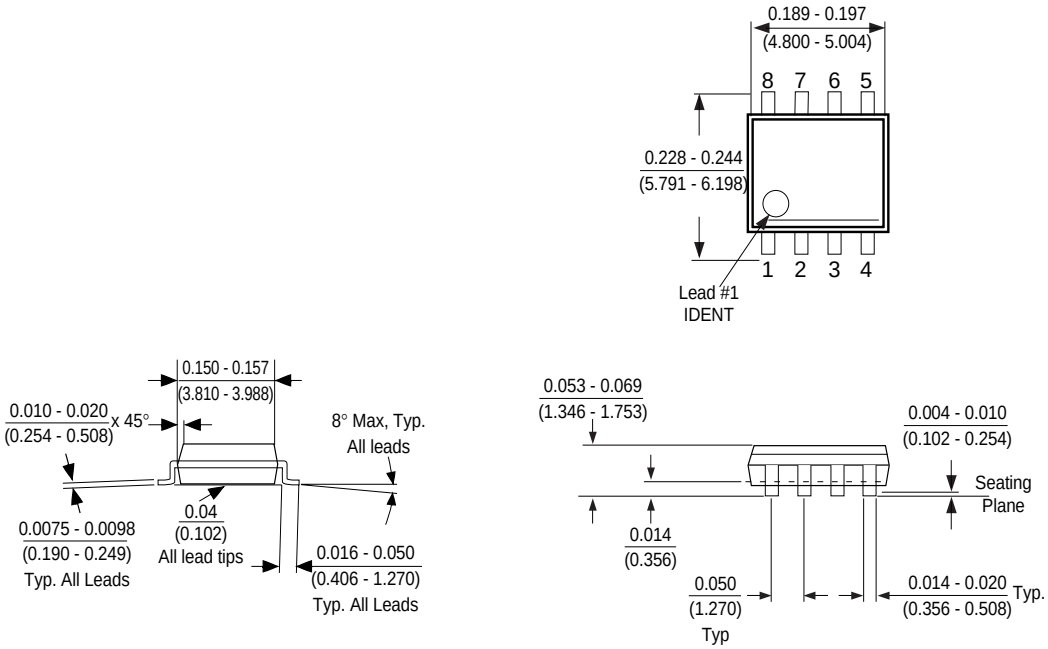
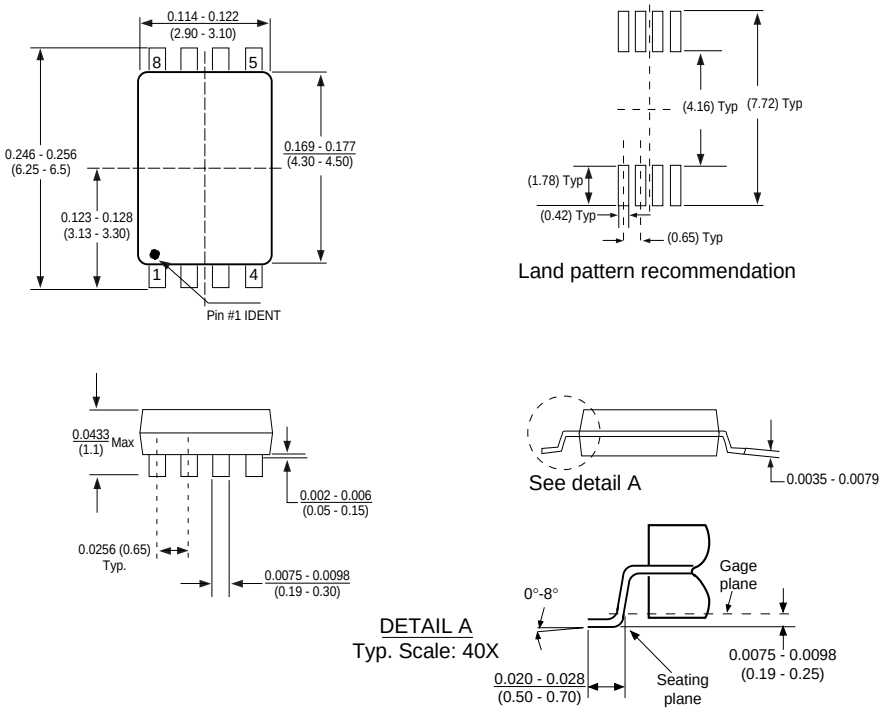
Physical Dimensions inches (millimeters) unless otherwise noted



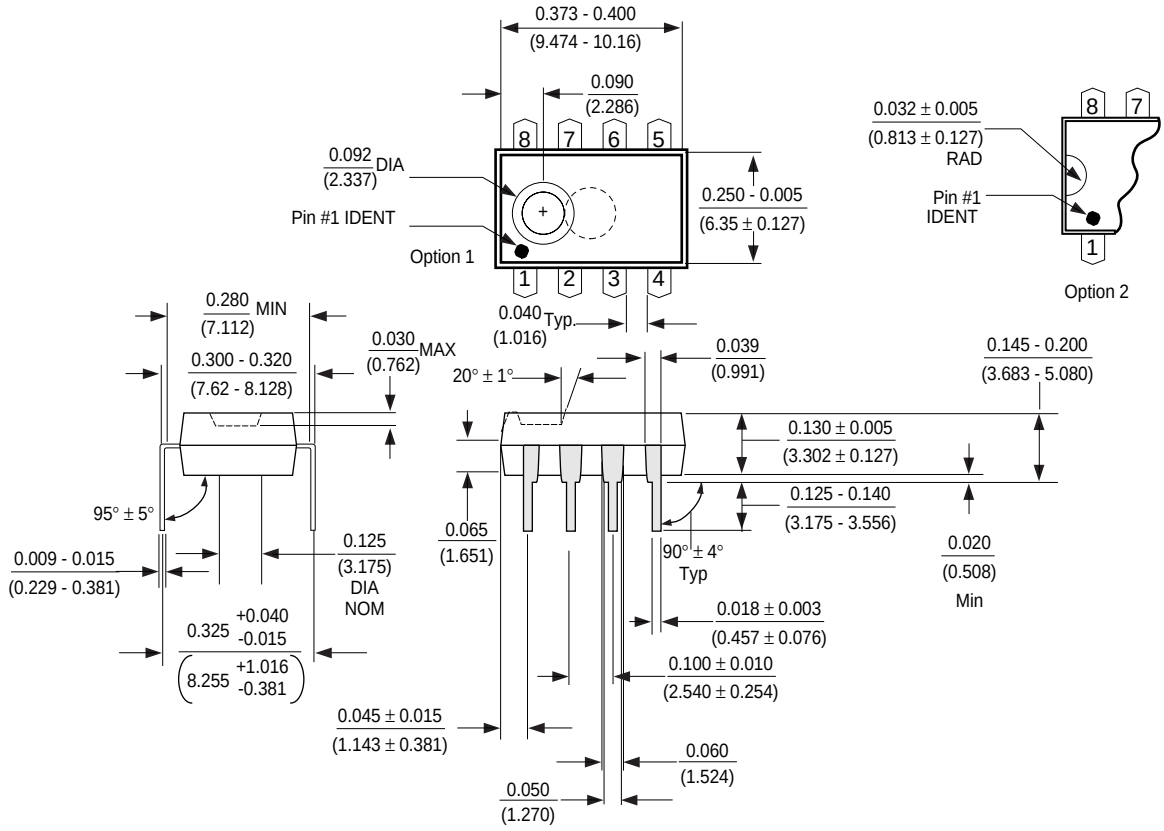
Molded Small Out-Line Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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