FAIRCHILD
SEMICONDUCTOR™

July 1998

NM27C520
524,288-Bit (64K x 8) Multiplexed Addresses/Outputs OTP CMOS EPROM

General Description

The NM27C520 is a high performance 512K CMOS one-time programmable read only memory (EPROM) manufactured using Fairchild's proprietary CMOS AMG™ EPROM technology for an excellent combination of speed and economy while providing excellent reliability. It incorporates latches for the 8 lower order address bits to multiplex with the 8 data bits. This minimizes chip count, reduces cost, and simplifies the design of multiplexed bus systems.

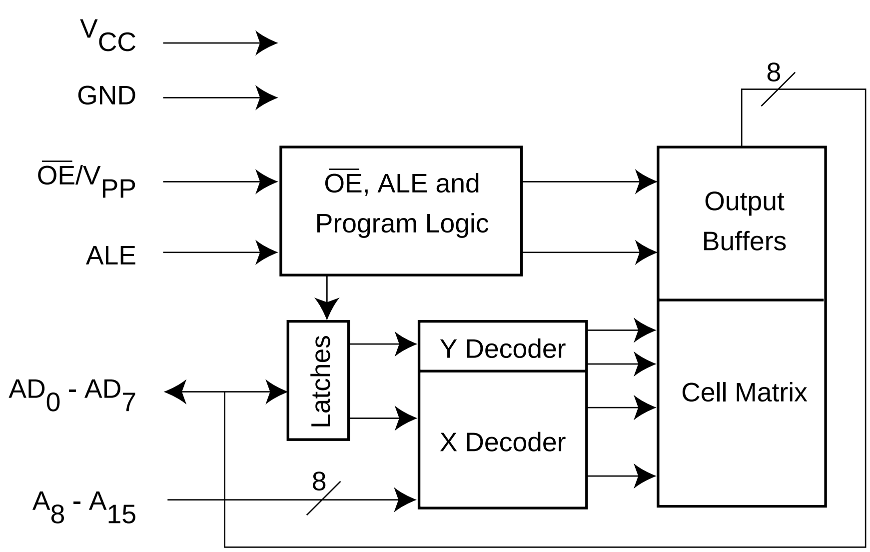
The NM27C520 provides microprocessor-based systems storage capacity for portions of operating system and application software. Its 90ns access time provides no wait-state operation with high-performance CPUs. The NM27C520 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The NM27C520 is one member of a high density EPROM Family which range in densities up to 4 Megabit.

Features

- 8-Bit multiplexed Addresses/Outputs
- High performance CMOS —
  - 90 ns access time
- Fast turn-off for microprocessor compatibility
- Manufacturers identification code
- JEDEC Standard Pin Configuration
  - 20-Lead SOIC package

Block Diagram



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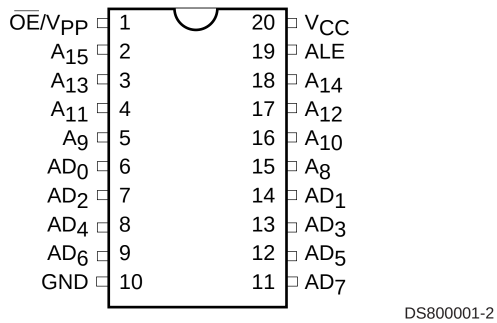
Connection Diagram



SOIC Top View

Commercial Temp. Range (0°C to + 70°C)

V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns) (Note 1)
NM27C520M 90	90

Industrial Temp. Range (-40°C to + 85°C)

V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns) (Note 1)
NM27C520ME 90	90

Note 1: All versions are guaranteed to function for slower speeds.

Package Type:

M=Wide Bodied SOIC

Pin Names

	Addresses/Outputs
AD_0-AD_7	Address/Data
A_8-A_{15}	Address
ALE	Address Latch Enable
OE/V_{PP}	Output Enable

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
All Input Voltage except A9 with Respect to Ground	-2.0V to +7V
V_{PP} and A9 with Respect to Ground	-2.0V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection (MIL Std. 883, Method 3015.2)	>2000V
All Output Voltages with Respect to Ground	V_{CC} +1.0V to GND -0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	-40°C to +85°C	+5V	±10%

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V
I_{CC}	V_{CC} Active Current	I_{OUT} = 0 mA, f = 5 MHz		20	mA
I_{CC2}	V_{CC} Standby Current	ALE = V_{IH}		2	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}		10	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} - 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	-1	1	µA
I_{LI2}	Input Load Current A13	V_{IN} = 5.5V or GND	-100	100	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	-5	5	µA

Read Operation

AC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
t_{ACC}	Address to Output Delay		90	ns
t_{ALE}	Address Latch Enable Width	45		ns
t_{OE}	OE to Output Delay		35	ns
t_{DF}	Output Disable to Output Float		25	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever Occurred First	0		ns
t_{AS}	Address Setup Time	15		ns
t_{AH}	Address Hold Time	15		ns

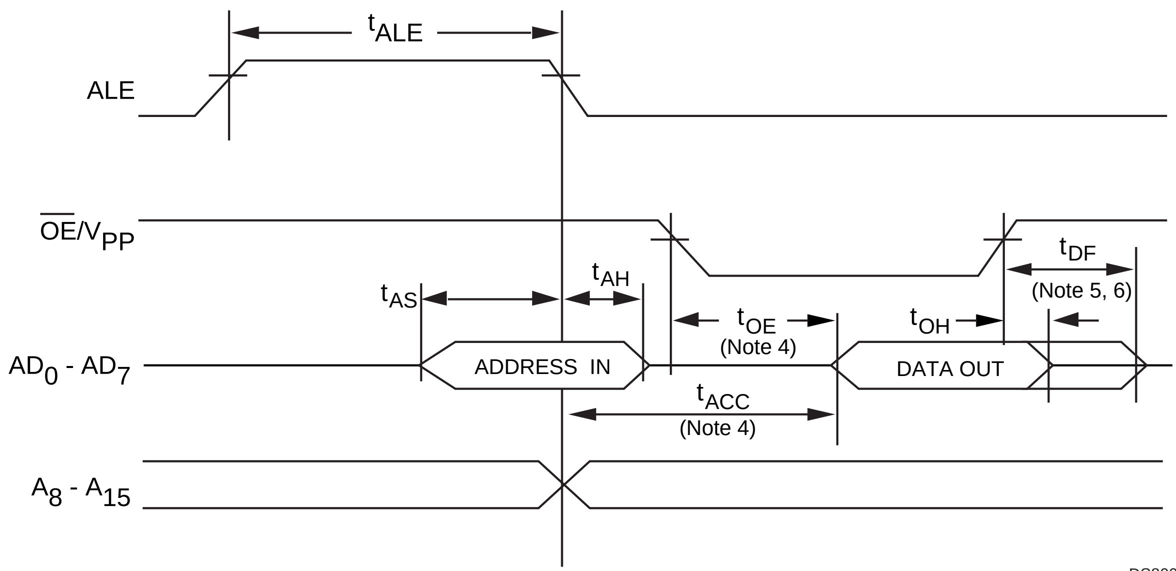
Capacitance T_A = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and CL = 100 pF (Note 9)
Input Rise and Fall Times	≤ 20 ns (10% to 90%)
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level (Note 9)	
Inputs	0.8V and 2.0V
Outputs	0.8V and 2.0V

AC Waveforms for Read Operation (Notes 7 and 8)



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Note 2: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to t_{ACC}- t_{OE} after the falling edge of ALE without impacting t_{ACC}.

Note 5: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) -0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V.

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L: 100 pF includes fixture capacitance.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

DC Programming Characteristics (Notes 11 & 12)

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 2.5V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$ (Note 13)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Level		-0.6		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4			V
I_{CC}	V_{CC} Supply Current				25	mA
I_{CC2}	V_{CC} Standby Current	ALE = V_{IL}			2.5	mA
I_{PP}	$\overline{OE}/V_{PP}$ Current	ALE = V_{IH}			25	mA
I_{LI}	Input Load Current	$V_{IN} = V_{IL}$ or V_{IH}	-10		10	µA
I_{LI2}	Input Load Current A13	$V_{IN} = V_{IL}$ or V_{IH}	-100		100	µA

AC Programming Characteristics (Notes 11 & 12)

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 2.5V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$ (Note 13)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{ALE}	Address Latch Enable Width		500			ns
t_{LAS}	Latched Address Setup Time		100			ns
t_{LAH}	Latched Address Hold Time		100			ns
t_{AS}	Address Setup Time		2			µs
t_{AH}	Address Hold Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{DH}	Data Hold Time		2			µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2			µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2			µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time during Programming		50			ns
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2			µs
t_{PW}	Program Pulse Width		45	50	105	µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{LP}	ALE Low to $\overline{OE}/V_{PP}$ High Voltage Delay		2			µs
t_{OE}	Data Valid from $\overline{OE}/V_{PP}$			150		ns
t_{DFP}	$\overline{OE}/V_{PP}$ High to Output Float Delay (Note 14)		0	130		ns

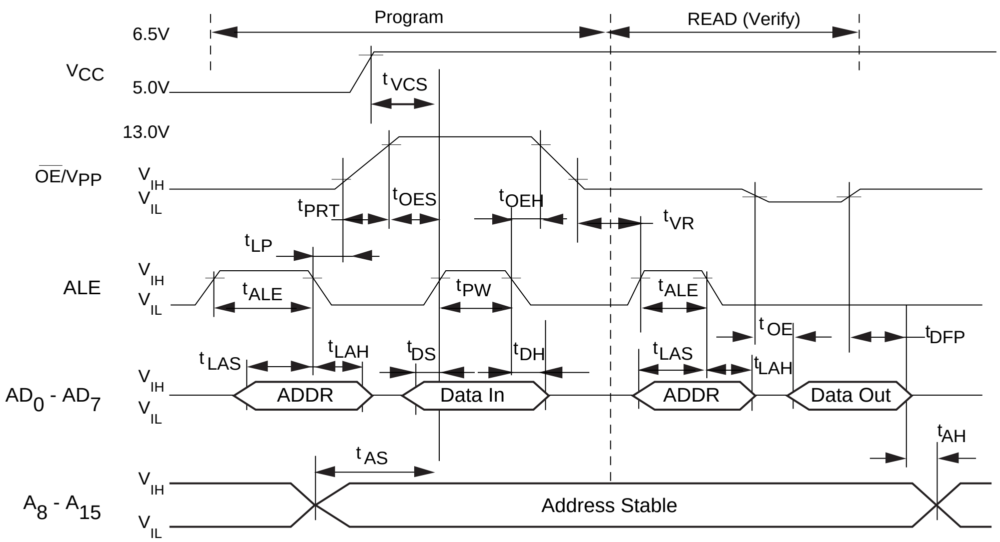
Note 11: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: This parameter is not 100% tested. Output Float is defined as the point where data is no longer driven. See timing diagram (page 6).

Programming Waveforms



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Note 15: The input timing reference is 0.8V for V_{IL} and 2.0V for V_{IH}.

Note 16: t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Turbo Programming Algorithm Flow Chart

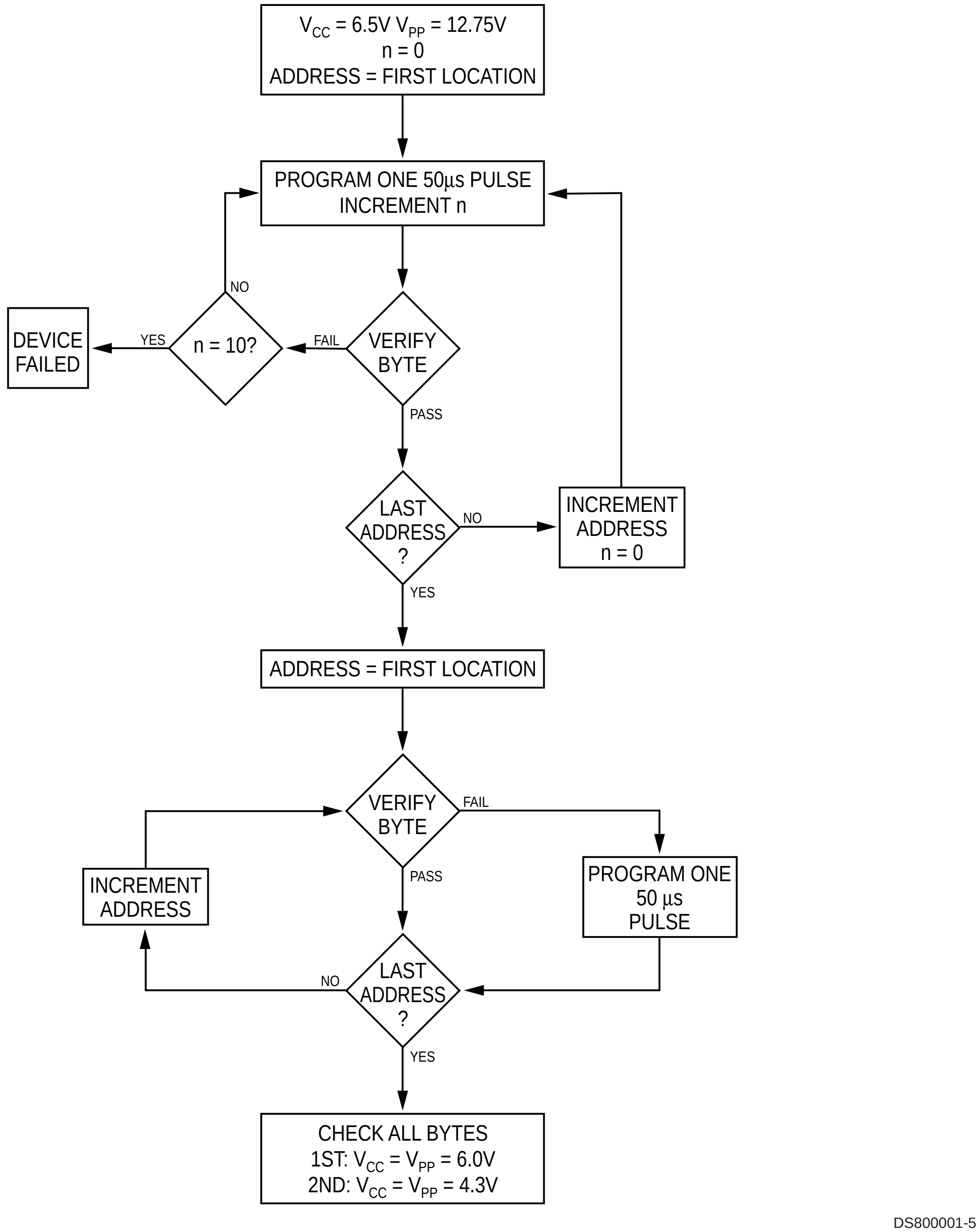


Figure 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and $\overline{OE}/V_{PP}$. The $\overline{OE}/V_{PP}$ power supply must be at 12.75V during the two programming modes, and must be at 5V in the other four modes. The V_{CC} power must be at 6.5V during the two programming modes, and at 5V in the other four modes.

Read Mode

The NM27C520 has two control pins which are used to read data on the output pins. Address Latch Enable (ALE) is pulsed to read address pins AD_0 - AD_7. On the falling edge of this pulse, the data on these pins are latched into memory. When the address pins A_8 - A_{15} are stable and output enable ($\overline{OE}$) is low, the data contained in the desired address location is gated to pins AD_0 - AD_7. Address access time (t_{ACC}) is either the time delay from address latch enable, or the time delay from when the address pins A_8 - A_{15} are stable, which ever happens last. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to drive data to the output pins.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 90%, from 110mW to less than 11mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the ALE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that ALE be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 ($\overline{OE}/V_{PP}$) will damage the EPROM.

Initially, all bits of the EPROM are in the “1’s” state. Data is introduced by selectively programming “0’s” into the desired bit locations. Although only "0’s" will be programmed, both “1’s” and “0’s” can be presented in the data word. It is not possible to change a “0” to a “1”.

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ power supply is at 12.75V. It is required that at least a 0.1 µF capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming mode can be accomplished after a TTL high pulse is applied to the ALE input latching in the addresses AD_0 - AD_7 by its falling edge. Once addresses A_8 - A_{15} are stable, the $\overline{OE}/V_{PP}$ power supply is set to 12.75V and a TTL high pulse is again applied to the ALE input. In order to program the entire memory array, a program pulse must be applied at each address location in this same manner.

The EPROM is programmed with the Turbo Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse.

The EPROM must not be programmed with a DC signal applied to the ALE input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A high level TTL pulse applied to the ALE input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for ALE all like inputs (including $\overline{OE}/V_{PP}$) of the parallel EPROM may be common. A TTL high level program pulse applied to an EPROM’s ALE input with $\overline{OE}/V_{PP}$ at 12.75V will program that EPROM. A TTL low level ALE input inhibits the other EPROMs from being programmed.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer’s identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer’s Identification code, shown in Table 2, specifically identifies the manufacture and device type. The code for NM27C520 is '8F9D', where '8F' designates that it is made by Fairchild Semiconductor, and '9D' designates the 520 part.

The code is accessed by applying 12V ± 0.5V to address pin A_9. Addresses AD_1 - A_8, A_{10}-A_{16}, and all control pins are held at V_{IL}.

Address pin A_8 is held at V_{IL} for the manufacturer’s code, and held at V_{IH} for the device code. The code is read on the eight data pins, AD_0- AD_7. Proper code access is only guaranteed at 25°C ± 5°C.

Mode Selection

The modes of operation of the NM27C520 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A_9 for device signature.

Table 1. Mode Selection

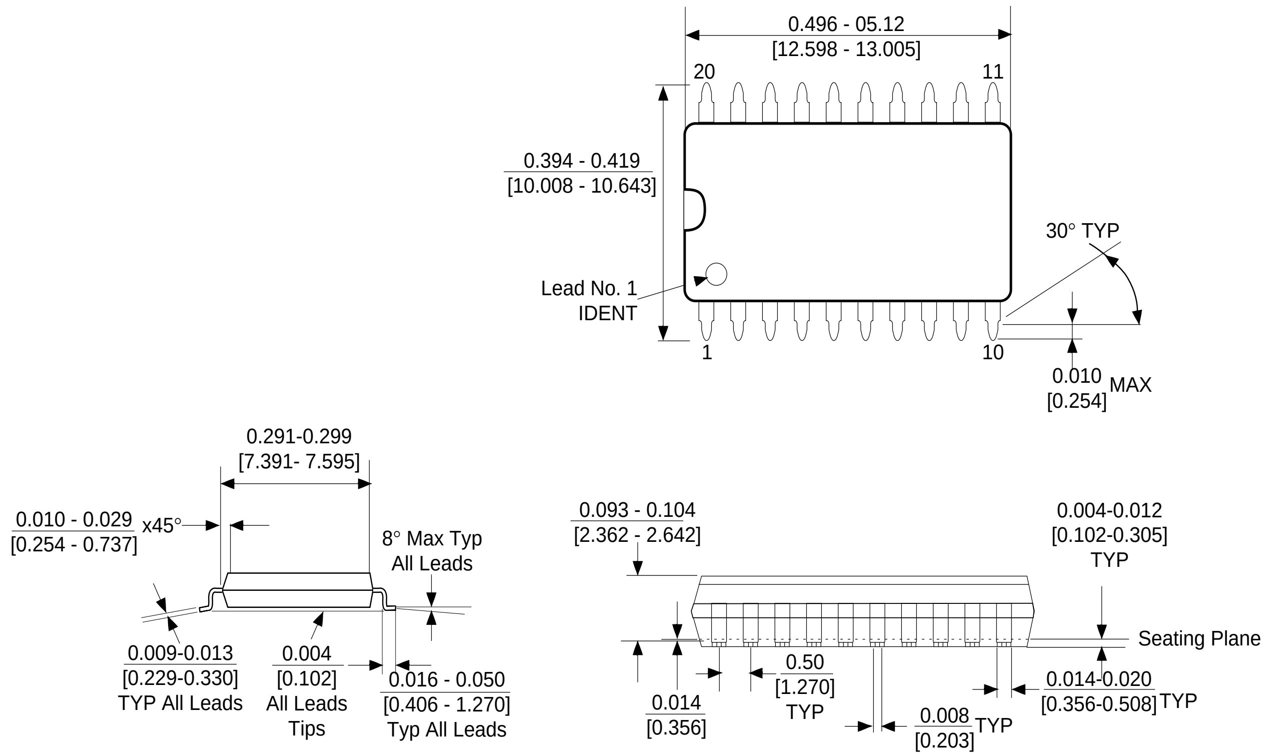
Mode \ Pins	ALE	$\overline{OE}/V_{PP}$	A_8 - A_{15}	AD_0 - AD_7
Read	V_{IL}	V_{IL}	A_{IN}	D_{OUT}
Output Disable	V_{IL}/V_{IH}	V_{IH}	A_{IN}	High Z/A_{IN}
Standby	V_{IH}	X	A_{IN}	A_{IN}
Address Latch Enable	‾‾╲__	V_{IH}	A_{IN}	A_{IN}
Programming	V_{IH}	12.75V	A_{IN}	D_{IN}
Program Inhibit	V_{IL}	12.75V	A_{IN}	High Z

Note 17: ‾‾╲__ = High to Low Transition, A_{IN} = Address In, D_{OUT} = Data Out, D_{IN} = Data In

Table 2. Manufacturer's Identification Code

Mode \ Pins	A_9	A_8	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0	Hex Data
Manufacturer Code	V_{PP}	0	1	0	0	0	1	1	1	1	8F
Device Code	V_{PP}	1	1	0	0	1	1	1	0	1	9D

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
Order Number NM27C520
Package Number M20B

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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