FAIRCHILD SEMICONDUCTOR™

February 1999

NM24C16/17 – 16,384-Bit Standard 2-Wire Bus Interface Serial EEPROM

General Description

The NM24C16/17 devices are 16,384 bits of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I²C™ 2-wire protocol and are designed to minimize device pin count, and simplify PC board layout requirements.

The upper half of the memory of the 24C17 can be disabled (Write Protected) by connecting the WP pin to V_{CC}. This section of memory then becomes unalterable unless WP is switched to V_{SS}.

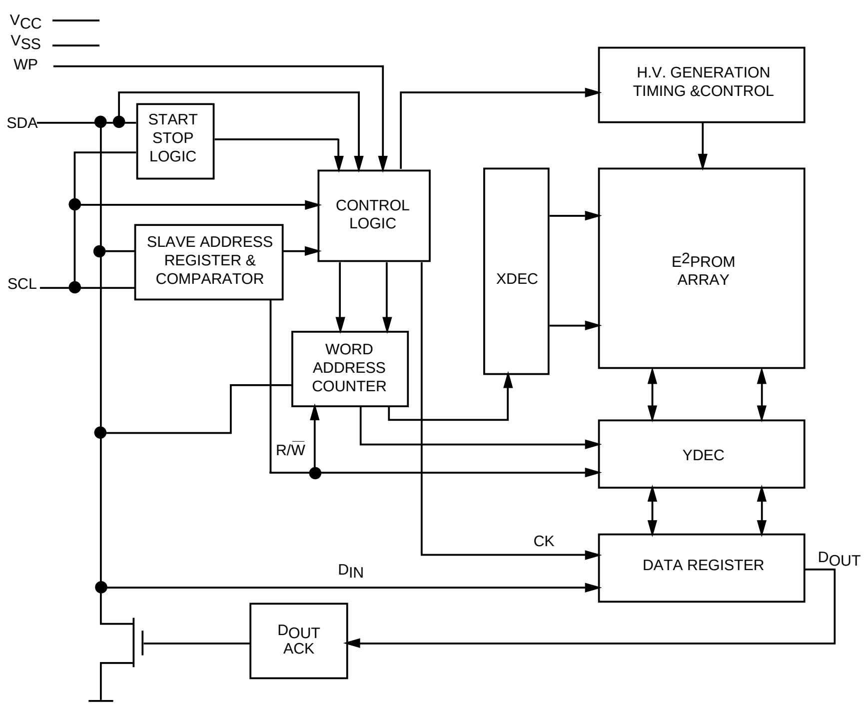
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the Fairchild family in 2K, 4K, 8K, and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K). For devices with densities greater than 16K, a different protocol is used. Refer to 32K or higher densities for additional details.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended operating voltage 2.7V – 5.5V
- 400 kHz clock frequency (F) at 2.7V - 5.5V
- 500µA active current typical
  10µA standby current typical
  1µA standby typical (L)
  0.1µA standby typical (LZ)
- I²C compatible interface
  – Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  – Minimizes total write time per byte
- Self timed write cycle
  Typical write cycle time of 6ms
- Hardware write protect for upper block (NM24C17 only)
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, and 8-pin TSSOP
- Available in three temperature ranges
  - Commercial: 0° to +70°C
  - Extended (E): -40° to +85C
  - Automotive (V): -40° to +125°C

Block Diagram



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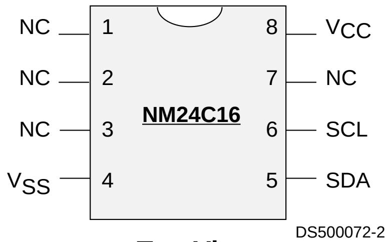
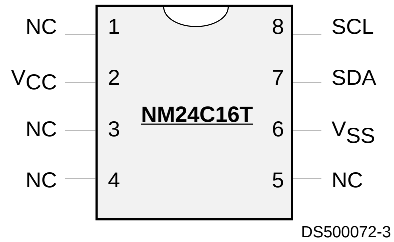
Connection Diagrams

Dual-In-Line Package (N) and SO Package (M8)



Top View
See Package Number N08E (N) and M08A (M8)

TSSOP Package (MT8)

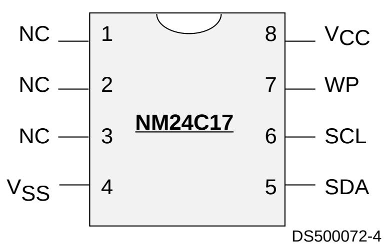


Top View - Rotated Die
See Package Number MTC08 (MT8)

Pin Names

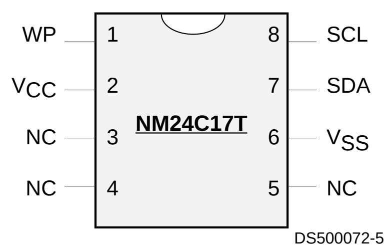
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Internal Connection
V_{CC}	Power Supply

Dual-In-Line Package (N) and SO Package (M8)



Top View
See Package Number N08E (N) and M08A (M8)

TSSOP Package (MT8)



Top View - Rotated Die
See Package Number MTC08 (MT8)

Pin Names

V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V_{CC}	Power Supply
NC	No Internal Connection

Ordering Information

NM 24 C XX F T LZ E XX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1μA Standby Current
	Blank	Normal Pin Out
	T	Rotated Die Pin Out
SCL Clock Frequency	Blank	100KHz
	F	400KHz
Density	16	16K
	17	16K with write protect
	C	CMOS Technology
	W	Total Array write protect
Interface	24	IIC - 2 Wire
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C16/17	0°C to +70°C
NM24C16E/17E	-40°C to +85°C
NM24C16V/17V	-40°C to +125°C
Positive Power Supply	
NM24C16/17	4.5V to 5.5V
NM24C16L/17L	2.7V to 5.5V
NM24C16LZ/17LZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.5	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.5	1.0	mA
I_{SB}	Standby Current for L Standby Current for LZ	V_{IN} = GND or V_{CC} V_{IN} = GND or V_{CC}		1 0.1	10 1	µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 1)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are T_A = 25°C and nominal supply voltage (5V).

AC Conditions of Test

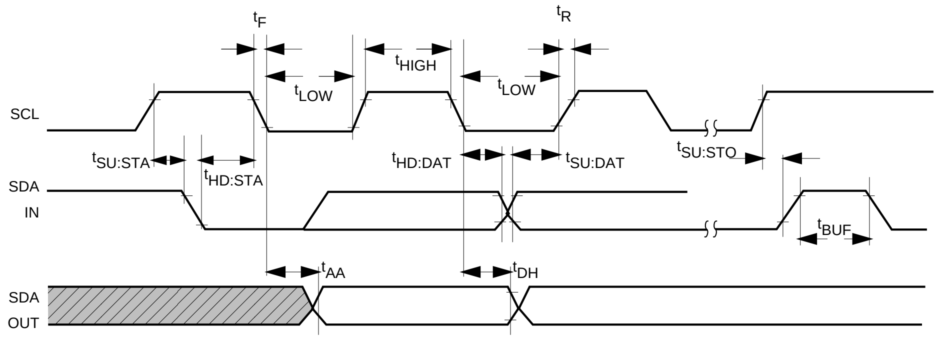
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 5.5V)

Symbol	Parameter	100 kHz		400 kHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 2)	Write Cycle Time - NM24C16/17 - NM24C16/17L, NM24C16/17LZ		10 15		10 15	ms

Note 2: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C16/17 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



Note 3: SCL = Serial Clock Data
SDA = Serial Data I/O

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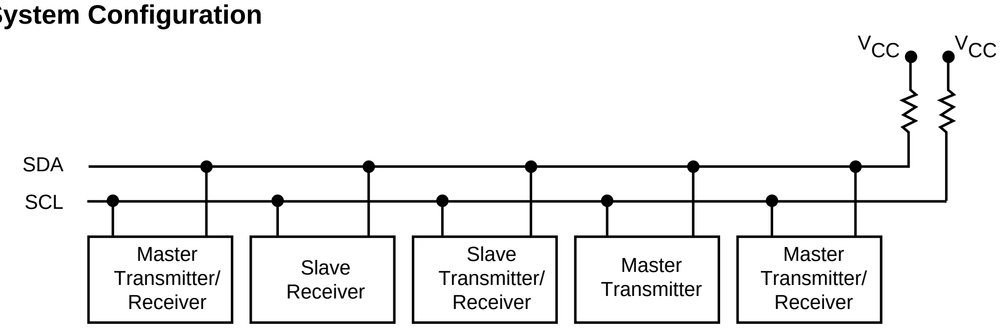
System Layout

Typical System Configuration



Note 4: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

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Example of 16K (Maximum size) of Memory on 2-Wire Bus

Device	Address Pins			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C16/17	No Connect	No Connect	No Connect	16,384 Bits	8

Device Operation

Background Information (I^2C Bus)

As mentioned, the I^2C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

As shown below, the EEPROMs on the I^2C bus may be configured in any manner required, the total memory addressed can not exceed 16k (16,384 bits). EEPROM memory address programming is controlled by 2 methods:

- **All unused pins must be grounded** (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

For devices with densities greater than 16K, a different protocol, extended I^2C protocol, is used. Refer to NM24C32 datasheet (for example) for additional details.

Addressing an EEPROM memory location involves sending a command string with the following information: [DEVICE TYPE]–[DEVICE ADDRESS]–[PAGE BLOCK ADDRESS]–[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data
PAGE	16 sequential addresses (one byte each) that may be programmed during a 'Page Write' programming cycle
PAGE BLOCK	2048 (2K) bits organized into **16 pages of addressable memory. (8 bits) x (16 pages) = 2048 bits**
MASTER	Any I^2C device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

WP Write Protection (NM24C17 Only)

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C16/17 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C16/17 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 2* and *Figure 3* on next page.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C16/17 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C16/17 to place the device in the standby power mode.

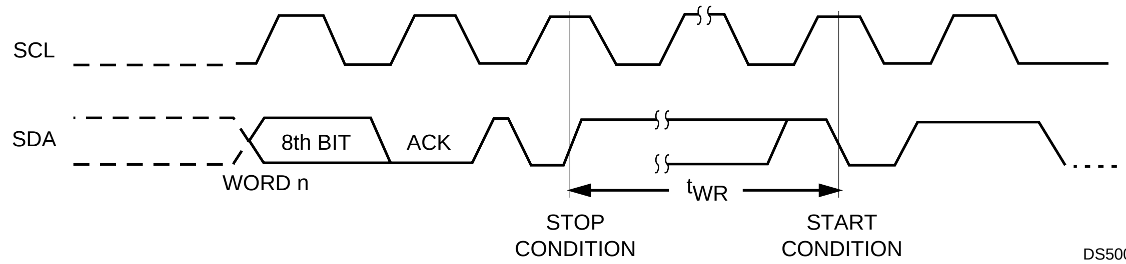
Write Cycle Timing

Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits.

During the ninth clock cycle the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4.*

Write Cycle Timing (Figure 1)



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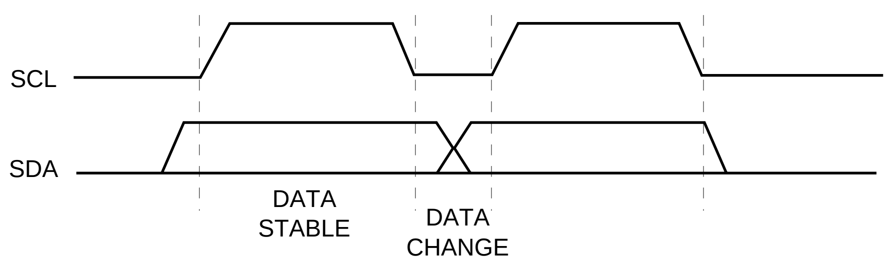
Note 6: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

Data Validity (Figure 2)



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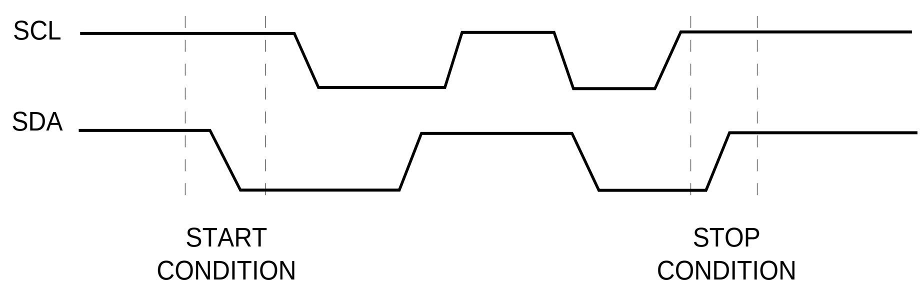
Start and Stop Definition (Figure 3)



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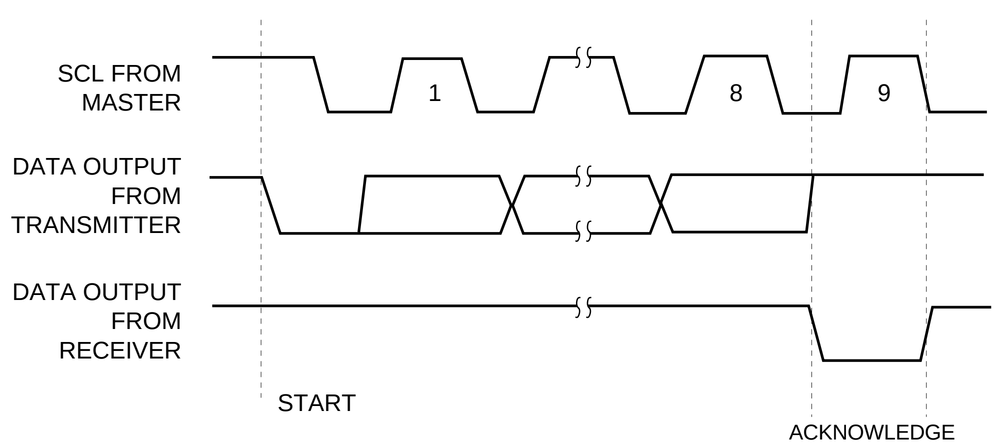
Acknowledge Response from Receiver (Figure 4)



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Write Cycle Timing (Continued)

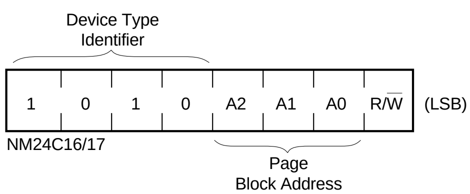
The NM24C16/17 device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C16/17 will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C16/17 slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (*see Figure 5)*. This is fixed as 1010 for all devices.

Slave Addresses (Figure 5)



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Refer to the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blcks	Page Block Addresses
NM24C16/17	P	P	P	8	000 001 010 011 ... 111

P: Refers to an internal PAGE BLOCK memory segment.

All I^{2}C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addressess 0000 through 1111). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C16/17 recognizes the start condition, the devices interfaced to the I^{2}C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page of memory. Upon receipt of the byte address the NM24C16/17 responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C16/17 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C16/17 inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24C16/17 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to fifteen more bytes. After the receipt of each byte, the NM24C16/17 will respond with an acknowledge.

After the receipt of each byte, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen bytes prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 9* for the address, acknowledge, and data transfer sequence.

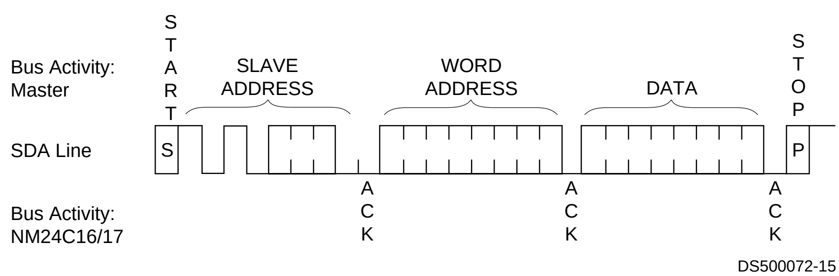
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24C16/17 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C16/17 is still busy with the write operation no ACK will be returned. If the NM24C16/17 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

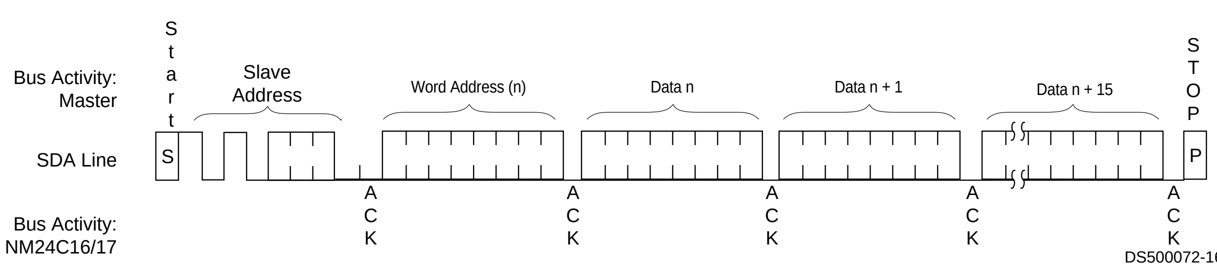
Write Protection (NM24C17 Only)

Programming of the upper half of the memory will not take place if the WP pin of the NM24C17 is connected to V_{CC}. The NM24C17 will accept slave and byte addresses; but if the memory accessed is write protected by the WP pin, the NM24C17 will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.FIGURE 6. Byte Write

Byte Write (Figure 6)



Page Write (Figure 7)



Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the $R/\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C16/17 contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with $R/\overline{W}$ set to one, the NM24C16/17 issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C16/17 discontinues transmission. Refer to *Figure* 8 for the sequence of address, acknowledge and data transfer.

Random Read

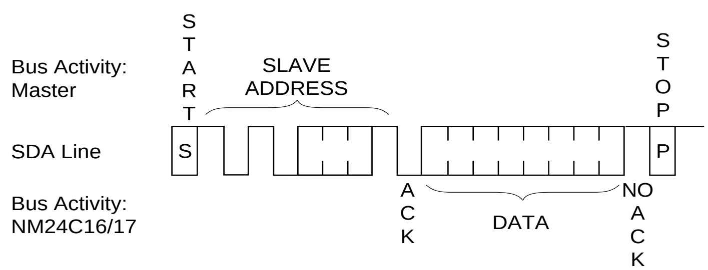
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the $R/\overline{W}$ bit set to one, the master must first perform a “dummy” write operation. The master issues the start condition, slave address and then the byte address it is to read. After the byte address acknowledge, the master immediately reissues the start condition and the slave address with the $R/\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C16/17 and then by the eight bit byte. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C16/17 discontinues transmission. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C16/17 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C16/17 continues to output data for each acknowledge received. Refer to *Figure 10* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 8)



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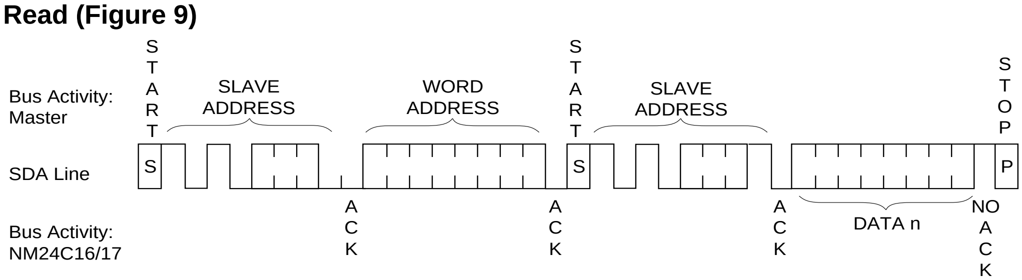
Random Read (Figure 9)



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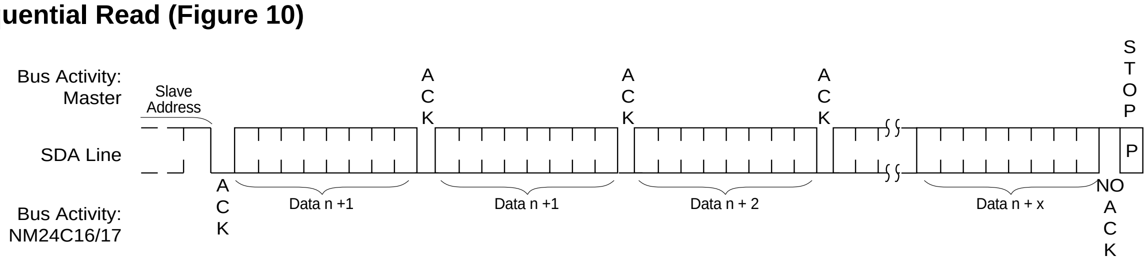
Sequential Read (Figure 10)



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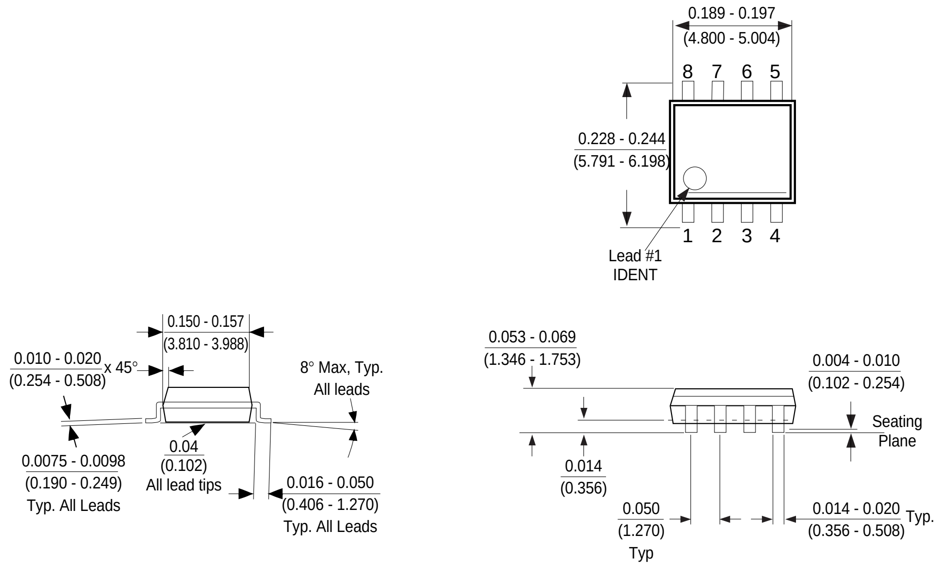
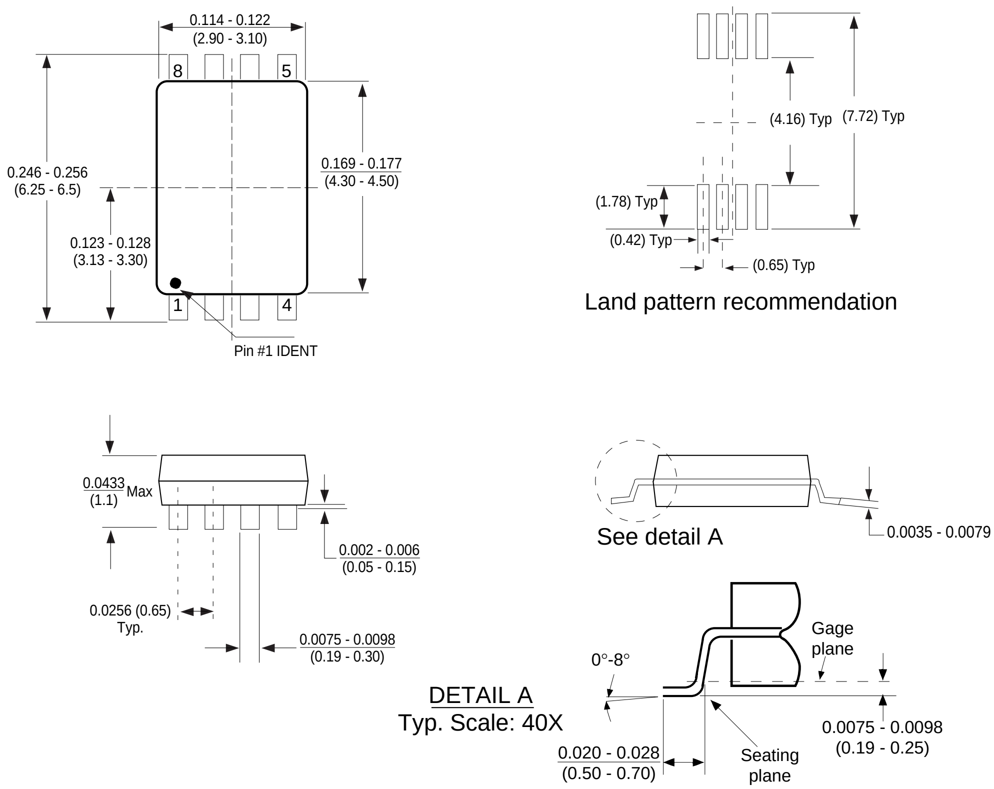
Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Molded Small Outline Package (M8)
Package Number M08A

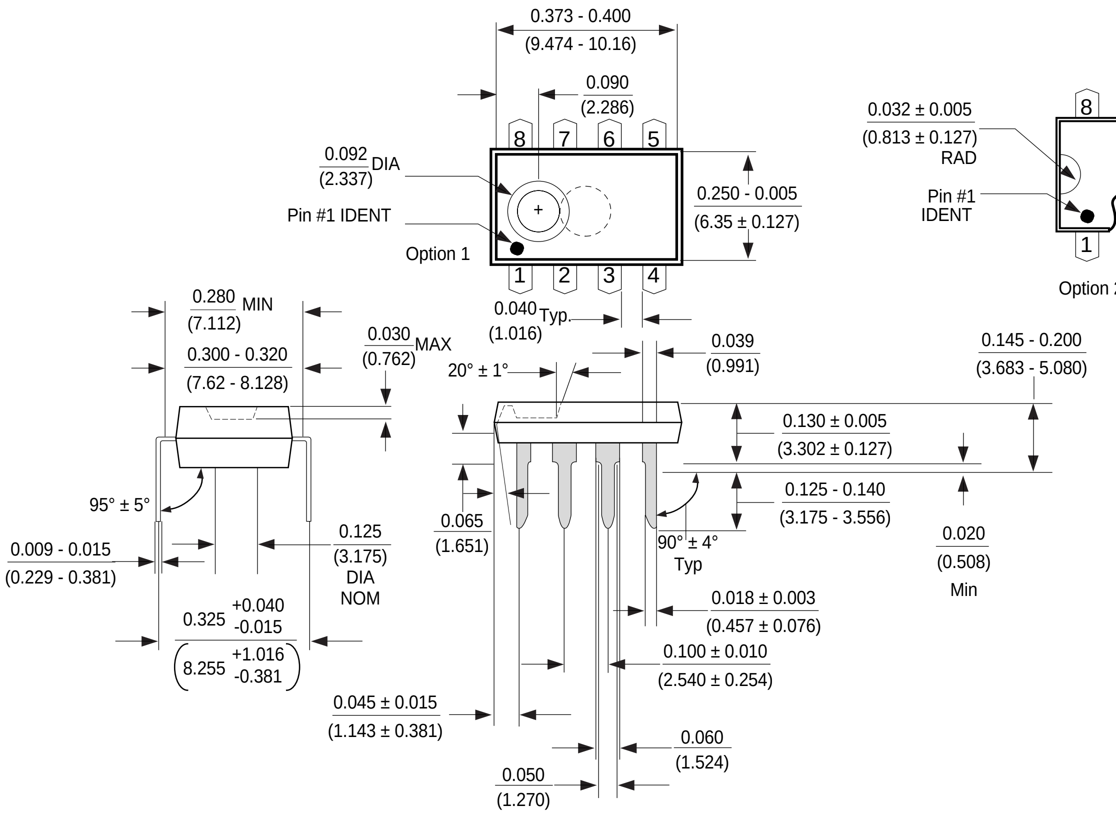


Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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