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NET2868 USB Hub Controller
Preliminary Specification

Document: TBD
Revision: 0.4
Date: 10/29/96

Revision History

Revision	Issue Date	Comments
0.1	July 8, 1996	Draft
0.2	August 8, 1996	Added more sections
0.3	October 8, 1996	Revised table headings
0.4	October 29, 1996	Updated Electrical Specifications

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NET2868 USB Hub Controller

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1. Highlights

1.1 Features

- Self-Powered or Bus-Powered USB Hub With Bus Powered Controller Supports both Full-Speed and Low-Speed Devices.
- One Upstream Port plus 4 Downstream Ports.
- Integrated Hub Protocol Controller for Power Control, Port Connect / Disconnect, Suspend, Fault Recovery.
- Ganged or Individual Port Power Control Support.
- Global or Individual Current Protection Support.
- Enable and Activity Status for each Port.
- Serial Bus Interface Engine (SIE) for Packet decoding/generation, CRC generation and checking, NRZI encoding/decoding and bit-stuffing.
- Complete Universal Serial Bus 1.0 Specification compatibility.
- 48-pin PQFP.

1.2 Overview

The NET2868 Four-Port USB Hub Chip allows up to four USB devices or hubs to connect to an upstream USB Hub or Host port. The two main components of the hub are the Repeater and the Controller.

The Repeater is responsible for the following functions:

- Connectivity Setup and Tear-Down
- Device Connect/Disconnect Detection
- Reset Support
- Suspend/Resume Support
- Frame Synchronization
- Full/Low Speed Device Support
- Bus Fault Detection and Recovery
- Power Management

The Controller is responsible for the following functions:

- Host to Hub Communication
- Control Registers
- Status Ports
- Standard and Class Specific Control Endpoint
- Enumeration Support

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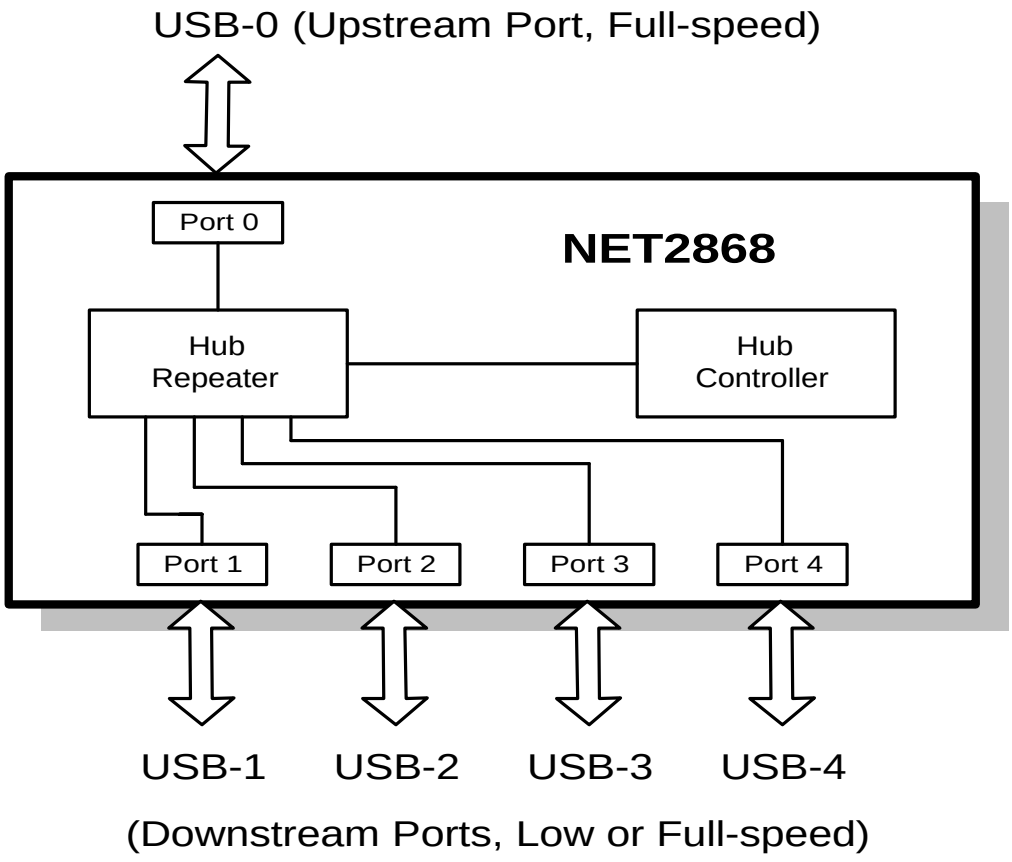
1.3 NET2868 Block Diagram



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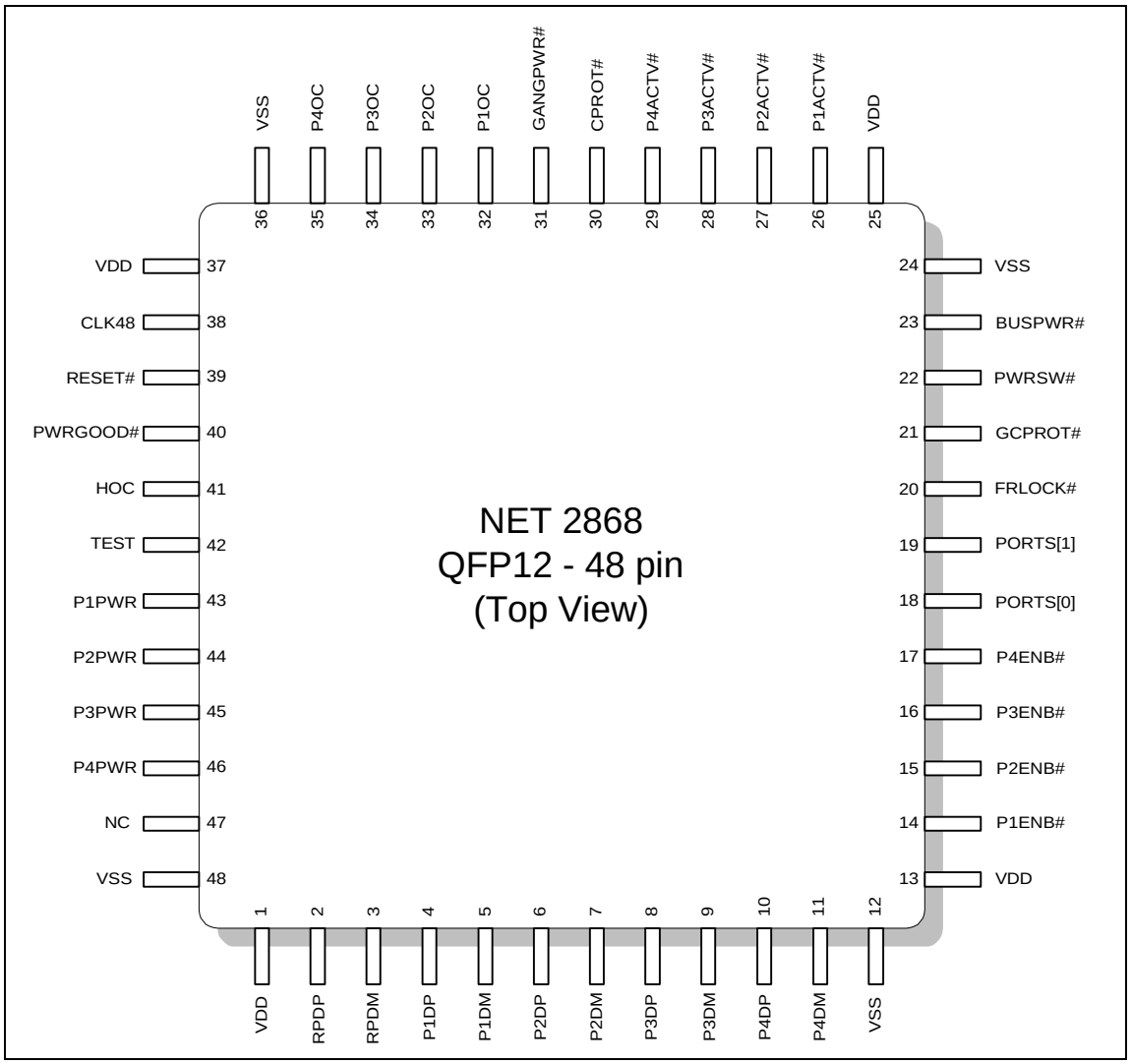
2. Pin Connection Diagram



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3. Pin Description

Pin Type	Description
I	Input
I, ST	Input, Schmitt Trigger
O	Output
I/O	Bi-Directional
TS	Tri-State
TP	Totem-Pole
#	Active low

Signal Name	Pin	Type	Description
CLK48	38	I	**Clock.** 48 MHz clock input.
RESET#	39	I, ST	**Reset.** External reset to the hub. Connect to system or power-on reset.
PORTS[1:0]	19, 18	I	**Number of Downstream Ports**. Number of downstream ports implemented. PORTS[1:0] Ports Implemented 0 0 1 0 1 2 1 0 3 1 1 4
CPROT#	30	I	**Current Protection** 0 = Hub implements current protection. 1 = Hub does not implement current protection (only allowed with bus powered hubs).
GCPROT#	21	I	**Global Current Protection** 0 = Hub reports over-current as a summation of all ports' current draw. 1 = Hub reports over-current on a per-port basis.
PWRSW#	22	I	**Power Switching** 0 = Hub implements power switching on downstream ports. 1 = Downstream ports are always powered up when hub is on.
GANGPWR#	31	I	**Ganged Power Switching** 0 = All ports power up at once. 1 = Ports can be powered up individually.
BUSPWR#	23	I	**Bus Powered** 0 = Hub is powered from the root port (bus-powered). 1 = Hub is powered from its own power supply (self-powered).

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RPDP,RPDM	2, 3	I/O	**Root Port** RPDP and RPDM are the differential data signals of the Root Port. NOTE: An external 1.5 KΩ resistor must be connected from RPDP to 3.3V. This pullup resistor indicates to the host that a full-speed device (the hub) is connected to the host port.
P1DP,P1DM	4, 5	I/O	**Downstream Port 1** P1DP and P1DM are the differential data signals of Downstream Port 1. NOTE: External 15 KΩ resistors must be connected from P1DP and P1DM to ground. These resistors signal a single ended zero, allowing the hub to recognize when no device is attached.
P2DP,P2DM	6, 7	I/O	**Downstream Port 2** P2DP and P2DM are the differential data signals of Downstream Port 2. NOTE: External 15 KΩ resistors must be connected from P2DP and P2DM to ground.
P3DP,P3DM	8, 9	I/O	**Downstream Port 3** P3DP and P3DM are the differential data signals of Downstream Port 3. NOTE: External 15 KΩ resistors must be connected from P3DP and P3DM to ground.
P4DP,P4DM	10, 11	I/O	**Downstream Port 4** P4DP and P4DM are the differential data signals of Downstream Port 4. NOTE: External 15 KΩ resistors must be connected from P4DP and P4DM to ground.
PWRGOOD#	40	I, ST	**Local Power Good** 0 = Local power supply is good. 1 = Local power supply lost.
HOC	41	I, ST	**Hub Over-Current.** 1 = The total of all of the downstream ports' current has exceeded the specified.
P1OC	32	I, ST	**Port 1 Over-Current.** 1 = Port 1 over-current detected.
P2OC	33	I, ST	**Port 2 Over-Current.** 1 = Port 2 over-current detected.
P3OC	34	I, ST	**Port 3 Over-Current.** 1 = Port 3 over-current detected.
P4OC	35	I, ST	**Port 4 Over-Current.** 1 = Port 4 over-current detected.
P1PWR	43	O	**Port 1 Power Enable.** 1 = Enable power to Port 1.
P2PWR	44	O	**Port 2 Power Enable.** 1 = Enable power to Port 2
P3PWR	45	O	**Port 3 Power Enable.** 1 = Enable power to Port 3
P4PWR	46	O	**Port 4 Power Enable.** 1 = Enable power to Port 4
P1ENB#	14	O	**Port 1 Enabled.** 0 = Port 1 is in the enabled state.
P2ENB#	15	O	**Port 2 Enabled.** 0 = Port 2 is in the enabled state.
P3ENB#	16	O	**Port 3 Enabled.** 0 = Port 3 is in the enabled state.
P4ENB#	17	O	**Port 4 Enabled.** 0 = Port 4 is in the enabled state.
P1ACTV#	26	O	**Port 1 Activity.** 0 = Data activity detected on port 1.

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P2ACTV#	27	O	**Port 2 Activity.** 0 = Data activity detected on port 2.
P3ACTV#	28	O	**Port 3 Activity.** 0 = Data activity detected on port 3.
P4ACTV#	29	O	**Port 4 Activity.** 0 = Data activity detected on port 4.
FRLOCK#	20	O	**Frame Timer Locked.** 0 = Hub frame timer is locked to host.
TEST	42	I	**Test.** For normal operation, connect this pin to ground.
NC	47	--	**No connect.**
VDD	1, 13, 25, 37	PWR	**Supply Voltage.** Connect these pins to the +3.3V supply voltage.
VSS	12, 24, 36, 48	GND	**Circuit Ground.** Connect these pins to ground.

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4. Electrical Specifications

4.1 Absolute Maximum Ratings

Conditions that exceed the Absolute Maximum limits may destroy the device.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply Voltage	With Respect to Ground	-2.0	7.0	V
V_I	DC input voltage	With Respect to Ground	-2.0	7.0	V
I_{OUT}	DC Output Current, per pin		-25	25	mA
T_{STG}	Storage Temperature	No bias	-65	150	° C
T_{AMB}	Ambient temperature	Under bias			° C
T_J	Junction temperature	Under bias			° C
P_D	Power Dissipation				mW
V_{ESD}	ESD Rating	R = 1.5K, C = 100pF		2	KV

4.2 Recommended Operating Conditions

Conditions that exceed the Operating limits may cause the device to function incorrectly.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply Voltage		3.0	3.6	V
V_I	Input Voltage		0	V_{DD}	V
V_O	Output Voltage		0	V_{DD}	V
T_A	Operating temperature		0	70	° C
t_R	Input rise time				ns/V
t_F	Input fall time				ns/V

4.3 DC Specifications

Operating Conditions: VDD: 3.3V ± 5%, TA = 0°C to 70°C
All typical values are at VDD = 3.3V and TA = 25°C
Notes 1,2;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DI}	Differential Input Sensitivity	| (D+) - (D-) |	0.2			V
V_{CM}	Differential Common Mode Range	Includes VDI range	0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8		2.0	V
V_{OH}	Static Output High	RL of 15 KΩ to GND	2.8		3.6	V
V_{OL}	Static Output Low	RL of 1.5 KΩ to 3.6V			0.3	V
I_{LO}	Hi-Z State Data Line Leakage	$0V < V_{IN} < 3.3V$	-10		+10	µA
I_{CC}	VDD Supply Current	VDD = 3.3V		60	100	mA
I_{CCS}	VDD Supply Current (Suspend)	Hub suspended			500	µA
C_{IO}	I/O Capacitance	Pin to GND			20	pF

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4.4 AC Specifications

Operating Conditions: VDD: 3.3V ± 5%, TA = 0°C to 70°C
All typical values are at VDD = 3.3V and TA = 25°C

4.4.1 Full Speed Port AC Specifications

Operating Conditions: Notes 1,2,3.

Symbol	Parameter	Conditions	Waveform	Min	Typ	Max	Unit
T_R	Rise & Fall Times	C_L = 50 pF		4		20	nS
T_F		Notes 5,6		4		20	
T_{RFM}	Rise/Fall time matching	(T_R/ T_F)		90		110	%
V_{CRS}	Output Signal Crossover Voltage			1.3		2.0	V
Z_{DRV}	Driver Output Resistance	Steady State Drive		28		43	Ω
T_{DRATE}	Data Rate			11.97	12	12.03	Mbs
T_{DDJ1}	Source Differential Driver Jitter to Next Transition	Notes 7,8.		-3.5	0	3.5	ns
T_{DDJ2}	Source Differential Driver Jitter for Paired Transitions	Notes 7,8		-4.0	0	4.0	ns
T_{DEOP}	Differential to EOP Transition Skew	Note 8		-2	0	5	ns
T_{EOPT}	Source EOP Width	Note 8		160	167	175	ns
T_{JR1}	Receiver Data Jitter Tolerance to Next Transition	Note 8		-18.5	0	18.5	ns
T_{JR2}	Receiver Data Jitter Tolerance for Paired Transitions	Note 8		-9	0	9	ns
T_{EOPR1}	EOP Width at Receiver; Must reject as EOP	Note 8		40			ns
T_{EOPR2}	EOP Width at Receiver; Must accept as EOP	Note 8		80			ns

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4.4.2 Low Speed Port AC Specifications

Operating Conditions: Notes 1,2,4.

Symbol	Parameter	Conditions	Waveform	Min	Typ	Max	Unit
T_R	Rise Times	C_L = 50 pF C_L = 350 pF, Notes 5,6	 Figure 4-1	75		 300	ns ns
T_F	Fall Times	C_L = 50 pF C_L = 350 pF Notes 5,6	 Figure 4-1	75		 300	ns ns
T_{RFM}	Rise/Fall time matching	($T_{R/}$ T_F)		80		120	%
V_{CRS}	Output Signal Crossover Voltage			1.3		2.0	V
T_{DRATE}	Data Rate			1.4775	1.5	1.5255	Mbs
T_{DDJ1}	Source Differential Driver Jitter to Next Transition	Notes 7,8	Figure 4-2	-75	0	75	ns
T_{DDJ2}	Source Differential Driver Jitter for Paired Transitions	Notes 7,8	Figure 4-2	-45	0	45	ns
T_{DEOP}	Differential to EOP Transition Skew	Note 8	Figure 4-3	-40	0	100	ns
T_{EOPT}	Source EOP Width	Note 8	Figure 4-3	1.25	1.33	1.5	µs
T_{UJR1}	Receiver Data Jitter Tolerance to Next Transition	Note 8	Figure 4-4	-152	0	152	ns
T_{UJR2}	Receiver Data Jitter Tolerance for Paired Transitions	Note 8	Figure 4-4	-200	0	200	ns
T_{EOPR1}	EOP Width at Receiver; Must reject as EOP	Note 8	Figure 4-3	330			ns
T_{EOPR2}	EOP Width at Receiver; Must accept as EOP	Note 8	Figure 4-3	675			ns

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4.4.3 Hub/Repeater Full Speed AC Specifications

Conditions: Root Port and Downstream Ports configured as Full Speed.
Note 2.

Symbol	Parameter	Conditions	Waveform	Min	Typ	Max	Unit
T_{HDD1}	Hub Differential Delay with Cable	Note 3,7,8	Figure 4-5			70	ns
T_{HDD2}	Hub Differential Delay without Cable	Note 3,7,8	Figure 4-5			40	ns
T_{HDJ1}	Hub Differential Driver Jitter to Next Transition	Note 3,7,8	Figure 4-5	-3	0	3	ns
T_{HDJ2}	Hub Differential Driver Jitter for Paired Transitions	Note 3,7,8	Figure 4-5	1	0	1	ns
T_{sop}	Data bit width distortion after SOP	Note 3,8	Figure 4-5	-5	0	3	ns
T_{EOPD}	Hub EOP Delay Relative to t_{HDD}	Note 3,8	Figure 4-6	0		15	ns
T_{HESK}	Hub EOP Output Width Skew	Note 3,8	Figure 4-6	-15		15	ns

4.4.4 Hub/Repeater Low Speed AC Specifications

Conditions: Downstream Ports configured as Low Speed.
Note 2.

Symbol	Parameter	Conditions	Waveform	Min	Typ	Max	Unit
T_{LHDD}	Hub Differential Delay	Note 4,7,8	Figure 4-5			300	ns
T_{LDHJ1}	Hub Differential Driver Jitter to Next Transition (Downstream)	Note 4,7,8	Figure 4-5	-45	0	45	ns
T_{LDHJ2}	Hub Differential Driver Jitter for Paired Transitions (Downstream)	Note 4,7,8	Figure 4-5	-15	0	15	ns
T_{LUHJ1}	Hub Differential Driver Jitter to Next Transition (Upstream)	Note 4,7,8	Figure 4-5	-45	0	45	ns
T_{LUHJ2}	Hub Differential Driver Jitter for Paired Transitions (Upstream)	Note 4,7,8	Figure 4-5	-45	0	45	ns
T_{sop}	Data bit width distortion after SOP	Note 4,8	Figure 4-5	-60	0	45	ns
T_{LEOPD}	Hub EOP Delay Relative to t_{HDD}	Note 4,8	Figure 4-6	0		200	ns
T_{LHESK}	Hub EOP Output Width Skew	Note 4,8	Figure 4-6	-300		300	ns

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4.4.5 AC/DC Specification Notes

1. All voltages measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50 pF, unless otherwise specified.
3. Full Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D+ data line.
4. Low Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D- data line.
5. Measured from 10% to 90% of the data signal.
6. The rising and falling edges should be smoothly transitioning (monotonic).
7. Timing difference between the differential data signals.
8. Measured at crossover point of differential data signals.
9. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub V_{BUS} droop of 330 mV.

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4.5 AC Waveforms

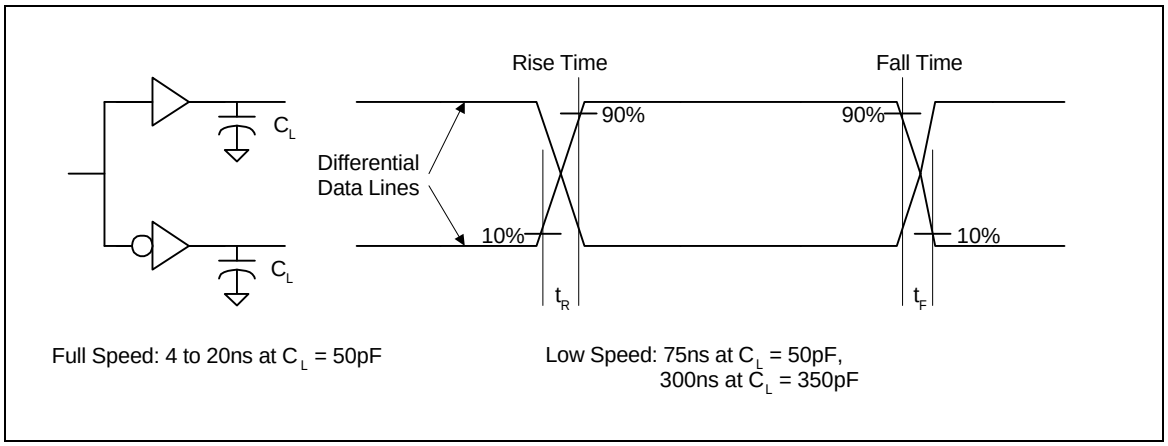

Figure 4-1. Data Signal Rise and Fall Time

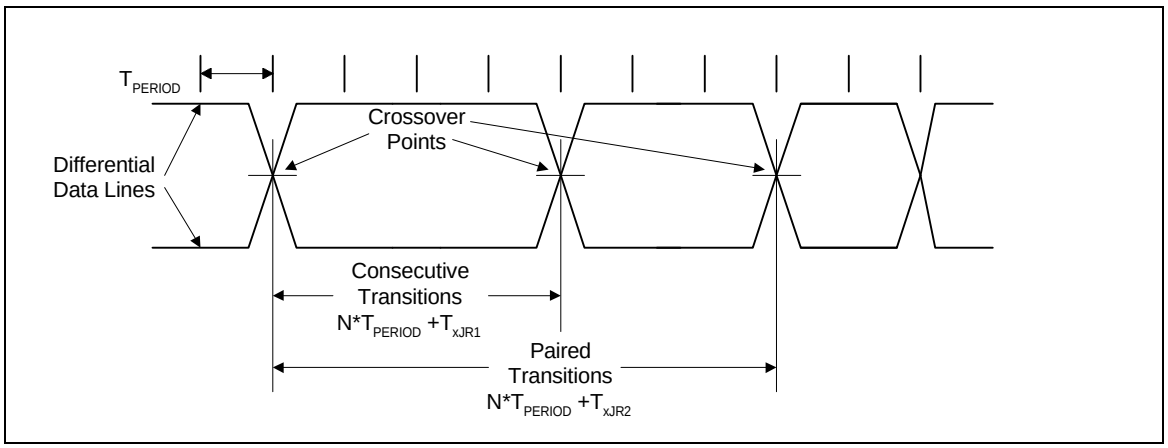

Figure 4-2. Differential Data Jitter

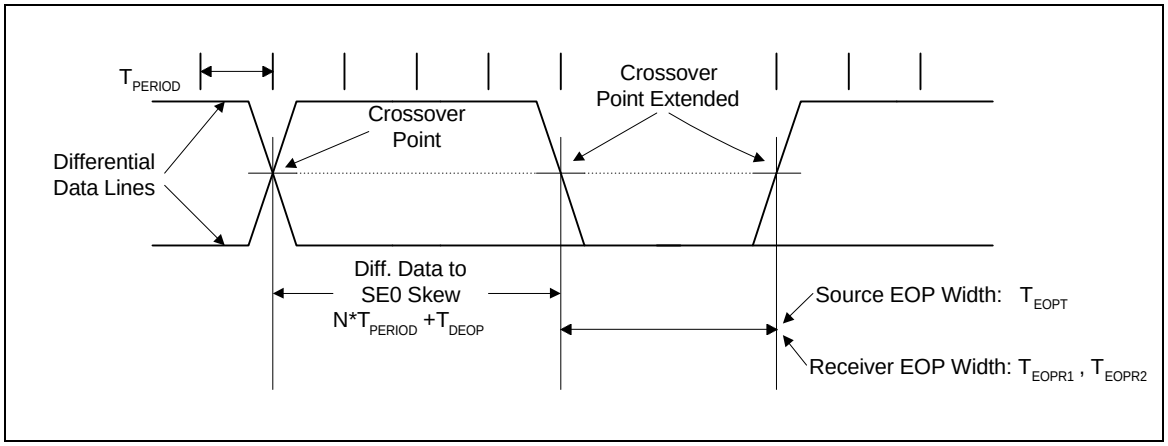

Figure 4-3. Differential to EOP Transition Skew and EOP Width

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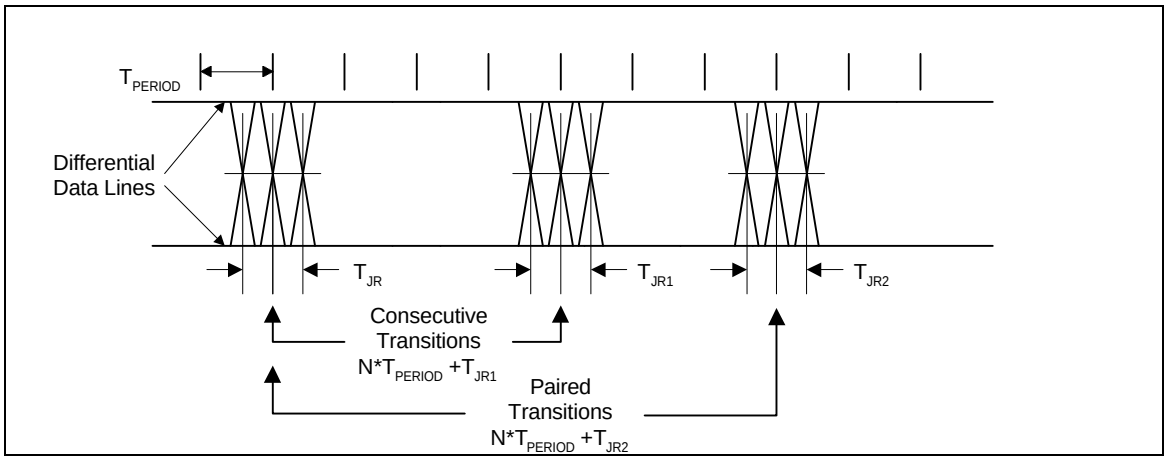
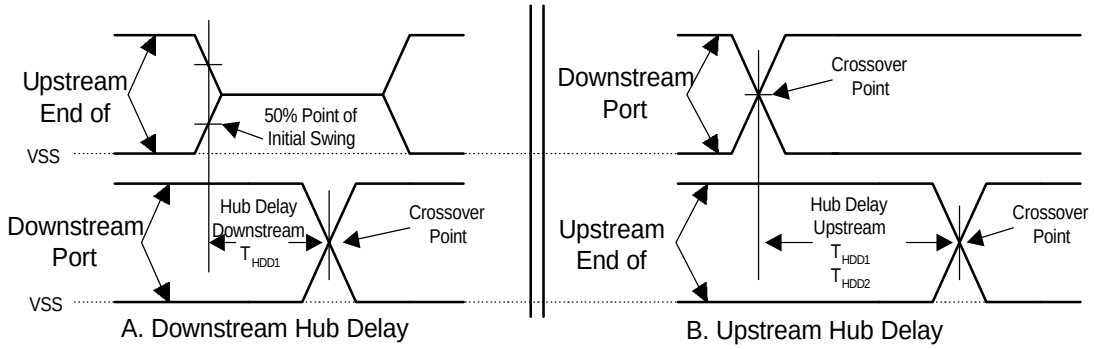


Figure 4-4. Receiver Jitter Tolerance



Hub Differential Jitter

$T_{HDJ1} = T_{HDDx}(J) - T_{HDDx}(K)$ or $T_{HDDx}(K) - T_{HDDx}(J)$ Consecutive Transitions

$T_{HDJ2} = T_{HDDx}(J) - T_{HDDx}(J)$ or $T_{HDDx}(K) - T_{HDDx}(K)$ Paired Transistors

Bit after SOP Width Distortion: (Same as data jitter for SOP and next J transition.)

$T_{HDJ1} = T_{HDDx}(SOP) - T_{HDDx}(next\ J)$

Low Speed timings are determine in the same way for:

T_{LHDD}, T_{LDHJ1}, T_{LDHJ2}, T_{LUHJ1}, T_{LUJH2}, and T_{LSOP}

Figure 4-5. Hub Differential Delay, Differential Jitter, and SOP Distortion

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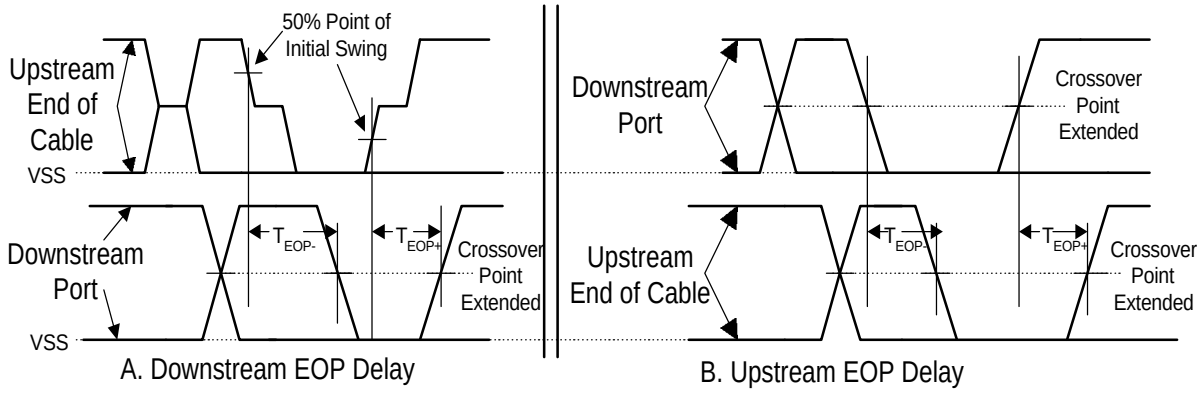

EOP Delay
$T_{EOPD} = T_{EOP-}$

EOP Skew
$T_{HESK} = T_{EOP+} - T_{EOP-}$

Low Speed timings are determined in the same way for:
T_{LEOPD} and T_{LHESK}

Figure 4-6. Hub EOP Delay and EOP Skew

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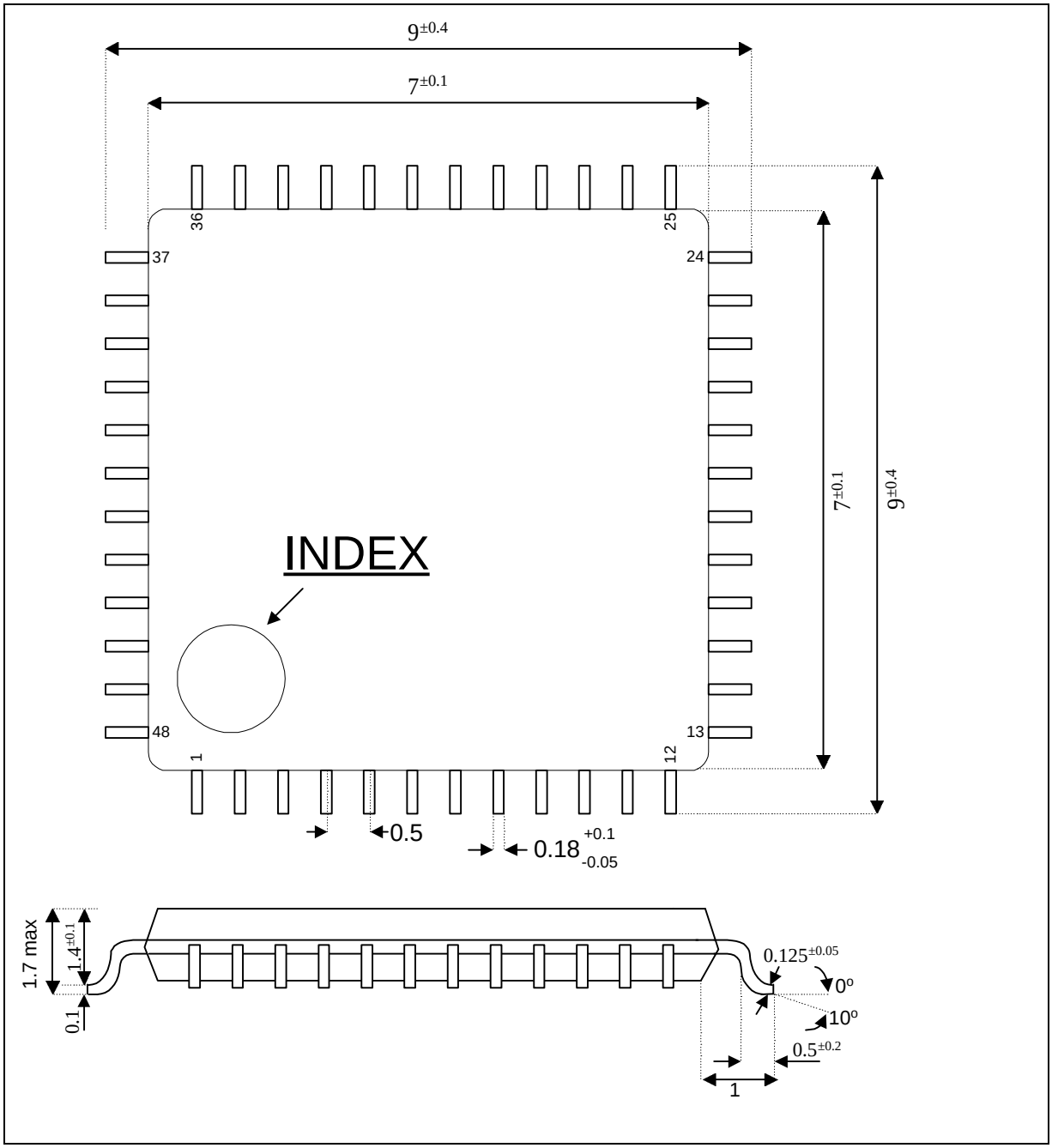
5. Mechanical Drawing



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