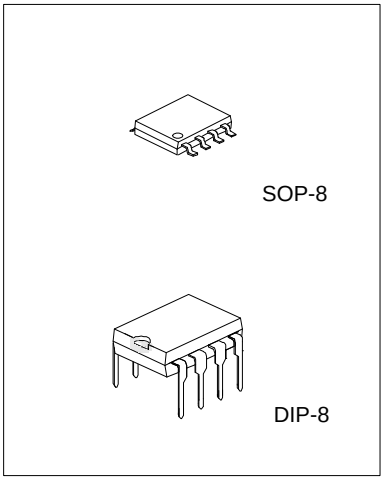
SINGLE TIMER



DESCRIPTION

The UTC NE555 is a highly stable timer integrated circuit. It can be operated in Astable mode and Monostable mode. With monostable operation, the time delay is controlled by one external and one capacitor. With a stable operation, the frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

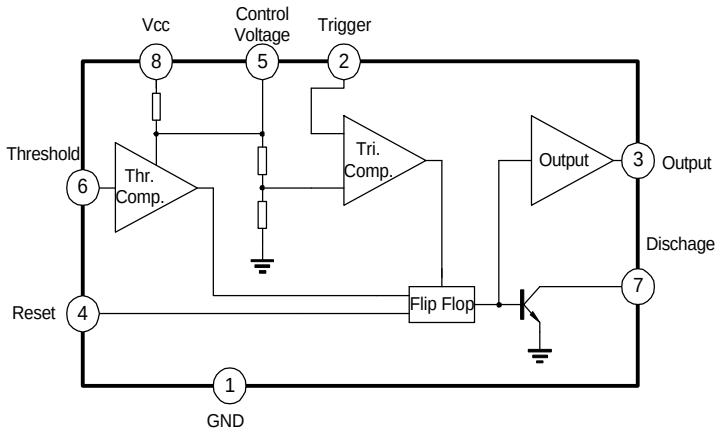
FEATURES

*High current driver capability(=200mA)
*Adjustable duty cycle
*Timing from μSec to Hours
*Turn off time less than 2μSec.

APPLICATIONS

*Precision timing
*Pulse generation
*Time delay generation

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

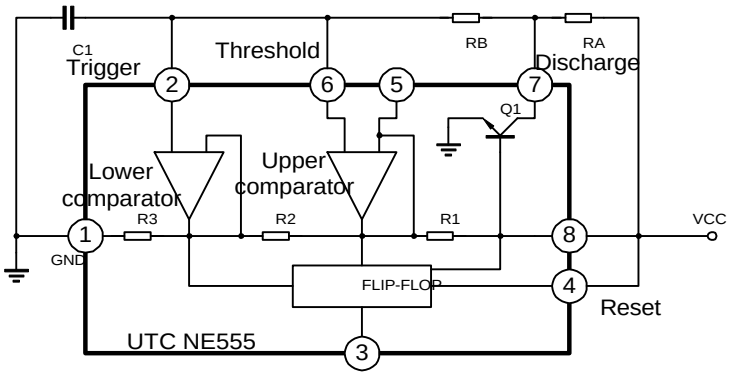
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	Vcc	16	V
Power Dissipation	Pd	600	mW
Lead Temperature	Tlead	300	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	-65 to 150	°C

ELECTRICAL CHARACTERISTICS(Ta=25°C ,Vcc=5 ~ 15V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	Vcc		4.5		16	V
Supply Current	Icc	Vcc=5V,RL=∝		3	6	mA
(Note 1)		Vcc=15V,RL=∝		7.5	15	mA
Timing Error(monostable)						
Initial Accurary(Note 2)	ACCUR	RA=1k to 100kΩ		1.0	3.0	%
Drift with Temperature	Δt/ΔT	C=0.1μF		50		ppm/°C
Drift with Supply Voltage	Δt/ΔVcc			0.1	0.5	%/V
Timing Error(astable)						
Initial Accurary(Note 2)	ACCUR	RA=1k to 100kΩ		2.25		%
Drift with Temperature	Δt/ΔT	C=0.1μF		150		ppm/°C
Drift with Supply Voltage	Δt/ΔVcc			0.3		%/V
Control Voltage	Vc	Vcc=15V	9.0	10.0	11.0	V
		Vcc=5V	2.6	3.33	4.0	V
Threshold Voltage	VTH	Vcc=15V		10.0		V
		Vcc=5V		3.33		V
Threshold Current(Note 3)	ITH			0.1	0.25	μA
Trigger Voltage	Vtr	Vcc=5V	1.1	1.67	2.2	V
		Vcc=15V	4.5	5	5.6	V
Trigger Current	Itr	Vtr=0		0.01	2.0	μA
Reset Voltage	Vrst		0.4	0.7	1.0	V
Reset Current	Irst			0.1	0.4	mA
Low Output Voltage	VOL	Vcc=15V				
		Isink=10mA		0.06	0.25	V
		Isink=50mA		0.3	0.75	V
		Vcc=5V				
		Isink=5mA		0.05	0.35	V
High Output Voltage	VOH	Vcc=15V				
		Isource=200mA		12.5		V
		Isource=100mA	12.75	13.3		V
		Vcc=5V, Isource=100mA	2.75	3.3		V
Rise Time of Output	tR			100		nSec
Fall Time of Output	tF			100		nSec
Dischage Leakage Current	ILKG			20	100	nA

Note 1:Supply current when output is high is typically 1mA less at Vcc=5V.
Note 2:Tested at Vcc=5.0V and Vcc=15V.
Note 3:this will determine the maximum value of RA+RB for 15V operation, The maximum total is R=20MΩ, and for 5V operation the maximum total is R=6.7MΩ.

APPLICATION CIRCUIT



APPLICATION NOTES

The application circuit shows astable mode configuration.
Pin 6 (Threshold) is tied to Pin 2 (Trigger) and Pin 4 (reset) is tied to Vcc (Pin 8). The external capacitor C1 of Pin 6 and Pin 2 charges through RA,RB and dischages through RB only. In the internal circuit of UTC NE555 , one input of the upper comparator is at voltage of 2/3Vcc(R1=R2=R3),another input is connected to Pin 6.As soon as C1 is charging to higher than 2/3Vcc, transistor Q1 is turned ON and discharge C1 to collector voltage of transistor Q1. Therefore, the flip-flop circuit is reset and output is low. One input of lower comparator is at voltage of 1/3Vcc, discharge transistor Q1 turn off and C1 charges through RA and RB. Therefore, the flip-flop circuit is set output high. That is, when C1 charges through RA and RB , output is high and when C1 discharge through RB ,output is low. The charge time(output is high) t1 is 0.6 9 3(RA+RB) C1 and the discharge time (output is low) T2 is 0.6 9 3 RB*C1.

$$\ln\left(\frac{Vcc-\frac{1}{3}Vcc}{Vcc-\frac{2}{3}Vcc}\right)=0.693$$

Thus the total period time T is given by

T1=0.693*(RA+RB)*C1
T2=0.693*RB*C1

T=T1+T2=0.693(RA+2RB)*C1.

Then the frequency of astable mode is given by

$$f=\frac{1}{T}=\frac{1.44}{(RA+2RB)*C1}$$

The duty cycle is given by

$$D.C.=\frac{T2}{T}=\frac{RB}{RA+2RB}.$$