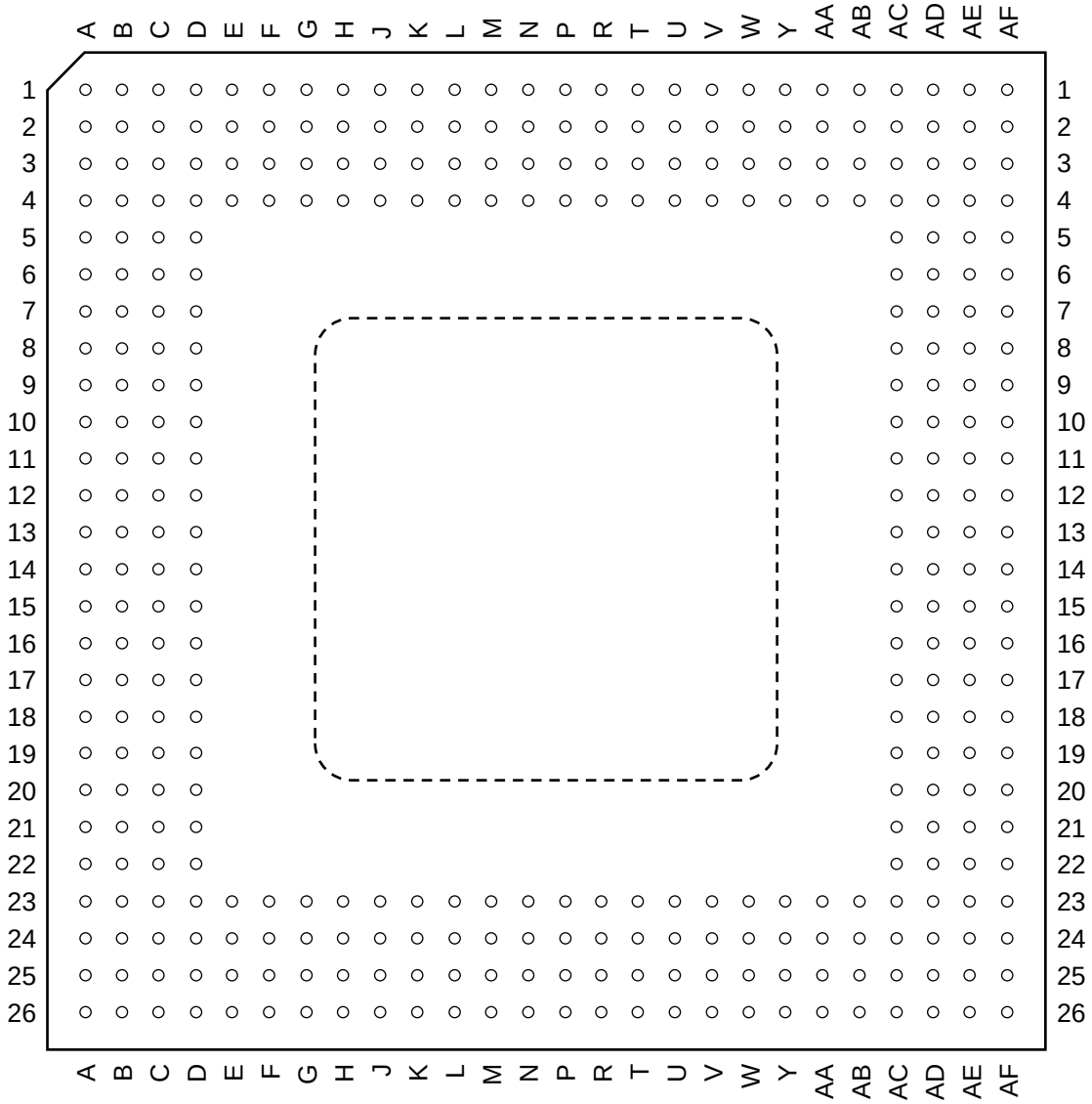
SYSTEM CONTROLLER WITH PCI BUS

—BOTTOM VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
D4	–	GND	B13	I/O	PERR	D23	–	GND	N25	I/O	SYSAD52	AC23	–	GND	AE14	O	MA11	AC4	–	GND	P2	I/O	DEVAD21
C3	–	SVcc	A13	I	LOCK	C24	–	SVcc	N26	I/O	SYSAD21	AD24	–	SVcc	AF14	O	CAS0	AD3	–	SVcc	P1	I	PLL EN
B2	I	PCICLK	D14	I/O	AD14	B25	I/O	SYSAD14	P23	I/O	SYSAD53	AE25	I/O	MD40	AC13	O	CAS1	AE2	I/O	DEVAD2	N4	O	ALE
A1	O	PRST	C14	I/O	AD15	A26	I/O	SYSAD47	P24	I/O	SYSAD22	AF26	I/O	MD36	AD13	O	CAS2	AF1	I/O	DEVAD3	N3	O	DACK0
C4	O	GNT2	B14	I/O	SERR	D24	I/O	SYSAD7	P25	I/O	SYSAD54	AD23	I/O	MD1	AE13	O	CAS3	AC3	I/O	DEVAD4	N2	I/O	DEVAD22
D5	O	GNT4	A14	I/O	C BE1	E23	I/O	SYSCMD4	P26	O	READY	AC22	I/O	MD2	AF13	O	CAS4	AB4	I/O	DEVAD5	N1	O	DACK1
B3	I	REQ1	D15	I/O	AD10	C25	I/O	SYSAD39	R23	I/O	SYSAD23	AE24	I/O	MD44	AC12	O	CAS5	AD2	I/O	DEVAD6	M4	O	DACK2
A2	I	REQ0	C15	I/O	AD11	B26	I/O	SYSAD46	R24	I/O	SYSAD55	AF25	I/O	MD41	AD12	O	CAS6	AE1	I/O	MD31	M3	I/O	DEVAD23
A3	O	GNT0	B15	I/O	AD12	C26	I/O	SYSAD38	R25	I/O	SYSAD24	AF24	I/O	MD45	AE12	O	CAS7	AD1	I/O	DEVAD7	M2	I/O	DEVAD24
C5	I	REQ4	A15	I/O	AD13	E24	I/O	SYSCMD3	R26	O	NMI	AD22	I/O	MD3	AF12	O	RAS0	AB3	I/O	DEVAD8	M1	O	DACK3
D6	I/O	AD28	D16	I/O	AD7	F23	I/O	SYSCMD2	T23	I/O	SYSAD56	AC21	I/O	MD6	AC11	O	RAS1	AA4	I/O	MD61	L4	I	STBY
B4	I	REQ2	C16	I/O	AD8	D25	I/O	SYSAD6	T24	I/O	SYSAD25	AE23	I/O	MD46	AD11	O	RAS2	AC2	I/O	MD28	L3	I/O	DEVAD25
A4	O	GNT1	B16	I/O	AD9	D26	I/O	SYSAD37	T25	I/O	SYSAD57	AF23	I/O	MD47	AE11	O	RAS3	AC1	I/O	DEVAD9	L2	I/O	DEVAD26
C6	I/O	AD29	A16	I/O	C BE0	F24	I/O	SYSCMD1	T26	I/O	SYSAD26	AD21	I/O	MD7	AF11	I/O	MD48	AA3	I/O	DEVAD10	L1	I	RXD0
B5	O	GNT3	D17	–	GND	E25	I/O	SYSAD5	U23	–	GND	AE22	I/O	MD4	AC10	–	GND	AB2	I/O	MD27	K4	–	GND
D7	–	GND	C17	–	Vcc	G23	–	GND	U24	–	Vcc	AC20	–	GND	AD10	–	Vcc	Y4	–	GND	K3	–	Vcc
C7	–	Vcc	B17	I/O	AD5	G24	–	Vcc	U25	I/O	SYSAD58	AD20	–	Vcc	AE10	I/O	MD49	Y3	–	Vcc	K2	O	TXD0
A5	I	REQ3	A17	I/O	AD6	E26	I/O	SYSAD36	U26	I/O	SYSAD27	AF22	I/O	MD5	AF10	I/O	MD50	AB1	I/O	DEVAD11	K1	O	BROMCS
B6	I/O	AD30	C18	I/O	AD2	F25	I/O	SYSAD4	V24	I	COLDRESET	AE21	I/O	MD8	AD9	I/O	MD52	AA2	I/O	DEVAD12	J3	I/O	DEVAD27
A6	I/O	AD31	D18	I/O	AD1	F26	I/O	SYSAD35	V23	I/O	SYSAD59	AF21	I/O	MD9	AC9	I/O	MD51	AA1	I/O	MD30	J4	I/O	DEVAD28
D8	I/O	AD24	B18	I/O	AD3	H23	I/O	SYSAD34	V25	I/O	SYSAD28	AC19	I/O	MD12	AE9	–	GND	W4	I/O	MD60	J2	I/O	DEVAD29
C8	I/O	AD25	A18	I/O	AD4	H24	I/O	SYSAD2	V26	I/O	SYSAD60	AD19	I/O	MD13	AF9	I/O	MD53	W3	I/O	DEVAD13	J1	I/O	DEVAD30
B7	I/O	AD26	B19	I/O	AD0	G25	I/O	SYSCMD0	W25	I	SCMATCH	AE20	I/O	MD10	AE8	I/O	MD16	Y2	I/O	DEVAD14	H2	I/O	DEVAD31
A7	I/O	AD27	C19	I/O	SYSAD9	G26	I/O	SYSAD3	W24	I/O	SYSAD61	AF20	I/O	MD11	AD8	I/O	MD55	Y1	I/O	MD29	H3	O	DEVWR0
B8	I/O	PAR	D19	I/O	SYSAD40	H25	I/O	SYSAD33	W23	I/O	SYSAD29	AE19	I/O	MD14	AC8	I/O	MD54	W2	I/O	MD26	H4	O	DEVWR1
D9	I/O	AD20	A19	I/O	SYSAD41	J23	I/O	SYSAD1	W26	O	SCDOE	AC18	O	WE	AF8	I/O	MD17	V4	I/O	DEVAD15	H1	O	DEVWR2
C9	I/O	AD21	A20	–	GND	J24	I/O	SYSAD32	Y26	I/O	SYSAD62	AD18	O	SDCAS	AF7	I/O	MD19	V3	I/O	DEVAD16	G1	O	DEVWR3
A8	I/O	C BE3	B20	I/O	SYSAD10	H26	O	INT	Y25	I/O	SYSAD31	AF19	I/O	MD15	AE7	I/O	MD18	W1	O	DEVCS0	G2	I	IOCLK
B9	I/O	AD22	C20	–	Vcc	J25	I/O	SYSAD0	Y24	–	Vcc	AE18	O	EDO OE	AD7	–	Vcc	V2	O	DEVCS1	G3	–	Vcc
A9	I/O	AD23	D20	–	GND	J26	I/O	SYSAD16	Y23	–	GND	AF18	O	MA0	AC7	–	GND	V1	I/O	DEVAD17	G4	–	GND
D10	–	GND	A21	I/O	SYSAD42	K23	–	GND	AA26	I/O	SYSAD63	AC17	–	GND	AF6	I/O	MD23	U4	–	PGND	F1	I	JTRST
C10	–	Vcc	B21	I	Vcc OK	K24	–	Vcc	AA25	I/O	SYSAD30	AD17	–	Vcc	AE6	I/O	MD22	U3	–	PVcc	F2	I	JTCLK
B10	I/O	AD18	A22	I/O	SYSAD43	K25	I/O	SYSAD48	AB26	I/O	MD32	AE17	O	MA1	AF5	I/O	MD59	U2	O	DEVCS2	E1	I	JTDI
A10	I/O	AD19	C21	I/O	SYSCMD8	K26	I/O	SYSAD17	AA24	O	TC	AF17	O	MA2	AD6	I/O	MD21	U1	I/O	DEVAD18	F3	I	JTMS
D11	I/O	AD16	D21	I/O	SYSCMD7	L23	I/O	SYSAD49	AA23	–	GND	AC16	O	MA3	AC6	I/O	MD20	T4	O	DEVCS3	F4	O	TXD1
C11	I/O	AD17	B22	I/O	SYSAD11	L24	I/O	SYSAD18	AB25	I/O	MD37	AD16	O	MA5	AE5	I/O	MD58	T3	O	DEVRD	E2	O	JTDO
B11	I/O	FRAME	C22	I/O	SYSCMD6	L25	I/O	SYSAD50	AB24	I/O	MD42	AE16	O	MA7	AD5	I/O	MD57	T2	I/O	DEVAD19	E3	I	TMODE
A11	I/O	C BE2	A23	I/O	SYSAD44	L26	O	VALIDIN	AC26	I/O	MD33	AF16	O	MA9	AF4	I/O	MD24	T1	I/O	DEVAD20	D1	I	RXD1
D12	I/O	STOP	B23	I/O	SYSAD12	M23	I/O	SYSAD19	AC25	I/O	MD38	AC15	O	MA4	AE4	I/O	MD63	R4	I	MCLK	D2	I	WAIT
C12	I/O	DEVSEL	D22	I/O	SYSCMD5	M24	I/O	SYSAD51	AB23	I/O	MD0	AD15	O	MA6	AC5	I/O	MD56	R3	O	CLKFB	E4	I	DREQ0
B12	I/O	TRDY	C23	I/O	SYSAD8	M25	I/O	SYSAD20	AC24	I/O	MD43	AE15	O	MA8	AD4	I/O	MD62	R2	–	Vcc	D3	I	DREQ1
A12	I/O	IRDY	A24	I/O	SYSAD45	M26	I	VALIDOUT	AD26	I/O	MD34	AF15	O	MA10	AF3	I/O	MD25	R1	–	GND	C1	I	SMODE
D13	–	GND	B24	I/O	SYSAD13	N23	–	GND	AD25	I/O	MD39	AC14	–	GND	AE3	I/O	DEVAD0	P4	–	GND	C2	I	DREQ2
C13	–	SVcc	A25	I/O	SYSAD15	N24	–	SVcc	AE26	I/O	MD35	AD14	–	Vcc	AF2	I/O	DEVAD1	P3	–	SVcc	B1	I	DREQ3

INPUTS

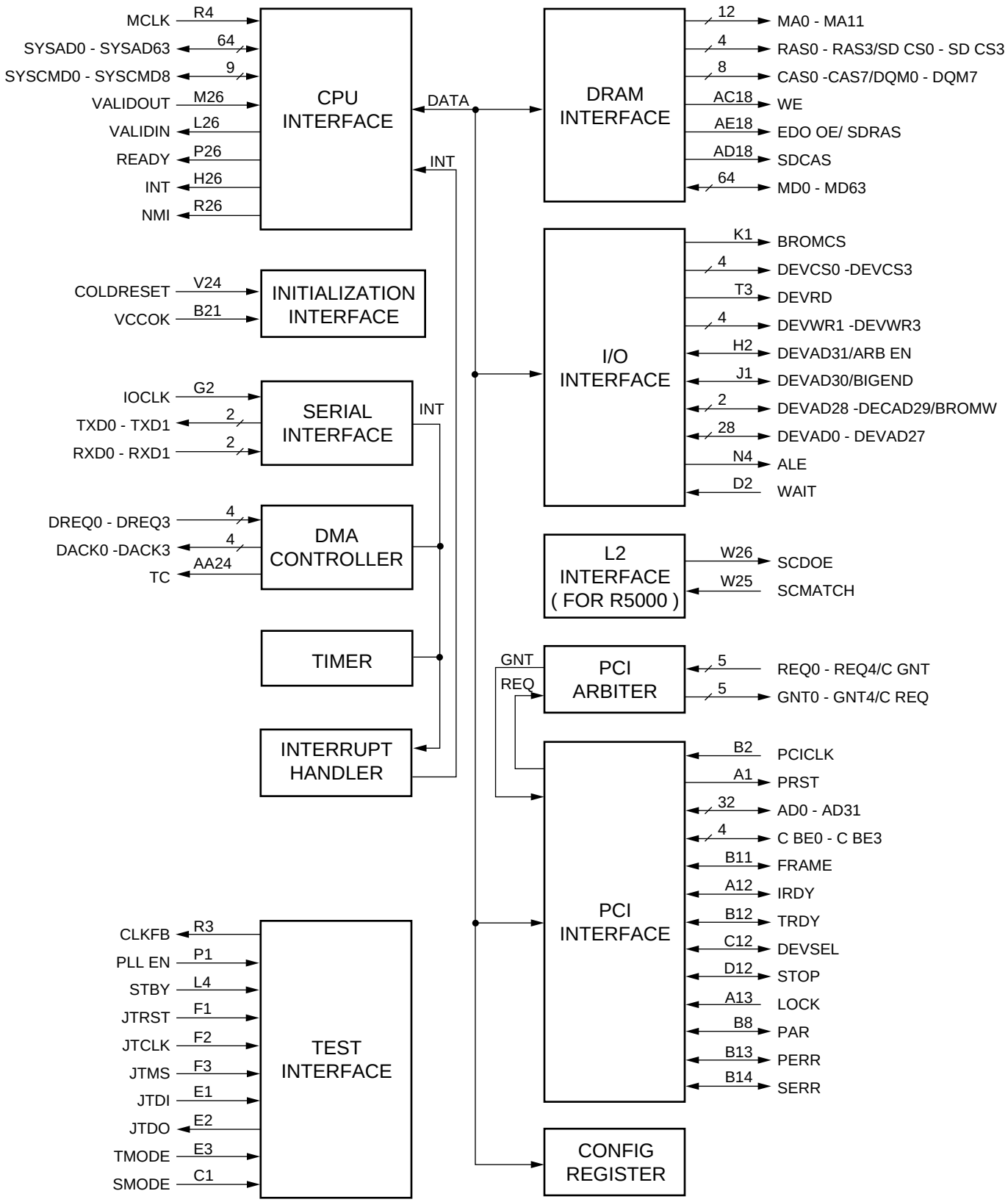
C GNT	:	ND5000LBG GRANT
COLDRESET	:	ND5000LBG RESET
DREQ0 - DREQ3	:	DMA REQUEST
IOCLK	:	I/O CLOCK
JTCLK	:	JTAG CLOCK
JTDI	:	JTAG DATA IN
JTMS	:	JTAG MODE SELECT
JTRST	:	JTAG RESET
LOCK	:	EXCLUSIVE ACCESS
MCLK	:	MASTER CLOCK
PCICLK	:	PCI CLOCK
PLL EN	:	PLL ENABLE
REQ0 - REQ4	:	PCI REQUEST
RXD0, RXD1	:	SERIAL RECEIVE DATA STREAM
SCMATCH	:	SECONDARY CACHE TAG MATCH
SMODE	:	SCAN MODE
STBY	:	5 V INPUT TOLERANT STAND BY
TMODE	:	TEST MODE
VALIDOUT	:	VALID OUTPUT
VccOK	:	VCCOK
WAIT	:	EXTERNAL WAIT

OUTPUTS

ALE	:	ADDRESS LATCH ENABLE
BROMCS	:	BOOT ROM CHIP SELECT
C REQ	:	ND5000LBG REQUEST
CAS0 - CAS7	:	COLUMN ADDRESS STROBE
CLKFB	:	FEEDBACK CLOCK MONITOR
DACK0 - DACK3	:	DMA ACKNOWLEDGE
DEVCS0 - DEVCS3	:	DEVICE CHIP SELECT
DEVRD	:	DEVICE READ
DEVWR0 - DEVWR3	:	DEVICE WRITE ENABLE
DQM0 -DQM7	:	DATA MASK FOR WRITES AND THE OUTPUT DISABLE FOR READS
EDO OE	:	DATA OUTPUT ENABLE FOR EDO
GNT0 - GNT4	:	PCI GRANT
INT	:	INTERRUPT
JTDO	:	JTAG DATA
MA0 - MA11	:	MEMORY ADDRESS
NMI	:	NON MASKABLE INTERRUPT
PRST	:	PCI RESET
RAS0 - RAS3	:	ROW ADDRESS STROBE FOR STANDARD DRAM
READY	:	READ/WRITE READY
SCDOE	:	SECONDARY CACHE DATA RAM OUTPUT ENABLE
SDCAS	:	COLUMN ADDRESS STROBE FOR SDRAM
SDCS0 -SDCS3	:	CHIP SELECT FOR SDRAM
SDRAS	:	ROW ADDRESS STROBE FOR SDRAM
TC	:	DMA TERMINAL COUNT
TXD0, TXD1	:	SERIAL TRANSMIT DATA STREAM
VALIDIN	:	VALID INPUT
WE	:	DRAM WRITE ENABLE

INPUTS/OUTPUTS

AD0 - AD31	:	PCI ADDRESS/DATA BUS
ARB EN	:	ARBITER ENABLE
BIGEND	:	BIG ENDIAN
BROMW	:	BOOT ROM WIDTH CONFIGURATION
C BE0 - C BE3	:	BUS COMMAND/BYTE ENABLE
DEVAD0 - DEVAD31	:	DEVICE ADDRESS/DATA BUS
DEVSEL	:	DEVICE SELECT
FRAME	:	CYCLE FRAME
IRDY	:	INITIATOR READY
MD0 - MD63	:	MEMORY DATA
PAR	:	PARITY
PERR	:	PARITY ERROR
SERR	:	SYSTEM ERROR
STOP	:	STOP ACCESS
SYSAD0 - SYSAD63	:	SYSTEM ADDRESS/DATA BUS
SYSCMD0 - SYSCMD8	:	SYSTEM COMMAND BUS
TRDY	:	TARGET READY


MCLK
R4
SYSAD0 - SYSAD63
64
SYSCMD0 - SYSCMD8
9
VALIDOUT
M26
VALIDIN
L26
READY
P26
INT
H26
NMI
R26
CPU INTERFACE
DATA
INT
COLDRESET
V24
VCCOK
B21
INITIALIZATION INTERFACE
IOCLK
G2
TXD0 - TXD1
2
RXD0 - RXD1
2
SERIAL INTERFACE
INT
DREQ0 - DREQ3
4
DACK0 -DACK3
4
TC
AA24
DMA CONTROLLER
TIMER
INTERRUPT HANDLER
CLKFB
R3
PLL EN
P1
STBY
L4
JTRST
F1
JTCLK
F2
JTMS
F3
JTDI
E1
JTDO
E2
TMODE
E3
SMODE
C1
TEST INTERFACE
DRAM INTERFACE
12
MA0 - MA11
4
RAS0 - RAS3/SD CS0 - SD CS3
8
CAS0 -CAS7/DQM0 - DQM7
AC18
WE
AE18
EDO OE/ SDRAS
AD18
SDCAS
64
MD0 - MD63
I/O INTERFACE
K1
BROMCS
4
DEVCS0 -DEVCS3
T3
DEVRD
4
DEVWR1 -DEVWR3
H2
DEVAD31/ARB EN
J1
DEVAD30/BIGEND
2
DEVAD28 -DECAD29/BROMW
28
DEVAD0 - DEVAD27
N4
ALE
D2
WAIT
L2 INTERFACE (FOR R5000)
W26
SCDOE
W25
SCMATCH
GNT
REQ
PCI ARBITER
5
REQ0 - REQ4/C GNT
5
GNT0 - GNT4/C REQ
PCI INTERFACE
B2
PCICLK
A1
PRST
32
AD0 - AD31
4
C BE0 - C BE3
B11
FRAME
A12
IRDY
B12
TRDY
C12
DEVSEL
D12
STOP
A13
LOCK
B8
PAR
B13
PERR
B14
SERR
CONFIG REGISTER