

October 1996 Revised November 1999

NC7SZ00

TinyLogic™ UHS 2-Input NAND Gate

General Description

The NC7SZ00 is a single 2-Input NAND Gate from Fairchild's Ultra High Speed Series of TinyLogicTM. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.8V to 5.5V V_{CC} operating range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 6V independent of V_{CC} operating voltage.

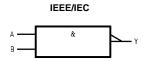
Features

- Space saving SOT23 or SC70 5-lead package
- Ultra High Speed; t_{PD} 2.4 ns typ into 50 pF at 5V V_{CC}
- High Output Drive; ±24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.8V–5.5V
- \blacksquare Matches the performance of LCX when operated at 3.3V $\rm V_{CC}$
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

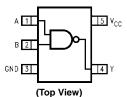
Ordering Code:

Order Number	Package Number	Package Top Mark	Package Description	Supplied As		
NC7SZ00M5	MA05B	7Z00	5-Lead SOT23, JEDEC MO-178, 1.6mm	250 Units on Tape and Reel		
NC7SZ00M5X	MA05B	7Z00	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel		
NC7SZ00P5	MAA05A	Z00	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	250 Units on Tape and Reel		
NC7SZ00P5X	MAA05A	Z00	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel		

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A, B	Inputs
Υ	Output

Function Table

In	puts	Output
Α	В	Y
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

H = HIGH Logic Level L = LOW Logic Level

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Absolute Maximum Ratings(Note 1)

-0.5V to +6V Supply Voltage (V_{CC}) -0.5V to +6V DC Input Voltage (V_{IN}) DC Output Voltage (VOUT) -0.5V to +6V

DC Input Diode Current (I_{IK}) $@V_{IN} < -0.5V$

DC Output Diode Current (I_{OK})

@ V_{IN} > 6V

 $@V_{OUT} < -0.5V$ -50 mA $@V_{OUT} > 6V, V_{CC} = GND$ +20 mA DC Output Current (I_{OUT}) \pm 50 mA DC V_{CC} /GND Current (I_{CC} / I_{GND}) \pm 50 mA -65°C to +150°C Storage Temperature (T_{STG}) Junction Temperature under Bias (T_J) 150°C

Junction Lead Temperature (T_L);

(Soldering, 10 seconds) 260°C

Power Dissipation (PD) @ +85°C

SOT23-5 200 mW SC70-5 150 mW

Recommended Operating Conditions (Note 2)

Supply Voltage Operating (V_{CC}) 1.8V to 5.5V Supply Voltage Data Retention (V_{CC}) 1.5V to 5.5V Input Voltage (V_{IN}) 0V to 5.5V Output Voltage (V_{OUT}) 0V to V_{CC} -40°C to +85°C Operating Temperature (T_A)

Input Rise and Fall Time (t_r, t_f)

-50 mA

+20 mA

 V_{CC} @ 1.8V, 2.5V $\pm 0.2V$ 0 ns/V to 20 ns/V V_{CC} @ 3.3V \pm 0.3V 0 ns/V to 10 ns/V V_{CC} @ $5.0V \pm 0.5V$ 0 ns/V to 5 ns/V $\,$

Thermal Resistance (θ_{JA})

SOT23-5 300°C/W SC70-5 425°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifi-

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} T _A = +25°C			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions		
Syllibol	i didilictor		Min	Тур	Max	Min	Max	Onics	00	ilaitions
V_{IH}	HIGH Level Input Voltage	1.8	0.75 V _{CC}			0.75 V _{CC}		V		
		2.3-5.5	0.70 V _{CC}			0.70 V _{CC}		V		
V _{IL}	LOW Level Input Voltage	1.8			0.25 V _{CC}		0.25 V _{CC}	V		
		2.3-5.5			$0.30~\mathrm{V}_\mathrm{CC}$		$0.30~\mathrm{V}_\mathrm{CC}$, v		
V _{OH}	HIGH Level Output Voltage	1.8	1.7	1.8		1.7				
		2.3	2.2	2.3		2.2		V	V = V	
		3.0	2.9	3.0		2.9		, v	$V_{IN} = V_{IL}$ $I_{OH} = -100 \mu A$	Юн — 100 р. (
		4.5	4.4	4.5		4.4				
		2.3	1.9	2.15		1.9				$I_{OH} = -8 \text{ mA}$
		3.0	2.4	2.80		2.4		V		$I_{OH} = -16 \text{ mA}$
		3.0	2.3	2.68		2.3				$I_{OH} = -24 \text{ mA}$
		4.5	3.8	4.20		3.8				$I_{OH} = -32 \text{ mA}$
V _{OL}	LOW Level Output Voltage	1.8		0.0	0.1		0.1			
		2.3		0.0	0.1		0.1	V	V = V	I _{OL} = 100 μA
		3.0		0.0	0.1		0.1	•	vIN – vIH	10L = 100 μΑ
		4.5		0.0	0.1		0.1			
		2.3		0.10	0.3		0.3			$I_{OL} = 8 \text{ mA}$
		3.0		0.15	0.4		0.4	V		$I_{OL} = 16 \text{ mA}$
		3.0		0.22	0.55		0.55	•		$I_{OL} = 24 \text{ mA}$
		4.5		0.22	0.55		0.55			$I_{OL} = 32 \text{ mA}$
I _{IN}	Input Leakage Current	0-5.5			±1		±10	μΑ	V _{IN} = 5.5\	, GND
I _{OFF}	Power Off Leakage Current	0.0			1		10	μΑ	V_{IN} or V_{OI}	_{JT} = 5.5V
I _{CC}	Quiescent Supply Current	1.8-5.5			2.0		20	μΑ	V _{IN} = 5.5\	, GND

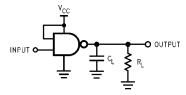
AC Electrical Characteristics

Symbol	Parameter	V_{CC} $T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	Fig. No.		
Cyllibol	rarameter	(V)	Min	Тур	Max	Min Max		Onits	Conditions	rig. No.
t _{PLH} ,	Propagation Delay	1.8	2.0	4.5	9.5	2.0	10.0		$C_L = 15 pF$,	Figure 1
t _{PHL}		2.5 ± 0.2	0.8	3.0	6.5	0.8	7.0	ns	$R_L = 1 M\Omega$	Figure 3
		3.3 ± 0.3	0.5	2.4	4.5	0.5	4.7	115		
		5.0 ± 0.5	0.5	2.0	3.9	0.5	4.1			
t _{PLH,}	Propagation Delay	3.3 ± 0.3	1.5	2.9	5.0	1.5	5.2	ns	$C_L = 50 pF$,	Figure 1
t _{PHL}		5.0 ± 0.5	0.8	2.4	4.3	0.8	4.5	115	$R_L = 500\Omega$	Figure 3
C _{IN}	Input Capacitance			4				pF		
C _{PD}	Power Dissipation Capacitance	3.3		24				pF	(Note 3)	Figure 2
		5.0		30				þΓ	(Note 3)	Figure 2

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:

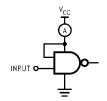
I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) +(I_{CC}static).

AC Loading and Waveforms



 C_L includes load and stray capacitance Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



$$\begin{split} &\text{Input} = \text{AC Waveform; t}_r = t_f = 1.8 \text{ ns;} \\ &\text{PRR} = 10 \text{ MHz; Duty Cycle} = 50\% \\ &\text{FIGURE 2. I}_{CCD} \text{ Test Circuit} \end{split}$$

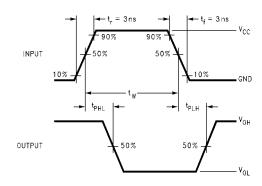
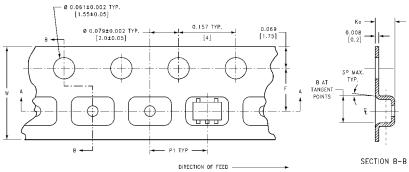
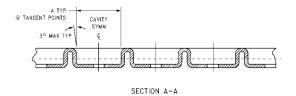


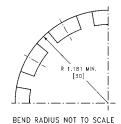
FIGURE 3. AC Waveforms

Tape and Reel Specification Tape Format Package Tape Number Cavity Cover Tape Designator Section Cavities Status Status 125 (typ) Leader (Start End) Empty Sealed M5, P5 Filled Carrier 250 Sealed Trailer (Hub End) 75 (typ) Sealed Empty Leader (Start End) 125 (typ) Empty Sealed M5X, P5X Carrier 3000 Filled Sealed Sealed Trailer (Hub End) 75 (typ) Empty

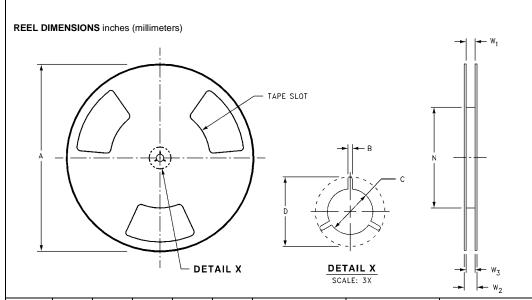
TAPE DIMENSIONS inches (millimeters)



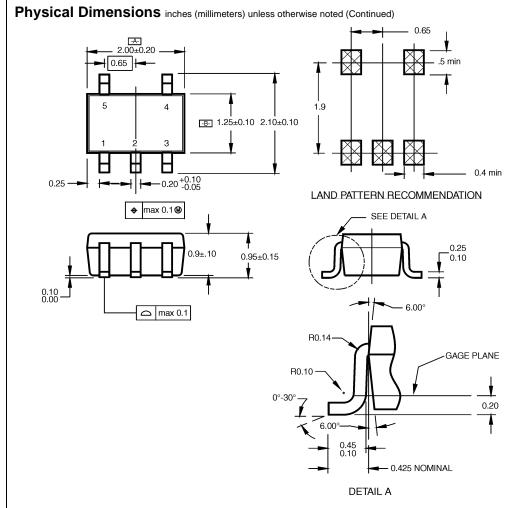




Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W		
SC70-5	8 mm	0.093	0.096	0.138 ± 0.004	0.053 ± 0.004	0.157	0.315 ± 0.004		
		(2.35)	(2.45)	(3.5 ± 0.10)	(1.35 ± 0.10)	(4)	(8 ± 0.1)		
SOT23-5	9 mm	0.130	0.130	0.138 ± 0.002	0.055 ± 0.004	0.157	0.315 ± 0.012		
	8 mm	(3.3)	(3.3)	(3.5 ± 0.05)	(1.4 ± 0.11)	(4)	(8 ± 0.3)		



Tape Size	Α	В	С	D	N	W1	W2	W3
8 mm	7.0	0.059	0.512	0.795	2.165	0.331 + 0.059/-0.000	0.567	W1 + 0.078/-0.039
0 111111	(177.8)	(1.50)	(13.00)	(20.20)	(55.00)	(8.40 + 1.50/-0.00)	(14.40)	(W1 + 2.00/-1.00)



NOTES:

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

MAA05ARevC

C. DIMENSIONS ARE IN MILLIMETERS.

5-Lead SC70, EIAJ SC-88a, 1.25mm Wide Package Number MAA05A

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