

SCOPE: CMOS HIGHSPEED 8-BIT A/D CONVERTER WITH TRACK AND HOLD

<u>Device Type</u>	<u>Generic Number</u>
01	MX7820U(x)/883B
02	MX7820T(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
MAXIM SMD			
Q R	GDIP1-T20 or CDIP2-T20	20 LEAD Cerdip	J20
E 2	CQCCI-N20	20 LEADLESS CHIP CARRIER	L20

Absolute Maximum Ratings

Supply Voltage to GND	0V, +7V
Digital Input Voltage	-0.3V, V_{DD}
Digital Output Voltage	-0.3V, V_{DD}
Positive Reference Voltage	V_{REF-} to V_{DD}
Negative Reference Voltage	0V to V_{REF+}
Input Voltage (V_{IN})	-0.3V to V_{DD}

Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature	-65°C to +150°C
Continuous Power Dissipation	$T_A = +70^\circ\text{C}$
20 pin Cerdip (derate 11.1mW/°C above +70°C)	889mW
20 pin LCC (derate 9.1mW/°C above +70°C)	727mW
Junction Temperature T_J	+150°C
Thermal Resistance, Junction to Case, θ_{JC}	
20 pin Cerdip	40°C/W
20 pin LCC	20°C/W
Thermal Resistance, Junction to Ambient, θ_{JA} :	
20 pin Cerdip	90°C/W
20 pin LCC	110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A)	-55°C to +125°C
Supply Voltage Range (V_{DD})	+4.75V to 5.25V
Positive Reference Voltage (V_{REF+})	+5.0V
Negative Reference Voltage (V_{REF-})	0V
Ground Potential (GND)	0V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤ T _A ≤ +125 °C 1/ 2/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Resolution	RES	This is the minimum resolution for which no missing codes are guaranteed.	1,2,3	All	8		LSB
Total Unadjusted Error	TUE	Includes gain error, offset error and linearity error.	1 2,3,12	01		±1.0 ±0.5	LSB
			1,2,3	02		±1.0	
Analog Input Leakage Current	I _{IN}		1,2,3	All		± 3.0	μA
Analog Input Capacitance	CIA	NOTE 3	4	All		60	pF
Reference Input Resistance	R _{IN}		1,2,3	All	1.0	4.0	kΩ
Digital Input High Level Voltage	V _{IH}	$\overline{\text{CS}}$, $\overline{\text{WR}}$, and $\overline{\text{RD}}$ inputs	1,2,3	All	2.4		V
		Mode Input (Pin 7)			3.5		
Digital Input Low Level Voltage	V _{IL}	$\overline{\text{CS}}$, $\overline{\text{WR}}$, and $\overline{\text{RD}}$ inputs	1,2,3	All		0.8	V
		Mode Input (Pin 7)				1.5	
Digital Input High Level Current	I _{IH}	$\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs	1,2,3	All		±1.0	μA
		$\overline{\text{WR}}$ Inputs				±3.0	
		Mode Input (Pin 7)				±200	
Digital Input Low Current	I _{IL}	$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$ and mode inputs	1,2,3	All		-1.0	μA
Digital Input Capacitance	C _{ID}	NOTE 3 $\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$ and mode inputs	4	All		8.0	pF
Digital Output High Level Voltage	V _{OH}	DB0-DB7, $\overline{\text{OFL}}$ and $\overline{\text{INT}}$ outputs I _{SOURCE} =360μA	1,2,3	All	4.0		V
Digital Output Low Level Voltage	V _{OL}	DB0-DB7, $\overline{\text{OFL}}$ and $\overline{\text{INT}}$ outputs I _{SINK} =1.6mA	1,2,3	All		0.4	V
Floating State Leakage Current	I _{OUT}	DB0-DB7	1,2,3	All		±3.0	μA
Digital Output Capacitance	C _{OUT}	NOTE 3	4	All		8.0	pF
Supply Current from V _{DD}	I _{DD}	$\overline{\text{CS}}$ = $\overline{\text{RD}}$ =0V	1,2,3	All		20.0	mA
Power Supply Sensitivity	PSS	V _{DD} =5.0V±5%	1,2,3	All		±.25	LSB
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ / $\overline{\text{WR}}$ Setup Time	t _{CSS}	NOTE 6 and 7	9,10,11	All	0		ns
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ / $\overline{\text{WR}}$ Hold Time	t _{CSH}	NOTE 6 and 7	9,10,11	All	0		ns
$\overline{\text{CS}}$ to RDY delay	t _{RDY}	NOTE 6 and 7, CL=50pF, pull-up resistor=2.0kΩ	9 10,11	All		70 100	ns

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T _A ≤ +125°C <u>1</u> / <u>2</u> / Unless otherwise specified					
___ Conversion Time (RD mode)	t _{CRD}	See Figure 3 in Commercial Datasheet. NOTE 7	9 10,11	All		1.6 2.5	μs
___ Data Access Time (RD mode)	t _{ACCO}	NOTE 4 and 7	9 10,11	All		1.62 2.55	μs
___ RD to INT Delay (RD mode)	t _{INTH}	NOTE 7, CL=50pF	9 10,11	All		175 225	ns
Data Hold Time	t _{DH}	NOTE 5, 6, 7	9 10,11	All		60 100	ns
Delay Time Between Conversion	t _p	NOTE 6, 7	9 10,11	All	500 600		ns
Write Pulse Width	t _{WR}	NOTE 6	9,10,11	All	0.6	50	μs
Delay Time between ___ WR and RD Pulses	t _{RD}	NOTE 6	9 10,11	All	600 700		ns
Delay Access Time ___ WR/RD mode	t _{ACC1}	NOTE 4, 6	9 10,11	All		160 250	ns
___ RD to INT delay	t _{R1}	NOTE 6	9 10,11	All		140 225	ns
___ WR to INT delay	t _{INTL}	NOTE 6, CL=50pF	9 10,11	All		1.0 1.7	μs
Data Access Time ___ WR/RD mode	t _{ACC2}	NOTE 4, 6	9 10,11	All		70 110	ns
___ WR to INT delay, Stand alone operation	t _{IHWR}	NOTE 6, CL=50pF	9 10,11	All		100 150	ns
Data access time ___ after INT Stand alone operation	t _{ID}	NOTE 6	9 10,11	All		50 75	ns

NOTE 1: V_{DD}=+5V, VREF(+)=+5V; VREF(-)=GND=0V, unless otherwise specified. ___

Specifications apply for RD mode (pin 7=0V).

NOTE 2: All input control signals are specified with tr=tf=20ns (10 percent to 90 percent of +5.0V) and timed from a voltage level of 1.6V.

NOTE 3: Tested at initial release and upon redesign. Sample size will be 116 units.

NOTE 4: Measured with load circuits of Figure 2 in the Commercial Datasheet and defined as the time required for an output to cross 0.8V to 2.4V.

NOTE 5: Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figures 2 in the Commercial Datasheet and is measured only for the initial test and after process or design changes which may affect t_{DH}.

NOTE 6: Refer to timing diagrams of Figure 3 of Commercial Datasheet. These parameters, if not tested, shall be guaranteed to the limits specified in Table 1.

NOTE 7: Refer to timing diagram of Figure 3 (RD mode). These parameters are tested to Subgroup 9 under Group A test requirements.

TERMINAL CONNECTIONS

	J20, L20		J20, L20
1	V _{IN}	11	VREF-
2	DB0(LSB)	12	VREF+
3	DB1	13	CS
4	DB2	14	DB4
5	DB3	15	DB5
6	$\overline{\text{WR/RDY}}$	16	DB6
7	Mode	17	DB7(MSB)
8	$\overline{\text{RD}}$	18	$\overline{\text{OFL}}$
9	$\overline{\text{INT}}$	19	NC
10	GND	20	V _{DD}

	Package	ORDERING INFORMATION:	SMD NUMBER
01	20 pin Cerdip	MX7820UQ/883B	5962-8865001RA
01	20 pin LCC	MX7820UE/883B	5962-88650012C
02	20 pin Cerdip	MX7820TQ/883B	5962-8865002RA
02	20 pin LCC	MX7820TE/883B	5962-88650022C

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4**, 9, 10, 11***
Group A Test Requirements Method 5005	1, 2, 3, 4**, 9, 10, 11***
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4, Capacitance tests are performed at initial qual and upon redesign.
Sample size will be 116 units.

*** Subgroups 10 and 11 if not tested, are guaranteed to the limits specified in Table 1.