SCOPE: CMOS, COMPLETE, HIGH-SPEED, 12-BIT A/D CONVERTER

Device Type	Generic Number
01	MX7572S(x)12/883B
02	MX7572S(x)05/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
Q	GDIP1-T24 or CDIP2-T24	24 LEAD CERDIP	J24
E	CQCC1-N28	28 LCC	L28

Absolute Maximum Ratings:

V_{DD} to DGND ..... -0.3V to 7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V, (V_{DD}+0.3V)
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V, (V_{DD}+0.3V)
Digital Output Voltage to DGND ..... -0.3V, (V_{DD}+0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
24 pin CERDIP(derate 12.5mW/°C above +70°C) 1000mW
28 pin LCC(derate 10.2mW/°C above +70°C) 816mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
24 pin CERDIP..... 40°C/W
28 pin LCC ..... 15°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
24 pin CERDIP..... 80°C/W
28 pin LCC ..... 98°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V_{DD}) ..... +4.75V dc to +5.25V dc
Negative Supply Voltage (V_{SS}) ..... -14.25V dc to +15.75V dc
Clock Frequency (f_{CLK}) device 01 ..... 1.0MHz
Clock Frequency (f_{CLK}) device 02 ..... 2.5MHz
Analog Input Voltage Range (AIN)
(specifications apply to slow memory mode) ..... 0 to 5.0V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C 1/ V_{DD}=+5V, V_{SS}=-15V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Resolution NOTE 2	RES			All	12		Bits
Integral Nonlinearity	INL		1,2,3	All		±1.0	LSB
Differential Nonlinearity	DNL		1,2,3	All		±1.0	LSB
Offset Error	VOS		1 2,3	All		±4 ±6	LSB
Full Scale Error	AE	Full Scale = 5V, including internal voltage reference error, (Ideal last code transition=FS-3/2LSB's)	1	All		±15	LSB
Full Scale Temperature Coefficient	ΔAE/ΔT	Guaranteed by internal reference temperature coefficient tests; includes internal voltage reference drift.	2,3	All		45	ppm/°C
Analog Input Current	I_{IN}	AIN=5V	1,2,3	All		3.5	mA
Internal Reference Voltage Output	VREF		1	All	-5.3	-5.2	V
Internal Reference Output Current Sink Capability		Constant external load during conversion	13,14,15	All		550	µA
Digital Input Low Voltage	V_{INL}	V_{DD}=4.75V, V_{SS}=-15V, $\overline{HBEN}$, CLK IN, $\overline{CS}$, $\overline{RD}$	1,2,3	All		0.8	V
Digital Input High Voltage	V_{INH}	V_{DD}=4.75V, V_{SS}=-15V, $\overline{HBEN}$, CLK IN, $\overline{CS}$, $\overline{RD}$	1,2,3	All	2.4		V
Digital Input Capacitance	C_{IN}	V_{DD}=4.75V, V_{SS}=-15V, $\overline{HBEN}$, CLK IN, $\overline{CS}$, $\overline{RD}$	13	All		10	pF
Digital Input Current	I_{IN}	V_{DD}=5.25V, V_{SS}=-15V, $\overline{HBEN}$, CLK IN, $\overline{CS}$, $\overline{RD}$ AIN=0V to V_{DD}	1,2,3	All	-10	10	µA
		CLK IN, V_{DD}=5.25V, V_{SS}=-15V, AIN=0V to V_{DD}			-20	20	
Digital Output Low Voltage	V_{OL}	I_{SINK}=1.6mA, BUSY, CLK OUT, V_{DD}=4.75V, V_{SS}=-15V, D11-D0/8	1,2,3	All		0.4	V
Digital Output High Voltage	V_{OH}	I_{SOURCE}=200µA, BUSY, CLK OUT, V_{DD}=4.75V, V_{SS}=-15V, D11-D0/8	1,2,3	All	4.0		V
Floating State Leakage Current	I_{LKG}	D11-D0/8, V_{DD}=5.25V, V_{SS}=-15V	1,2,3	All	-10	10	µA
Floating State Output Capacitance NOTE 2	C_{OUT}		13,14,15	All		15	pF
Conversion Time Using Synchronous Clock	t_{CONV}		13,14,15	01 02		12.5 5.0	µs
Conversion Time Using Asynchronous Clock	t_{CONV}		9,10,11	01 02	12.0 4.8	13.0 5.2	µs
Positive Supply Current	I_{DD}	VDD=5.25V, VSS=-15.75V, $\overline{CS}$=$\overline{RD}$=$\overline{BUSY}$=HIGH, AIN=5V	1,2,3	All		7.0	mA

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C 1/ V_{DD}=+5V, V_{SS}=-15V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Negative Supply Current	I_{SS}	V_{DD}=5.25V, V_{SS}=-15.75V, $\overline{CS}$=$\overline{RD}$=$\overline{BUSY}$=HIGH, AIN=5V	1,2,3	All		12.0	mA
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1	NOTE 3	9,14,15	All	0		ns
$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay	t_2	NOTE 3	9 14,15	All		190 270	ns
Data-Access Time $\overline{RD}$ after $\overline{RD}$	t_3	CL=60pF, NOTE 3, 4, 5	9 14,15	All		110 150	ns
		CL=100pF, NOTE 3, 5	9 14,15			125 170	
$\overline{RD}$ Pulse Width	t_4	NOTE 3	9,14,15	All	t_3		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5	NOTE 3	9,14,15	All	0		ns
Data-Setup Time after $\overline{BUSY}$	t_6	CL=60pF, NOTE 3, 5	9 14,15	All		70 100	ns
Bus-Relinquish Time	t_7	NOTE 3, 6	9 14,15	All	35 20	90 90	ns
$\overline{HBEN}$ to $\overline{RD}$ Setup Time	t_8	NOTE 3	9,14,15	All	0		ns
$\overline{HBEN}$ to $\overline{RD}$ Hold Time	t_9	NOTE 3	9,14,15	All	0		ns
Delay Between Successive Read Operations	t_{10}	NOTE 3	9,14,15	All	500		ns

NOTE 1: V_{DD}=+5V, V_{SS}=-15V, AIN=0V to +5V, slow-memory mode, f_{CLK}=1.0MHz for -01 and f_{CLK}=2.5MHz for -02, unless otherwise specified.

NOTE 2: Characteristics supplied for use as a typical design limit but not production tested.

NOTE 3: All input control signals are specified with tr=tf=5ns (10% to 90% of +5V) and timed from a 1.6V voltage level. Times t_6 and t_{10} are measured only for the initial test and after process or design changes which may affect switching parameters.

NOTE 4: If not tested, shall be guaranteed to the limits specified in Table 1, herein.

NOTE 5: Times t_3 and t_6 are measured with the load circuits of Figure 2 in the commercial datasheet and defined as the time required for an output to cross 0.8V or 2.4V.

NOTE 6: Time t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 3 in the commercial datasheet.

ORDERING INFORMATION:

	Package	Pkg. Code	MAXIM PART #	SMD Number
01	24 pin CERDIP	J24	MX7572SQ12/883B	5962-8759101LA
01	28 pin LCC	L28	MX7572SE12/883B	5962-87591013C
02	24 pin CERDIP	J24	MX7572SQ05/883B	5962-8759104LA
02	28 pin LCC	L28	MX7572SE05/883B	5962-87591043C

TERMINAL CONNECTIONS:

	J24	L28
Pin		
1	AIN	NC
2	VREF	AIN
3	AGND	VREF
4	D11	AGND
5	D10	D11
6	D9	D10
7	D8	D9
8	D7	NC
9	D6	D8
10	D5	D7
11	D4	D6
12	DGND	D5
13	D3/11	D4
14	D2/10	DGND
15	D1/9	NC
16	D0/8	D3/11
17	CLK IN	D2/10
18	CLK OUT	D1/9
19	HBEN	D0/8
20	$\overline{RD}$	CLK IN
21	$\overline{CS}$	CLK OUT
22	$\overline{BUSY}$	NC
23	V_{SS}	HBEN
24	V_{DD}	$\overline{RD}$
25		$\overline{CS}$
26		$\overline{BUSY}$
27		V_{SS}
28		V_{DD}

SLOW MEMORY MODE				
PARALLEL READ DATA-BUS STATUS		**TWO-BYTE READ DATA-BUS STATUS**		
DATA OUTPUTS	**READ**	**DATA OUTPUTS**	**FIRST READ**	**SECOND READ**
D11	DB11	D7	DB7	LOW
D10	DB10	D6	DB6	LOW
D9	DB9	D5	DB5	LOW
D8	DB8	D4	DB4	LOW
D7	DB7	D3/D11	DB3	DB11
D6	DB6	D2/D10	DB2	DB10
D5	DB5	D1/D9	DB1	DB9
D4	DB4	D0/D8	DB0	DB8
D3/D11	DB3			
D2/D10	DB2			
D1/D9	DB1			
D0/D8	DB0			

ROM MODE						
PARALLEL READ DATA BUS STATUS			**TWO-BYTE READ DATA BUS STATUS**			
DATA OUTPUTS	**FIRST READ (OLD DATA)**	**SECOND READ**	**DATA OUTPUTS**	**FIRST READ (OLD DATA)**	**SECOND READ**	**THIRD READ**
D11	DB11	DB11	D7	DB7	LOW	DB7
D10	DB10	DB10	D6	DB6	LOW	DB6
D9	DB9	DB9	D5	DB5	LOW	DB5
D8	DB8	DB8	D4	DB4	LOW	DB4
D7	DB7	DB7	D3/D11	DB3	DB11	DB3
D6	DB6	DB6	D2/D10	DB2	DB10	DB2
D5	DB5	DB5	D1/D9	DB1	DB9	DB1
D4	DB4	DB4	D0/D8	DB0	DB8	DB0
D3/D11	DB3	DB3				
D2/D10	DB2	DB2				
D1/D9	DB1	DB1				
D0/D8	DB0	DB0				

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 4**, 5, 6 , 9, 10, 11, 13**, 14, 15
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Special subgroups 13, 14, 15 shall be measured only for initial test and after process or design changes and shall be guaranteed to the limits specified in Table 1. Subgroup 13 is +25°C, Subgroup 14 is +125°C and Subgroup 15 is -55°C.