SCOPE: CMOS, 12-BIT BUFFERED, MULTIPLYING D/A CONVERTER

Device Type	Generic Number
01	MX7545S(x)/883B
02	MX7545T(x)/883B
03	MX7545U(x)/883B
04	MX7545GU(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter		Mil-Std-1835	Case Outline	Package Code
MAXIM	SMD			
Q	R	GDIP1-T20 or CDIP2-T20	20 LEAD CERDIP	J20
E	2	CQCC1-N20	20 LCC	L20

Absolute Maximum Ratings:

V_{REF} to GND ..... -0.3V, + 17V
Digital Input to DGND ..... -0.3V to V_{DD}
V_{RFB} to GND ..... ±25V
V_{REF} to GND ..... ±25V
V_{OUT1} to AGND ..... -0.3V to V_{DD}
AGND to DGND ..... -0.3V to V_{DD}

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
20 pin CERDIP(derate 11.1mW/°C above +70°C) 889mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
20 pin CERDIP..... 40°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
20 pin CERDIP..... 90°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Supply Voltage Range ..... +5V to +15V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Resolution NOTE 4	RES	V_{DD}=+5V and +15V		All	12		Bits
Relative Accuracy	RA	V_{DD}=+5V and +15V	1,2,3	01 02 03,04		±2.0 ±1.0 ±0.5	LSB
Differential Nonlinearity	DNL	10-bit monotonic, V_{DD}=+5V and +15V 12-bit monotonic, V_{DD}=+5V and +15V	1,2,3	01 02,03,04		±4.0 ±1.0	LSB
Gain Error NOTE 3	AE	V_{DD}=5V	1,2,3	01 02		±20 ±10	LSB
			1 2,3	03		±5.0 ±6.0	
			1 2,3	04		±1.0 ±2.0	
Gain Error NOTE 3	AE	V_{DD}=15V	1,2,3	01 02 03		±25 ±15 ±10	LSB
			1 2,3	04		±6.0 ±7.0	
Gain Temperature Coefficient NOTE 4	TC_{AE}	V_{DD}=+5V V_{DD}=+15V		All		±5 ±10	ppm/°C
Power Supply Rejection	PSRR	ΔV$_{DD}$=±5%, V_{DD}=5V	1 2,3	All		±0.015 ±0.03	%/%
		ΔV$_{DD}$=±5%, V_{DD}=15V	1 2,3			±0.01 ±0.02	
Out1 Leakage Current	I_{OUT1}	V_{DD}=+5V & +15V, ___ __ D0-D11=0V, WR=CS=0V	1 2,3	All		±10 ±200	nA
Feedthrough Error NOTE 4, NOTE 5	FTE	VREF=±10V, 10kHz sine wave V_{DD}=5V VREF=±10V, 10kHz sine wave V_{DD}=15V	4,5,6	All		10	mVp-p
Input Resistance	R_{IN}	V_{DD}=+5V and +15V	1,2,3	All	7	25	kΩ
Digital Input High Voltage	V_{IH}	V_{DD}=+5V V_{DD}=+15V	1,2,3	All	2.4 13.5		V
Digital Input Low Voltage	V_{IL}	V_{DD}=+5V V_{DD}=+15V	1,2,3	All		0.8 1.5	V

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Digital Input Leakage Current	I_{IN}	V_{IN}=0V or V_{DD} V_{DD}=+5V or +15V	1 2,3	All		±1.0 ±10	µA
Digital Input Capacitance NOTE 2, NOTE 6	C_{IN}	D0-D11, V_{DD}=5V	4	All		5	pF
		$\overline{WR}$, $\overline{CS}$, V_{DD}=5V				20	
		D0-D11, V_{IN}=0V, V_{DD}=15V				5	
		$\overline{WR}$, $\overline{CS}$, V_{IN}=0V, V_{DD}=15V				20	
Output Capacitance NOTE 2, NOTE 6	C_{OUT1}	V_{DD}=5V D0-D11=0V, $\overline{WR}$, $\overline{CS}$=0V	4	All		70	pF
		V_{DD}=5V D0-D11=V_{DD}, $\overline{WR}$, $\overline{CS}$=0V				200	
		V_{DD}=15V D0-D11=0V, $\overline{WR}$, $\overline{CS}$=0V				70	
		V_{DD}=15V D0-D11=V_{DD}, $\overline{WR}$, $\overline{CS}$=0V				200	
Chip Select to Write-Setup Time NOTE 7	t_{CS}	V_{DD}=5V V_{DD}=15V	9,10,11	All	170 95		ns
Chip Select to Write-Hold Time NOTE 7	t_{CH}	V_{DD}=+5V and +15V	9,10,11	All	0		ns
Write Pulse Width NOTE 7	t_{WR}	t_{CS}±t_{WR}, t_{CH}±0, V_{DD}=+5V t_{CS}≥t_{WR}, t_{CH}≥0, V_{DD}=15V	9,10,11	All	170 95		ns
Data-Setup Time NOTE 7	t_{DS}	V_{DD}=5V V_{DD}=15V	9,10,11	All	150 80		ns
Data-Hold Time NOTE 7	t_{DH}	V_{DD}=+5V and +15V	9,10,11	All	5		ns
Supply Current	I_{DD}	All digital inputs V_{IL} or V_{IH} V_{DD}=+5V and +15V	1,2,3	All		2.0	mA
		All digital inputs 0V or V_{DD} V_{DD}=+5V and +15V	1 2,3			100 500	µA

NOTE 1: V_{DD}=+15V, V_{OUT1}=0V; VREF=+10V, AGND=DGND, unless otherwise specified.
NOTE 2: These parameters may be guaranteed if not tested at 25°C to the limits specified in Table 1.
NOTE 3: Measured using internal feedback resistor and includes effect of 5ppm max gain TC.
NOTE 4: These parameters may be guaranteed if not tested over the full military temp range to the limits specified in Table 1.
NOTE 5: Feedthrough error can be reduced by connecting the metal lid on the package to ground.
NOTE 6: Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance.
NOTE 7: Timing Diagram. See Commercial Datasheet.

ORDERING INFORMATION:

	Package	Pkg. Code	MAXIM PART #	SMD Number
01	20 pin CERDIP	J20	MX7545SQ/883B	5962-8770201RA
01	20 pin LCC	L20	MX7545SE/883B	5962-87702012C
02	20 pin CERDIP	J20	MX7545TQ/883B	5962-8770202RA
02	20 pin LCC	L20	MX7545TE/883B	5962-87702022C
03	20 pin CERDIP	J20	MX7545UQ/883B	5962-8770203RA
03	20 pin LCC	L20	MX7545UE/883B	5962-87702032C
04	20 pin CERDIP	J20	MX7545GUQ/883B	5962-8770204RA
04	20 pin LCC	L20	MX7545GUE/883B	5962-87702042C

TERMINAL CONNECTIONS:

	J20 & L20
Pin	
1	OUT1
2	AGND
3	DGND
4	D11(MSB)
5	D10
6	D9
7	D8
8	D7
9	D6
10	D5
11	D4
12	D3
13	D2
14	D1
15	D0(LSB)
16	$\overline{CS}$
17	$\overline{WR}$
18	V_{DD}
19	VREF
20	R_{FB}

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3
Group A Test Requirements Method 5005	1, 2, 3, 4**, 5, 6, 9, 10***, 11***
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 116 units.
*** Subgroups 10 and 11, if not tested shall be guaranteed to the specified limits of Table 1.