SCOPE: CMOS 12-BIT MULTIPLYING D/A CONVERTER

Device Type	Generic Number
01	MX7521S(x)/883B
02	MX7521T(x)/883B
03	MX7521U(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
MAXIM			
Q	GDIP1-T18 or CDIP2-T18	18 LEAD CERDIP	J18
E	CQCCI-N20	20 LEADLESS CHIP CARRIER	L20

Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V, +17V
V_{OUT1}, V_{OUT2}, to GND ..... -0.3V, V_{DD}
VREF to GND..... -25V to +25V
V_{RFB} to GND..... -25V to +25V
Digital Input Voltage Range ..... -0.3V,V_{DD}

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
18 pin CERDIP(derate 10.5mW/°C above +70°C) 842mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
18 pin CERDIP..... 45°C/W
20 pin LCC ..... 50°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
18 pin CERDIP..... 95°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Resolution	RES	NOTE 2		All	12		Bits
Relative Accuracy	RA		1,2,3	01 02 03	-8.0 -4.0 -2.0	+8.0 +4.0 +2.0	LSB
Nonlinearity Tempco	TC_{NL}	NOTE 2	1,2,3	All	-2.0	+2.0	ppm/°C
Gain Tempco	TC_{AE}	NOTE 2	1,2,3	All	-20	+20	ppm/°C
OUT1 Leakage Current	I_{OUT1}	Digital inputs at V_{IL}, VREF=+10V	1,2,3	All	-200	200	nA
OUT2 Leakage Current	I_{OUT2}	Digital inputs at V_{IH}, VREF=+10V	1,2,3	All	-200	200	nA
Output Current Settling Time NOTE 2		To ±0.5LSB, OUT1 load is 100Ω||13pF. Digital inputs = V_{IH} to V_{IL} or V_{IL} to V_{IH}.	4	All		0.5	µs
Feedthrough Error NOTE 3	FTE	VREF=20Vp-p at 10kHz sine wave, digital inputs at V_{IL}	4			30	mVp-p
Reference Input Resistance	R_{IN}		1,2,3	All	5	20	kΩ
Input High Level Voltage	V_{IH}		1,2,3	All	2.4		V
Input Low Level Voltage	V_{IL}		1,2,3	All		0.8	V
Input Leakage Current	I_{IL}	V_{IN}=0V or V_{DD}	1,2,3	All	-1.0	1.0	µA
Output Capacitance	C_{OUT1}	Digital Inputs at V_{IH} Digital Inputs at V_{IL}	4	All		120 37	pF
	C_{OUT2}	Digital Inputs at V_{IH} Digital Inputs at V_{IL}				37 120	
Supply Current	I_{DD}	Digital Inputs at V_{IH} or V_{IL}	1,2,3	All		2	mA

NOTE 1: V_{DD}=+15V, V_{OUT1}=V_{OUT2}=0V, VREF=+10V, unless otherwise specified.
NOTE 2: Characteristics supplied for use as a typical design limit but not production tested.
NOTE 3: Feedthrough error can be reduced by connecting the lid of the ceramic SB package to ground.

TERMINAL CONNECTIONS

	J18, D18	20 LCC		J18, D18	20 LCC
1	OUT1	NC	11	D8	NC
2	OUT2	OUT1	12	D9	D7
3	GND	OUT2	13	D10	D8
4	D1(MSB)	GND	14	D11	D9
5	D2	D1(MSB)	15	D12(LSB)	D10
6	D3	D2	16	V_{DD}	D11
7	D4	D3	17	VREF	D12(LSB)
8	D5	D4	18	R_{FB}	V_{DD}
9	D6	D5	19		VREF
10	D7	D6	20		R_{FB}

	Package	ORDERING INFORMATION:
01	18 pin CERDIP	MX7521SQ/883B
01	20 pin LCC	MX7521SE/883B
02	18 pin CERDIP	MX7521TQ/883B
02	20 pin LCC	MX7521TE/883B
03	18 pin CERDIP	MX7521UQ/883B
03	20 pin LCC	MX7521UE/883B

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4**
Group A Test Requirements Method 5005	1, 2, 3, 4**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroup 4, Capacitance tests are performed at initial qual and upon redesign. Sample size will be 116 units.