SCOPE: 12-BIT A/D CONVERTER

Device Type	Generic Number
01	MX674ASQ/883B
02	MX674ATQ/883B
03	MX674AUQ/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter		Mil-Std-1835	Case Outline	Package Code
Q	X	GDIP1-T28 or CDIP2-T28	28 Lead CERDIP	J28

Absolute Maximum Ratings

V_{CC} to DGND ..... 0V to +16.5V
V_{EE} to DGND ..... 0V to -16.5V
V_L to DGND ..... 0V to +7V
DGND to AGND ..... ±1V
Control Inputs to DGND
(CE, A0, 12/$\overline{8}$, R/$\overline{C}$, $\overline{CS}$) ..... -0.3V to V_{CC} +0.3V
Digital Output Voltage to DGND(DB11-DB0, STS) ..... -0.3V to V_L +0.3V
Analog Inputs (REF IN, BIP OFF, 10 V_{IN}) to AGND ..... ±16.5V
20 V_{IN} analog input voltage to AGND ..... ±24V
REF OUT .....Indefinite short to V_{CC} or AGND
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Continuous Power Dissipation ..... T_A=+70°C
28 pin CERDIP(derate 16.7mW/°C above +70°C) 1333mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
28 pin CERDIP..... 25°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
28 pin CERDIP..... 60°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
V_L ..... +5V
V_{CC} ..... +15V or +12V
V_{EE} ..... -15V or -12V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C V_{CC}=+15V or +12V, V_{LOGIC}=5V, V_{EE}=-15V or -12V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
ACCURACY							
Resolution	RES		1	All	12		Bits
Integral Nonlinearity	INL		1,2,3 1 2,3	01 02,03		±1.0 ±0.5 ±0.75	LSB
Differential Nonlinearity	DNL	12 bits, no misssing codes over temp.	1	All		±1.0	LSB
Unipolar Offset Error		NOTE 1	1	01 02,03		±2.0 ±1.0	LSB
Bipolar Offset Error		NOTES 2, 3	1	01,02 03		±4.0 ±2.0	LSB
Full-Scale Calibration Error		NOTE 3	1	All		0.25	%
TEMPERATURE COEFFICIENTS		Using Internal Reference NOTES 2, 3, 4					
Unipolar Offset Change			1,2,3	01 02,03		±2.0 ±1.0	LSB
Biplar Offset Change			1,2,3	01 02 03		±4.0 ±2.0 ±1.0	LSB
Full-Scale Calibration Change			1,2,3	01 02 03		±20 ±10 ±5	LSB
INTERNAL REFERENCE							
Output Voltage		No Load	1	01,02 03	9.97 9.99	10.03 10.01	V
Output Current		Available for external loads, in addition to REFIN and BIPOFF load. NOTE 5	1	All		2.0	mA
ANALOG INPUT							
Bipolar Input Range		Using 10V input Using 20V input	1	All		±5 ±10	V
Unipolar Input Range		Using 10V input Using 20V input	1	All	0 0	+10 +20	V
Input Impedance		10V input 20V input	1	All	3 6	7 14	kΩ
POWER-SUPPLY REJECTION		Max change in Full-scale calibration					
V_{CC} only		+15V±1.5V or +12V±0.6V	1	01 02,03		±2 ±1	LSB
V_{EE} only		-15V±1.5V or -12V±0.6V	1	All		±0.5	LSB
V_L only		+5V±0.5V	1	All		±0.5	LSB

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C V_{CC}=+15V or +12V, V_{LOGIC}=5V, V_{EE}=-15V or -12V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$	1	All		0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$	1	All	2.0		V
Input Current	I_{IN}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$, VIN=0 to V_L	1	All		±5	µA
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	DB11-DB0, STS, I_{SINK}=1.6mA	1	All		0.4	V
Output High Voltage	V_{OH}	DB11-DB0, STS, I_{SOURCE}=500µA	1	All	4.0		V
Floating State Leakage Current	I_{LKG}	DB11-DB0, STS, V_{OUT}=0 to V_L	1	All		±10	µA
CONVERSION TIME							
12-Bit Cycle	t_{CONV}		9	All	9	15	µs
8-Bit Cycle	t_{CONV}		9	All	6	11	µs
POWER REQUIREMENTS							
V_{CC} Operating Range			1	All	11.4	16.5	V
V_L Operating Range			1	All	4.5	5.5	V
V_{EE} Operating Range			1	All	-11.4	-16.5	V
V_{CC} Supply Current	I_{CC}	NOTE 5	1	All		5	mA
V_L Supply Current	I_L	NOTE 5	1	All		8	mA
V_{EE} Supply Current	I_{EE}	NOTE 5	1	All		10	mA
Power Dissipation	P_D	V_{CC}=+15V and V_{EE}=-15V NOTE 5	1	All		265	mW
CONVERT START TIMING		**FULL CONTROL MODE NOTE 6**					
STS Delay from CE	t_{DSC}	CL=50pF	9 10,11	All		200 320	ns
CE Pulse Width	t_{HEC}		9,10,11	All	50		ns
$\overline{CS}$ to CE Setup	t_{SSC}		9,10,11	All	50		ns
$\overline{CS}$ Low During CE high	t_{HSC}		9,10,11	All	50		ns
R/$\overline{C}$ to CE Setup	t_{SRC}		9,10,11	All	50		ns
R/$\overline{C}$ Low During CE high	t_{HRC}		9,10,11	All	50		ns
A0 to CE Setup	t_{SAC}		9,10,11	All	0		ns
A0 Valid During CE high	t_{HAC}		9,10,11	All	50		ns
READ TIMING		**FULL CONTROL MODE 6/**					
Access Time (from CE)	t_{DD}	CL=100pF	9 10,11	All		120 200	ns

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C V_{CC}=+15V or 12V, V_{LOGIC}=5V, V_{EE}=-15V or -12V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Data Valid after CE low	t_{HD}		9 10,11	All	25 15		ns
Output Float Delay	t_{HL}		9 10,11	All		75 120	ns
$\overline{CS}$ to CE Setup	t_{SSR}		9,10,11	All	50		ns
$\overline{R/C}$ to CE Setup	t_{SRR}		9,10,11	All	0		ns
A0 to CE Setup	t_{SAR}		9,10,11	All	50		ns
$\overline{CS}$ to Valid after CE Low	t_{HSR}		9,10,11	All	0		ns
$\overline{R/C}$ High After CE Low	t_{HRR}		9,10,11	All	0		ns
A0 Valid After CE Low	t_{HAR}		9,10,11	All	0		ns
STAND-ALONE MODE		**NOTE 6**					
Low $\overline{R/C}$ Pulse Width	t_{HRL}		9,10,11	All	50		ns
STS Delay from $\overline{R/C}$	t_{DS}		9 10,11	All		200 320	ns
Data Valid from $\overline{R/C}$ Low	t_{HDR}		9 10,11	All	25 15		ns
STS Delay After Data Valid	t_{HS}		9,10,11	All	30	600	ns
High $\overline{R/C}$ Pulse Width	t_{HRH}		9 10,11	All	150 200		ns
Data Access Time	t_{DDR}	C_L=100pF	9 10,11	All		120 200	ns

NOTE 1: Adjustable to zero

NOTE 2: With 50Ω fixed resistor from REFOUT to BIPOFF. Adjustable to zero.

NOTE 3: With 50Ω fixed resistor from REFOUT to REFIN. Adjustable to zero.

NOTE 4: Maximum change in specification from T_A=+25°C to T_{MIN} or T_A=+25°C to $T_{MAX.}$

NOTE 5: External load current should not change during a conversion. For ±12V supply operation, REFOUT need not be buffered except when external load in addition to REFIN and BIPOFF inputs have to be driven.

NOTE 6: Timing specifications guaranteed by design. All input control signals specified with tr=tf=5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. See loading circuits in Figures 1 and 2 in the Commercial data sheet.

	Package	ORDERING INFORMATION:
01	28 pin CERDIP	MX674ASQ/883B
02	28 pin CERDIP	MX674ATQ/883B
03	28 pin CERDIP	MX674AUQ/883B

TRUTH TABLE:					
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-bit conversion
1	0	0	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit parallel output
1	0	1	0	0	Enable 8 most significant bits
1	0	1	0	1	Enable 4 LSBs +4 trailing zeros

TERMINAL CONNECTIONS:

	J28		
1	V_{LOG}	15	DGND
2	$\overline{12/8}$	16	DB0
3	$\overline{CS}$	17	DB1
4	A0	18	DB2
5	R/$\overline{C}$	19	DB3
6	CE	20	DB4
7	V_{CC}	21	DB5
8	REF OUT	22	DB6
9	AGND	23	DB7
10	REFIN	24	DB8
11	V_{EE}	25	DB9
12	BIP OFF	26	DB10
13	10 V_{IN}	27	DB11(MSB)
14	20 V_{IN}	28	STS

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9**, 10**, 11**
Group A Test Requirements Method 5005	1, 2, 3, 9**, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroups 10 and 11, if not tested shall be guarnateed to the specified limits of Table 1. Conversion Time is tested for Subgroup 9 and Timing Specifications are guaranteed by design.