SCOPE: COMPLETE 12-BIT A/D CONVERTER WITH MICROPROCESSOR INTERFACE

Device Type	Generic Number
01	MX574AU(x)/883B
02	MX574AT(x)/883B
03	MX574AS(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter		Mil-Std-1835	Case Outline	Package Code
MAXIM	SMD			
D	X	CDIP2-T28	28 LEAD Sidebraze	D28
E	3	CQCC1-N28	28 Leadless Chip Carrier	L28
Q	X	GDIP1-T28	28 Lead CERDIP	J28

Absolute Maximum Ratings

V_{CC} to digital common ..... 0V dc to +16.5V dc
V_{EE} to digital common ..... 0V dc to -16.5V dc
V_{LOGIC} to digital common ..... 0V dc to +7V dc
Analog common to digital common ..... ±1V
Control Inputs to digital common
(CE, A0, 12/8, R/C, CS) ..... -0.5V dc to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, 10 V_{IN}) to Analog common ..... V_{EE} to V_{CC}
20 V_{IN} analog input voltage to analog common ..... ±24V dc
VREF OUT .....Indefinite short to common, momentary short to V_{CC}
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Continuous Power Dissipation ..... T_A=+70°C
28 pin CERDIP(derate 16.7mW/°C above +70°C) 1333mW
28 pin Sidebraze(derate 20mW/°C above +70°C) 1600mW
28 pin LCC (derate 10.2mW/°C above +70°C) 816mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
28 pin CERDIP..... 25°C/W
28 pin Sidebraze ..... 15°C/W
28 pin LCC ..... 15°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
28 pin CERDIP..... 60°C/W
28 pin Sidebraze ..... 50°C/W
28 pin LCC ..... 98°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Logic Supply Voltage (V_L) ..... +4.5V to +5.5V
Positive Supply Voltage (V_{CC}) ..... +11.4V to +16.5V
Negative Supply Voltage (V_{EE}) ..... -11.4V to -16.5V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤+125°C V_{CC}=+15V, V_{LOGIC}=5V, V_{EE}=-15V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Power Supply Current from V_{LOGIC}	I_{LOGIC}		1,2,3	All		40	mA
Power Supply Current from V_{CC}	I_{CC}		1,2,3	All		5	mA
Power Supply Current from V_{EE}	I_{EE}		1,2,3	All	-30		mA
Resolution	N		1,2,3	All	12		Bits
Integral Linearity error	ILE		1 2,3 1,2,3	01,02 03	-0.5 -1.0 -1.0	+0.5 +1.0 +1.0	LSB
Differential Linearity error	DLE	Minimum resolution for which no missing codes are guaranteed.	1,2,3	All	12		Bits
Unipolar Offset Error	V_{IO}		1	All	-2.0	+2.0	LSB
Unipolar Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	Using Internal Reference	2,3	01,02 03	-1.0 -2.0	+1.0 +2.0	LSB
Bipolar Zero Offset Error	BZ		1	All	-4.0	+4.0	LSB
Bipolar Zero Offset Drift	ΔBZ/ΔT	Using Internal Reference	2,3	01 02 03	-1.0 -2.0 -4.0	+1.0 +2.0 +4.0	LSB
Gain Error	AE	With 50Ω resistor from REF OUT to REF IN	1	All		0.25	%FSR
Gain Error Drift	ΔAE/ΔT	Using internal reference	2,3	01 02,03	-12.5 -25.0	12.5 25.0	ppm/°C
Power Supply Sensitivity to V_{CC} (Maximum change in full scale calibration)	+PSS1 +PSS2 +PSS3 -PSS1 -PSS2	+13.5V≤V_{CC}≤+16.5V +11.4V≤V_{CC}≤+12.6V +4.5V≤V_{CC}≤+5.5V -16.5V≤V_{CC}≤-13.5V -12.6V≤V_{CC}≤-11.4V	1	All	-1.0 -1.0 -0.5 -1.0 -1.0	+1.0 +1.0 -0.5 -1.0 -1.0	LSB
Input Impedence	ZIN	10V span 20V span	1,2,3	All	3.0 6.0	7.0 14.0	kΩ
Internal Reference Voltage NOTE 1	VREF		1	All	9.98	10.02	V
Input Voltage (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$) NOTE 3	V_{IH} V_{IL}	Logic “1” Logic “0”	1,2,3	All	+2.0 -0.5	+5.5 +0.8	V
Output Current NOTE 2	I_O	Available for external loads	1	All		1.5	mA
Input Current	I_{IN}		1	All	-20	+20	µA
Output Voltage (DB11-DB0, STS)	V_{OL}	Logic “0”, I_{SINK}=+1.6mA	1	All		+0.4	V
Output Voltage (DB11-DB0)	V_{OH}	Logic “1”, I_{SOURCE}=500µA	1	All	+2.4		V
High impedance state Output current	IZ	High-Z state (DB11-DB0 only)	1	All	-20	+20	µA
Functional Tests		Verify the truth tables	7	All			

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤+125°C V_{CC}=+15V, V_{LOGIC}=5V, V_{EE}=-15V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Low R/C Pulse Width	t_{HRL}	NOTE 4	9,10,11	All	250		ns
$\overline{R/C}$ STS delay from	t_{DS}	NOTE 4	9,10,11	All		600	ns
Data Valid after $\overline{R/C}$ Low	t_{HRD}	NOTE 4	9,10,11	All	25		ns
STS delay after data valid	t_{HS}	NOTE 4	9,10,11	All	300	1000	ns
$\overline{R/C}$ High pulse width	t_{HRH}	NOTE 5	9,10,11	All	300		ns
Data Access Time	t_{DDR}	NOTE 5	9,10,11	All		250	ns
STS delay from CE	t_{DSC}	NOTE 5	9,10,11	All		350	ns
CE pulse width	t_{HEC}	NOTE 5	9,10,11	All	300		ns
Conversion Time	t_C	8 bit cycle, NOTE 4 12-bit cycle, NOTE 4	9,10,11	All	10 15	24 35	µs
Access Time from CE	t_{DD}	NOTE 4	9,10,11	All		200	ns
Data Valid after CE low	t_{HD}	NOTE 4	9,10,11	All	25		ns
Output Float delay	t_{HL}	NOTE 4	9,10,11	All		100	ns

NOTE 1: The reference voltage external load current shall be a constant dc and shall not exceed 1.5mA.
NOTE 2: Reference should be buffered for operation on ±12V supplies. External load should not change during conversion.
NOTE 3: $\overline{12/8}$ is not TTL compatible and must be hard wired to V_{LOG} or digital common.
NOTE 4: Subgroup 10 and 11, if not tested, shall be guaranteed to the specified limits.
NOTE 5: Parameters t_{HRH}, t_{DDR}, t_{DSC}, and t_{HEC}, if not tested, shall be guaranteed to the specified limits.

	Package	ORDERING INFORMATION:	SMD NUMBER
01	28 pin CERDIP	MX574AUQ/883B	5962-8512701XA
01	28 pin Sidebraze	MX574AUD/883B	5962-8512701XC
02	28 pin LCC	MX574ATE/883B	5962-85127023A
02	28 pin Sidebraze	MX574ATD/883B	5962-8512702XC
02	28 pin CERDIP	MX574ATQ/883B	5962-8512702XA
03	28 pin CERDIP	MX574ASQ/883B	

TRUTH TABLE:					
CE	$\overline{CS}$	$\overline{R/C}$	$\overline{12/8}$	A0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-bit conversion
1	0	0	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit parallel output
1	0	1	0	0	Enable 8 most significant bits
1	0	1	0	1	Enable 4 LSBs +4 trailing zeros

TERMINAL CONNECTIONS:

	J28/D28/L28
1	V_{LOG}
2	$\overline{12/8}$
3	$\overline{CS}$
4	A0
5	$\overline{R/C}$
6	CE
7	V_{CC}
8	REF OUT
9	AGND
10	REFIN
11	V_{EE}
12	BIP OFF
13	10 V_{IN}
14	20 V_{IN}
15	DGND
16	DB0
17	DB1
18	DB2
19	DB3
20	DB4
21	DB5
22	DB6
23	DB7
24	DB8
25	DB9
26	DB10
27	DB11(MSB)
28	STS

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10**, 11**
Group A Test Requirements Method 5005	1, 2, 3, 7***, 9, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroups 10 and 11, if not tested shall be guarnateed to the specified limits of Table 1.
*** Subgroup 7: Verify the truth table.