SCOPE: HIGH SPEED 12-BIT MONOLITHIC D/A CONVERTER

Device Type	Generic Number
01	MX565AS(x)/883B
02	MX565AT(x)/883B
03	MX566AS(x)/883B
04	MX566AT(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
Q	GDIP1-T24 or CDIP2-T24	24 LEAD CERDIP	J24
D	GDIP1-T24 or CDIP2-T24	24 LEAD Sidebraze	D24

Absolute Maximum Ratings:

V_{CC} to Power Ground (-01, -02 only) ..... 0V, +18V
V_{EE} to Power Ground..... 0V, -18V
Voltage on DAC Output ..... -3V to +12V
Digital Inputs (pins 13 to 24) to Power Ground ..... -1V to +7V
REF IN to Reference Ground ..... ±12V
Bipolar Offset to Reference Ground ..... ±12V
10V Span R to Reference Ground ..... ±12V
20V Span R to Reference Ground ..... ±24V
REF OUT (-01, -02 only) Short Circuit to Power Ground ..... Continuous
Short to V_{CC} ..... Momentary

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
24 pin CERDIP(derate 12.5mW/°C above +70°C) 1000mW
24 pin Sidebraze(derate 14.3mW/°C above +70°C) 1143mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
24 pin CERDIP..... 40°C/W
24 pin Sidebraze ..... 25°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
24 pin CERDIP..... 80°C/W
24 pin Sidebraze ..... 70°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Logic Supply Voltage (V_{LOGIC}) ..... +4.5V to +5.5V
Positive Supply Voltage (V_{CC}) for -01, -02..... +15V
Negative Supply Voltage (V_{EE})..... -15V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{CC}=+15V (01,02), V_{EE}=-15V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Data Inputs (Pins 13-24)							Bits
Input Voltage Bit ON Logic "1" Bit OFF Logic "0"	 V_{IH} V_{IL}	NOTE 1 TTL or 5V CMOS	1,2,3	All	 +2.0 0	 +5.5 +0.8	V
Logic Current, each bit Bit ON Logic "1" Bit OFF Logic "0"	 I_{IH} I_{IL}	NOTE 1 TTL or 5V CMOS	1,2,3	All		 +300 +100	µA
Resolution			1	All		12	Bits
Output							
Output Current Unipolar Bipolar	I_{OUT}	 All bits ON All bits ON or OFF	1	All	 -1.6 -0.8	 -2.4 -1.2	mA
Output Resistance	R_{OUT}	Exclusive of span resistors	1	All	6	10	kΩ
Output Offset Unipolar Bipolar Bipolar	BPZE	 Adjustable to zero R1 and R2 = 50Ω fixed. R1 and R2 = 50Ω fixed.	1	All 01,03 02,04		0.05 0.15 0.10	% of F.S.
Output Compliance Voltage	CV		1,2,3	All	-1.5	+10	V
Accuracy	RA	Error relative to full scale	1 2,3	01,03		±0.50 ±0.75	LSB
Accuracy Resistance Match	RA	Error relative to full scale	1 2,3	02,04		±0.25 ±0.50	LSB
Differential Nonlinearity	DNL	Monotonicity guaranteed over temperature	1 2,3	01,03 02,04 All		±0.75 ±0.50 ±1.00	LSB
Temperature Coefficient							
Unipolar Zero Bipolar Zero	TCVOS TCBPZE	With Internal Reference for -01,-02	1,2,3	All		2 10	ppm/°C
Gain (Full Scale)	TCAE		1,2,3	01 02 03 04		30 15 10 5	ppm/°C
Full Scale Transition	t_{FS}	10% to 90% plus Rise Time 90% to 10% plus Fall Time NOTE 3	9	All		 30 50	ns
Settling Time to within ±0.5LSB	t_S	NOTE 3, All bits ON-to-OFF or OFF-to-ON	9	01,02 03,04		250 350	ns
Power Requirements							
+IPS -IPS -IPS	I_{CC} I_{EE}	11.4V>$\lvert V_{CC} \rvert$>16.5V 11.4V>$\lvert V_{EE} \rvert$>16.5V	1	01,02 03,04		5 -18 -20	mA
Power Dissipation	PD		1	01,02 03,04		345 300	mW

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{CC}=+15V (01,02), V_{EE}=-15V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
+V_{CC} Gain Sensitivity -V_{EE} Gain Sensitivity -V_{EE} Gain Sensitivity	PSRR	11.4V> $\lvert V_{CC} \rvert$ >16.5V, NOTE 2 11.4V> $\lvert V_{EE} \rvert$ >16.5V, NOTE 2 11.4V> $\lvert V_{EE} \rvert$ >16.5V	1 1 1	01,02 01,02 03,04		10 25 25	ppm of F.S./%
External Adjustments							
Gain Error with Fixed 50Ω Resistor	AE		1	All		±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω resistor	BPZE		1	01,03 02,04		±0.15 ±0.10	% of F.S.
Reference Input Impedance	R_{IN}		1	All	15	25	kΩ
Reference Output Voltage	VREF		1,2,3	01,02	9.9	10.10	V
Reference Output Current	IREF	Available for external loads	1	01,02	1.5		mA
Multiplying Mode Performance							
Quadrants		Two(2): Bipolar Operation at Digital Input Only.	1	03,04	See	Con-ditions	
Reference Voltage		+1V to +10V, Unipolar	1	03,04	See	Con-ditions	
Accuracy		10 Bits (±0.5% of reduced F.S.) for 1V DC Reference Voltage	1	03,04	See	Con-ditions	
Reference Feedthrough		Unipolar Mode, all bits OFF, and 1 to 10V[p-p] sinewave frequency for 0.5LSB[p-p] feedthrough)	1	03,04	See	Con-ditions	
Output Slew Rate		10%-90% 90%-10%	9	03,04	5.0 1.0		mA/µs
Output Settling Time		All bits ON and a 0-10V step change in reference voltage	9	03,04	1.5 to 0.01%		µs F.S.
Control Amplifier							
Full-Power Bandwidth Small-Signal Closed Loop Bandwidth		Full Power Small-Signal Closed-Loop	9	03,04	300 1.8		kHz MHz

NOTE 1: The digital input levels are guaranteed but not tested over the temperature range.
NOTE 2: The power supply gain sensitivity is tested in reference to a V_{CC} of +15V and V_{EE} of -15V.
NOTE 3: Sample tested at +25°C to ensure compliance.

ORDERING INFORMATION:

	Package	Pkg. Code	Device ID
01	24 pin Sidebraze	D24	MX565ASD/883B
01	24 pin CERDIP	J24	MX565ASQ/883B
02	24 pin Sidebraze	D24	MX565ATD/883B
02	24 pin CERDIP	J24	MX565ATQ/883B
03	24 pin Sidebraze	D24	MX566ASD/883B
03	24 pin CERDIP	J24	MX566ASQ/883B
04	24 pin Sidebraze	D24	MX566ATD/883B
04	24 pin CERDIP	J24	MX566ATQ/883B

TERMINAL CONNECTIONS:

	MX565	MX566
	J24/D24	J24/D24
1	NC	NC
2	NC	NC
3	VCC+15V	REFERENCE GND
4	REF OUT(+10V±1%)	AMP SUMMING JUNCTION
5	REFERENCE GND	REF V HI IN
6	REFERENCE IN	V_{EE}-15V IN(20mA)
7	V_{EE}-15V	Bipolar Offset R IN
8	BIPOLAR OFFSET IN	NC
9	DAC OUT (-2mA F S)	DAC OUT (-2mA F S)
10	10V SPAN R	10V SPAN R
11	20V SPAN R	20V SPAN R
12	POWER GND	POWER GND
13	BIT 12 (LSB) IN	BIT 12 (LSB) IN
14	BIT 11 IN	BIT 11 IN
15	BIT 10 IN	BIT 10 IN
16	BIT 9 IN	BIT 9 IN
17	BIT 8 IN	BIT 8 IN
18	BIT 7 IN	BIT 7 IN
19	BIT 6 IN	BIT 6 IN
20	BIT 5 IN	BIT 5 IN
21	BIT 4 IN	BIT 4 IN
22	BIT 3 IN	BIT 3 IN
23	BIT 2 IN	BIT 2 IN
24	BIT 1 (MSB) IN	BIT 1 (MSB) IN

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.