Industrial Grade MX27C8000

8M-BIT[1M x 8] CMOS EPROM

FEATURES

- 1M x 8 organization
- Single +5V power supply
- +12.5V programming voltage
- Fast access time: 120/150 ns
- Totally static operation

- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100µA
- Package type:
  - 32 pin ceramic DIP, plastic DIP
 - 32 pin PLCC/SOP

GENERAL DESCRIPTION

The MX27C8000 is a 5V only, 8M-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 1M words by 8 bits per word, operates from a single +5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27C8000 supports a intelligent quick pulse programming algorithm which can result in programming times of less than two minutes.
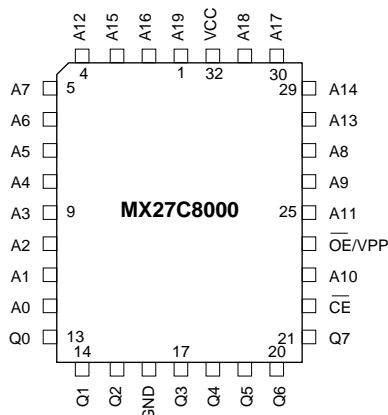
This EPROM is packaged in industry standard 32 pin dual-in-line packages, 32 lead PLCC packages, and 32 lead SOP packages.
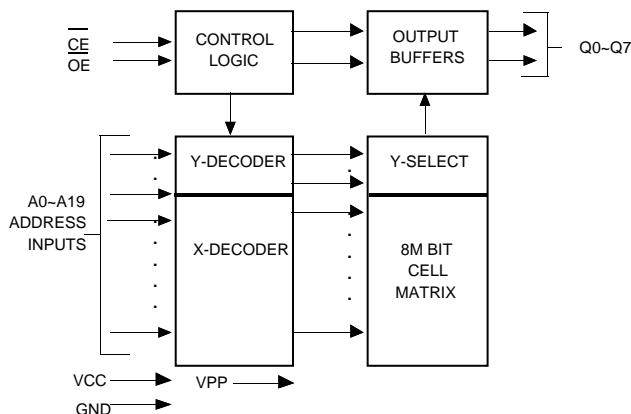
PIN CONFIGURATIONS

32 CDIP/PDIP/SOP
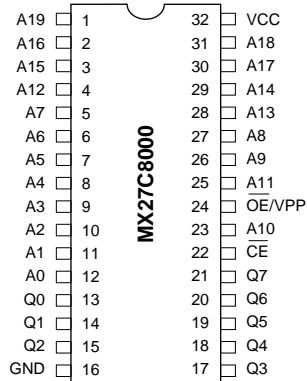
32 PLCC

BLOCK DIAGRAM

PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
OE/VPP	Output Enable Input/Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C8000, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

READ MODE

The MX27C8000 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$'s, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX27C8000 has a CMOS standby mode which reduces the maximum VCC current to 100 µA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27C8000 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

			PINS		
MODE	$\overline{CE}$	$\overline{OE}$/VPP	A0	A9	OUTPUTS
Read	VIL	VIL	X	X	DOUT
Output Disable	VIL	VIH	X	X	High Z
Standby (TTL)	VIH	X	X	X	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	High Z
Program	VIL	VPP	X	X	DIN
Program Verify	VIH	VIL	X	X	DOUT
Program Inhibit	VIH	VPP	X	X	High Z
Manufacturer Code	VIL	VIL	VIL	VH	C2H
Device Code	VIL	VIL	VIH	VH	80H

NOTES:
1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL(For auto select)
3. A1 - A8 = A10 - A19 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

Figure1. INTERACTIVE PROGRAMMING FLOW CHART
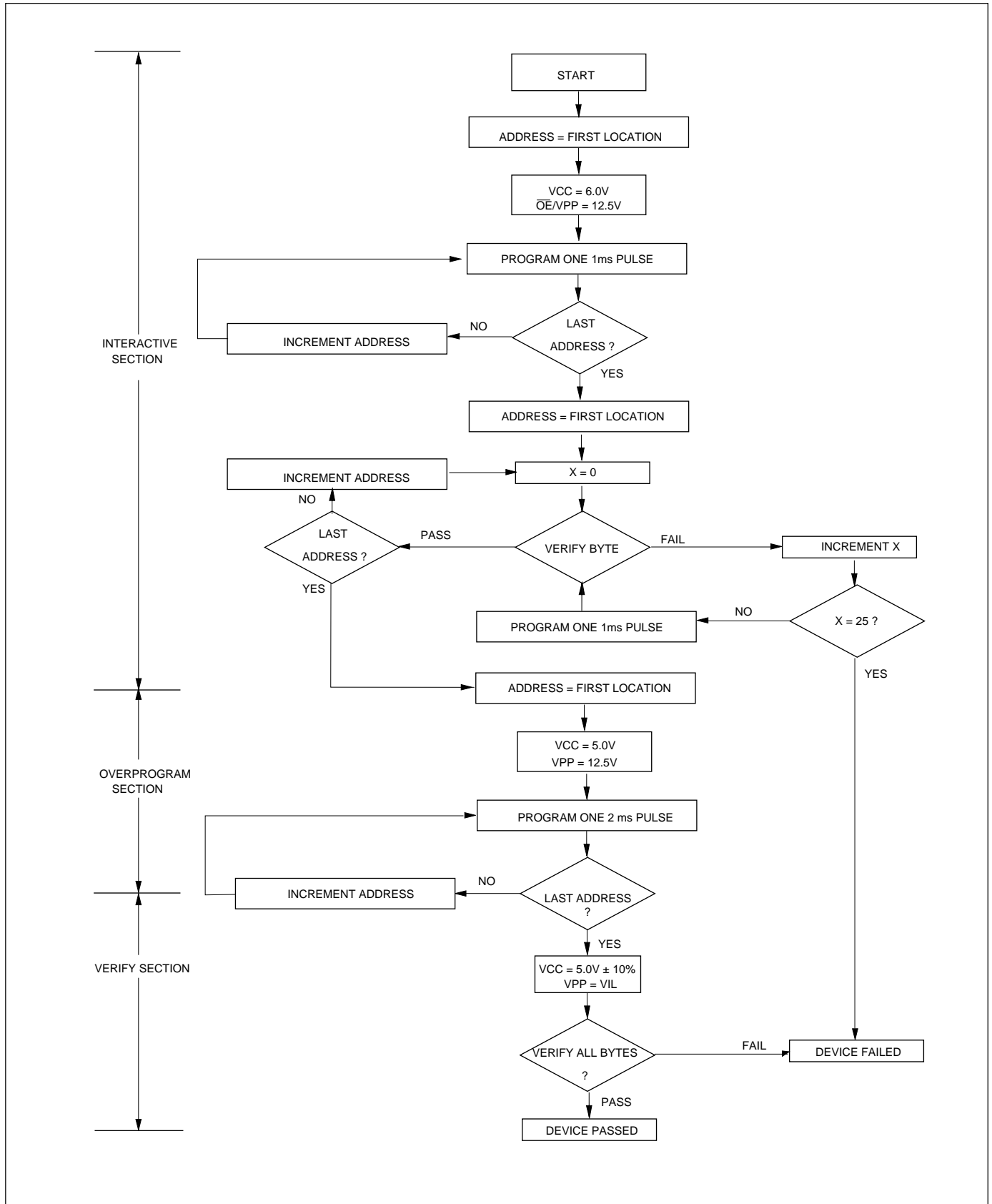
Fligure 2. FAST PROGRAMMING FLOW CHART
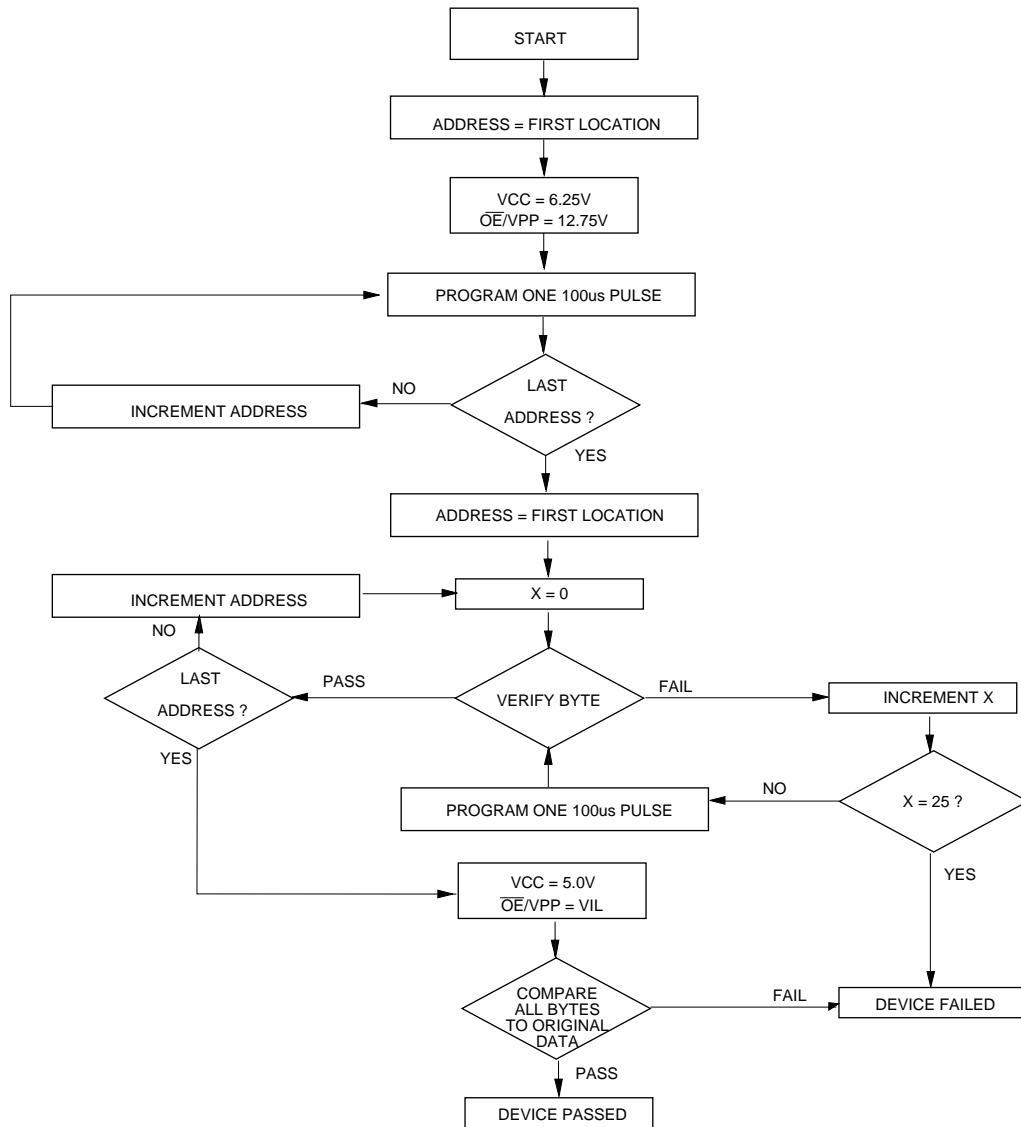
SWITCHING TEST CIRCUITS

```
DEVICE
UNDER
TEST

CL

6.2K Ω

1.8K Ω      +5V

DIODES = IN3064
OR EQUIVALENT
```

CL = 100 pF Including jig capacitance
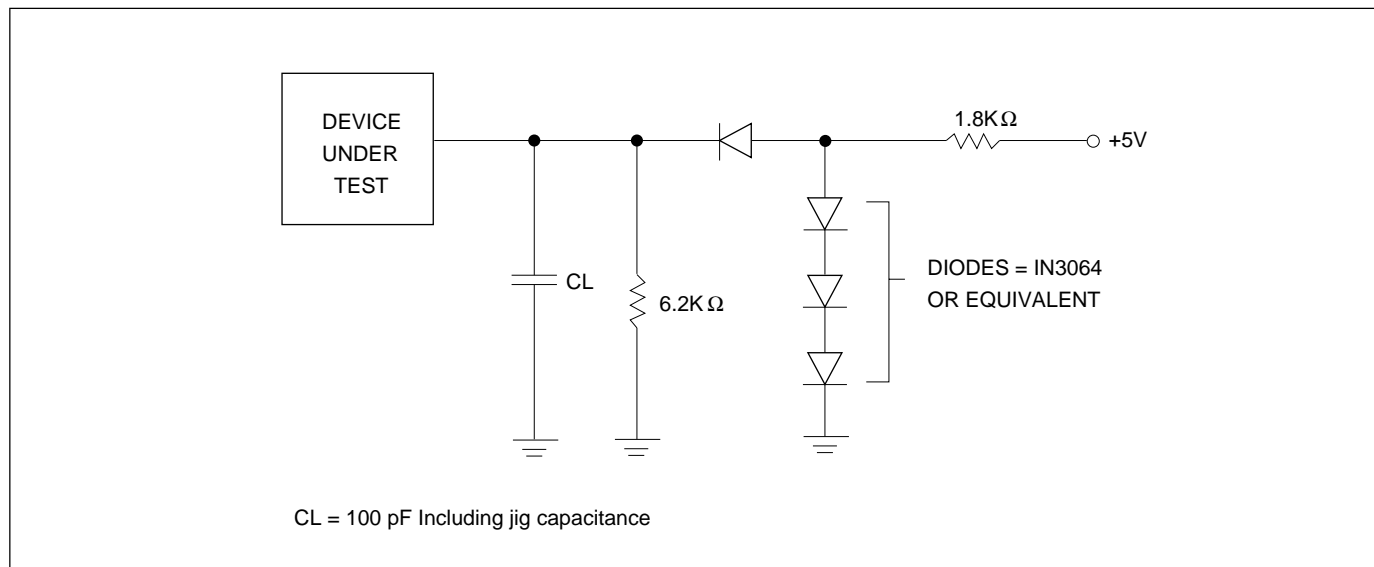
SWITCHING TEST WAVEFORMS

```
3.0V                2.0V              2.0V
                                             TEST POINTS
                    0.8V              0.8V
0V
        INPUT                                OUTPUT
```

AC TESTING: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".

Input pulse rise and fall times are ≤ 10ns.
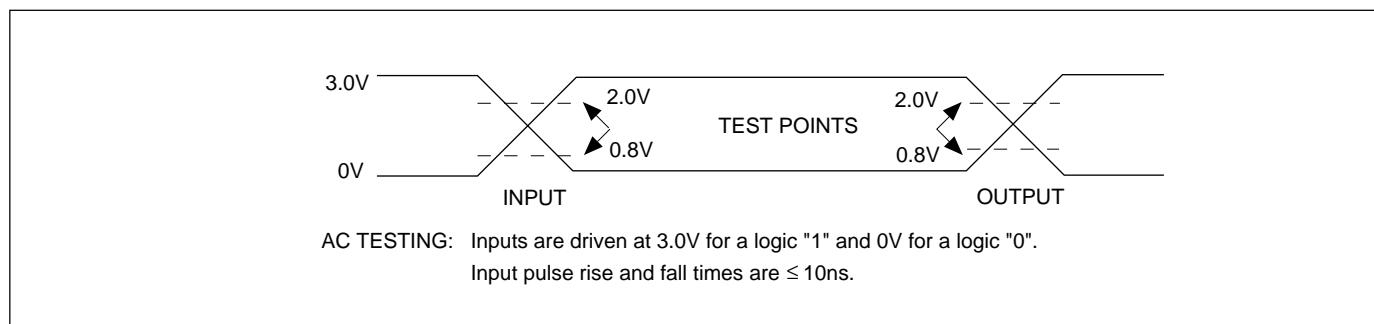
ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
V9 & VPP	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS   TA = -40°C to 85°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	3.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	µA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	µA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		60	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	µA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS   TA = -40°C to 85°C, VCC = 5V± 10%

SYMBOL	PARAMETER	27C8000-12 MIN.	27C8000-12 MAX.	27C8000-15 MIN.	27C8000-15 MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		120		150	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		50		65	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or CE High to Output Float	0	35	0	50	ns	
tOH	Output Hold from Address, CE or OE which ever occurred first	0		0		ns	

DC PROGRAMMING CHARACTERISTICS   TA = 25°C ± 5°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL
VCC1	Interactive Supply Voltage	5.75	6.25	V	
VPP1	Interactive Programming Voltage	12.0	13.0	V	
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS   TA = 25°C ± 5°C

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time		2.0		µS	
tOES	$\overline{OE}$ Setup Time		2.0		µS	
tDS	Data Setup Time		2.0		µS	
tAH	Address Hold Time		0		µS	
tDH	Data Hold Time		2.0		µS	
tDFP	$\overline{CE}$ to Output Float Delay		0	130	nS	
tVPS	VPP Setup Time		2.0		µS	
tPW	$\overline{CE}$ Program Pulse Width	Fast	95	105	µS	
		Interactive	0.95	1.05	mS	
tOPW	$\overline{CE}$ Overprogram Pulse(Interactive)		1.95	2.05	mS	
tVCS	VCC Setup Time		2.0		µS	
tDV	Data Valid from $\overline{CE}$			250	nS	
tOEH	$\overline{OE}$/VPP Hold Time		2.0		µS	
tVR	OE/VPP Recovery Time		2.0		µS	

WAVEFORMS
READ CYCLE
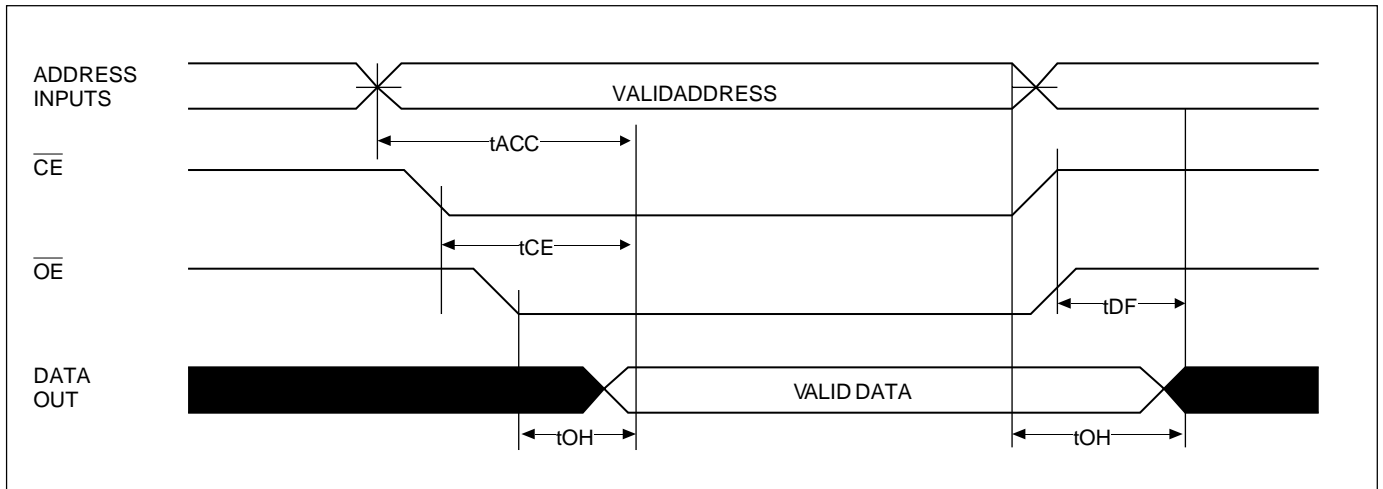
INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS

NOTES:
1. The input timing reference level is 0.8V for VIL and 2V for VIH.
2. tOE and tDFP are characteristics of the device, but must be accomodated by the programmer.
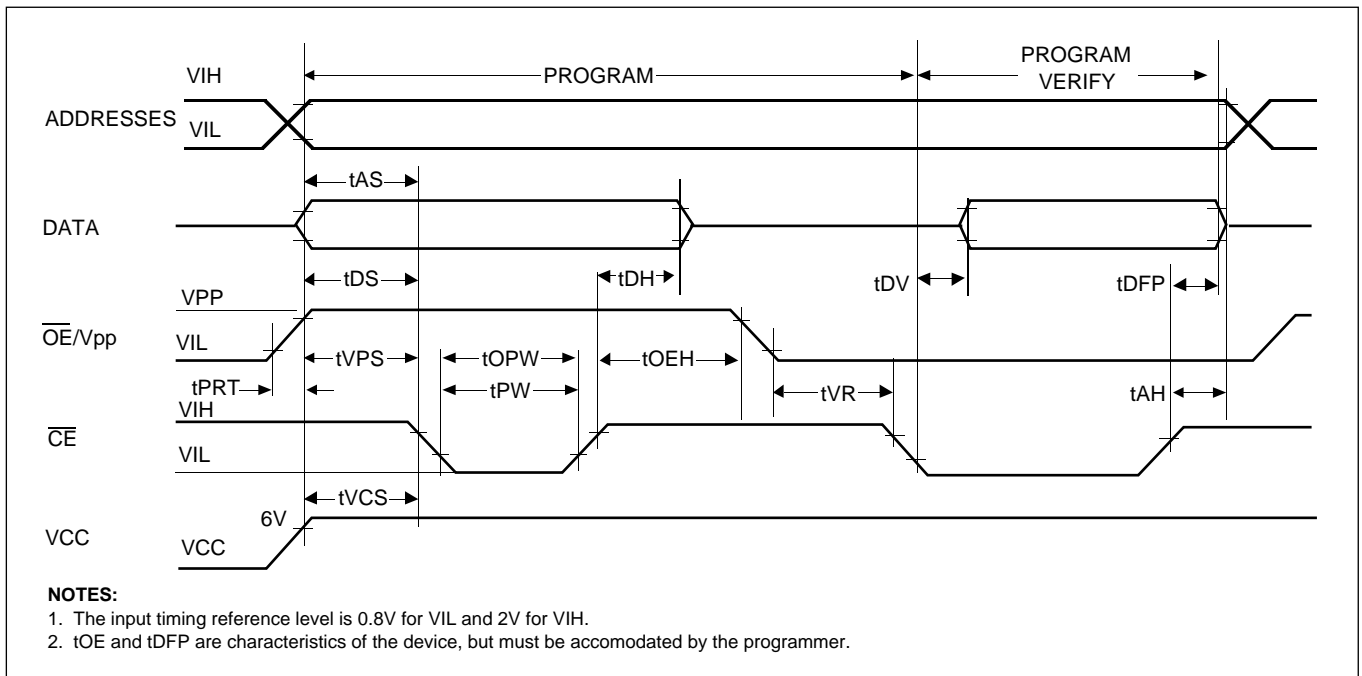
ORDERING INFORMATION
CERAMIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX27C8000DI-12	120	60	100	32 Pin DIP
MX27C8000DI-15	150	60	100	32 Pin DIP

PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX27C8000PI-12	120	60	100	32 Pin DIP
MX27C8000QI-12	120	60	100	32 Pin PLCC
MX27C8000MI-12	120	60	100	32 Pin SOP
MX27C8000PI-15	150	60	100	32 Pin DIP
MX27C8000QI-15	150	60	100	32 Pin PLCC
MX27C8000MI-15	150	60	100	32 Pin SOP

PACKAGE INFORMATION

32-PIN CERDIP(MSI) WITH WINDOW (600mil)

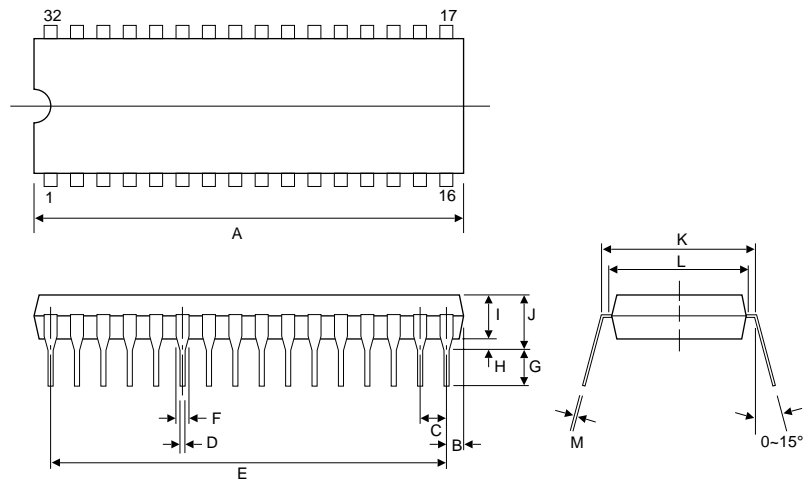| ITEM	MILLIMETERS	INCHES
A	42.26 max	1.665 max
B	1.90 ± .38	.075 ± .015
C	2.54 [TP]	.100 [TP]
D	.46 [REF]	.018 [REF]
E	38.07	1.500
F	1.42 [REF]	.056 [REF]
G	3.43 ± .38	.135 ± .015
H	.96 ± .43	.038 ± .017
I	4.06	.160
J	5.00	.203
K	15.58 ± .13	.614 ± .005
L	13.20 ± .38	.520 ± .015
M	.25 [REF]	.010 [REF]
N	ø8.12	ø.320

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.
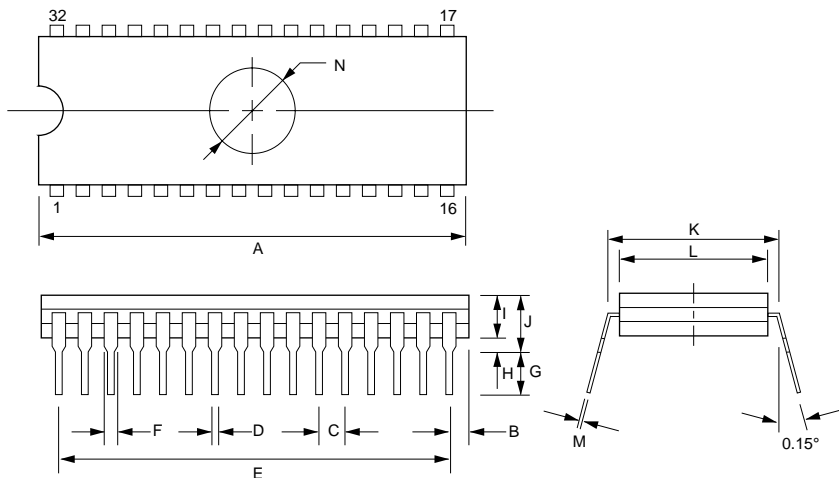
32-PIN PLASTIC DIP(600 mil)

ITEM	MILLIMETERS	INCHES
A	42.13 max.	1.660 max.
B	1.90 [REF]	.075 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	38.07	1.500
F	1.27 [Typ.]	.050 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.97 ± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.

PACKAGE INFORMATION

32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	12.44 ± .13	.490 ± .005
B	11.50 ± .13	.453 ± .005
C	14.04 ± .13	.553 ± .005
D	14.98 ± .13	.590 ± .005
E	1.93	.076
F	3.30 ± .25	.130 ± .010
G	2.03 ± .13	.080 ± .005
H	.51 ± .13	.020 ± .005
I	1.27 [Typ.]	.050 [Typ.]
J	.71 [REF]	.028 [REF]
K	.46 [REF]	.018 [REF]
L	10.40/12.94 (W) (L)	.410/.510 (W) (L)
M	.89 R	.035 R
N	.25 (TYP.)	.010 (TYP.)

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.
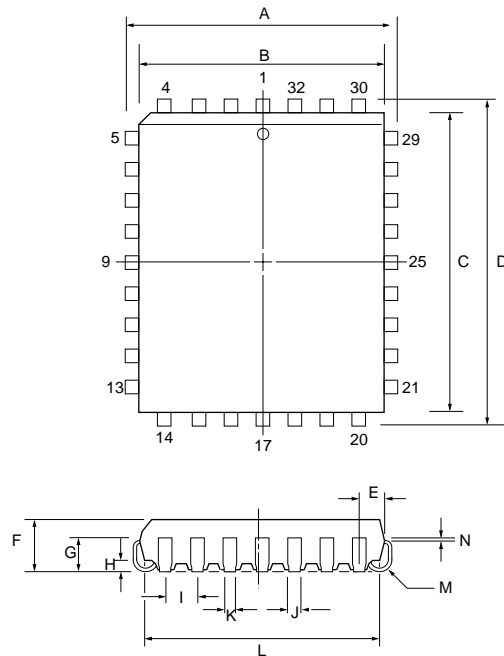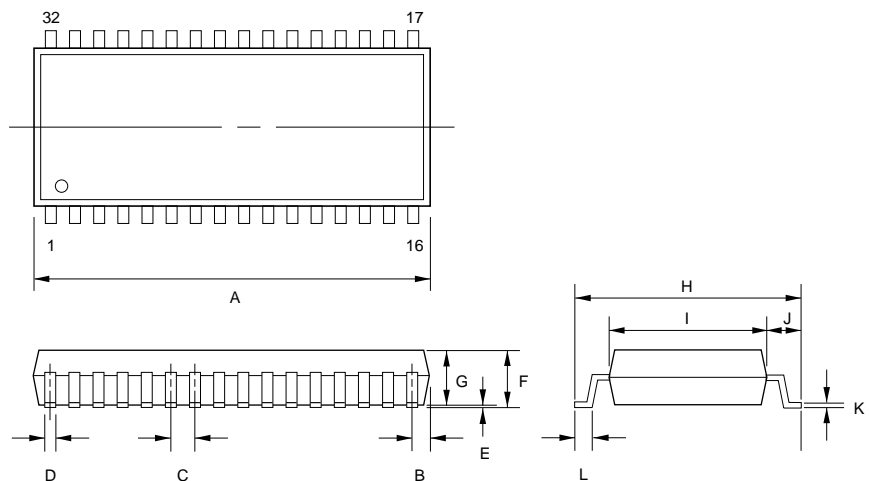

32-PIN PLASTIC SOP(450 mil)

ITEM	MILLIMETERS	INCHES
A	20.95 max.	.825 max.
B	1.00 [REF]	.039 [REF]
C	1.27 [TP]	.050 [TP]
D	.40 [Typ.]	.016 [Typ.]
E	.05 min.	.002 min.
F	3.05 max.	.120 max.
G	2.69 ± .13	.106 ± .005
H	14.12 ± .25	.556 ± .010
I	11.30 ± .13	.445 ± .005
J	1.42	.056
K	.20 [Typ.]	.008 [Typ.]
L	.79	.031

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.

MACRONIX INTERNATIONAL CO., LTD

HEADQUARTERS :
TEL : +886-3-578-8888
FAX : +886-3-578-8887

EUROPE OFFICE :
TEL : +32-2-456-8020
FAX : +32-2-456-8021

JAPAN OFFICE :
TEL : +81-44-246-9100
FAX : +81-44-246-9105

SINGAPORE OFFICE :
TEL : +65-747-2309
FAX : +65-748-4090

TAIPEI OFFICE :
TEL : +886-2-2509-3300
FAX : +886-2-2509-2200

MACRONIX AMERICA INC.
TEL : +1-408-453-8088
FAX : +1-408-453-8488

CHICAGO OFFICE :
TEL : +1-847-963-1900
FAX : +1-847-963-1909

http : //www.macronix.com