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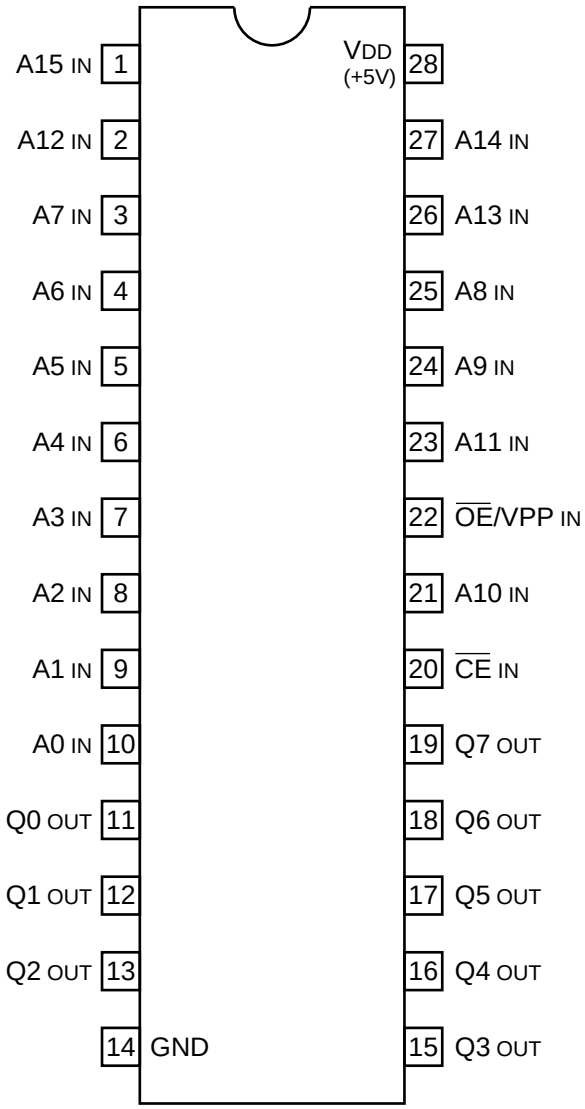
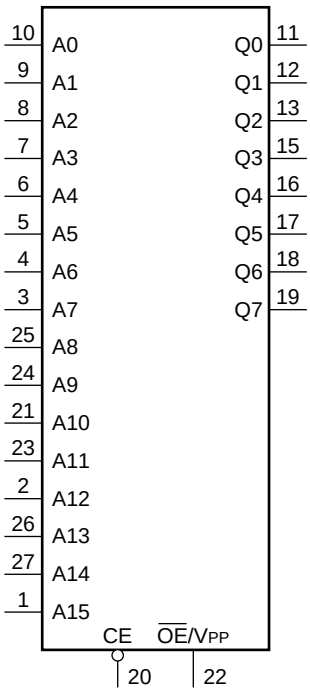
C-MOS 512K (65, 536·8) -BIT GATE PROCESS ERASABLE PROM
— TOP VIEW —





A0 - A15 ; ADDRESS INPUTS
$\overline{CE}$; CHIP ENABLE INPUT
$\overline{OE}$; OUTPUT ENABLE INPUT
Q0 - Q7 ; DATA INPUTS/OUTPUTS
VPP ; PROGRAM POWER SUPPLY