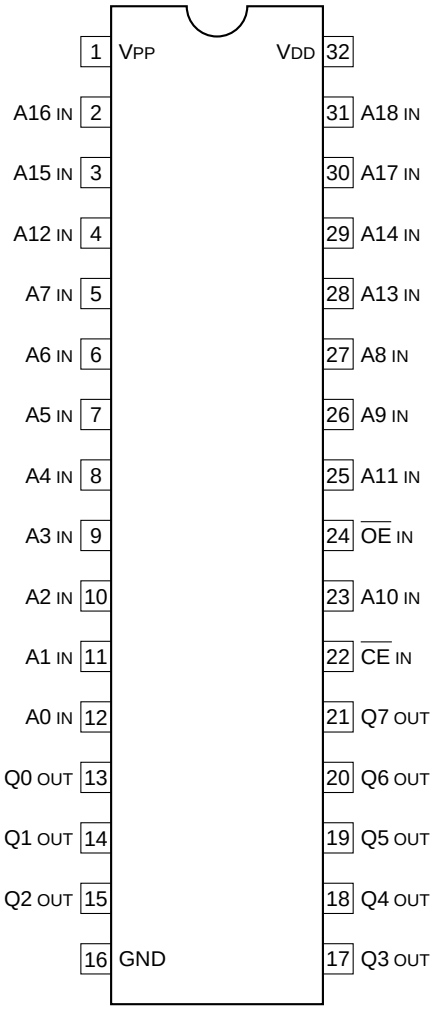
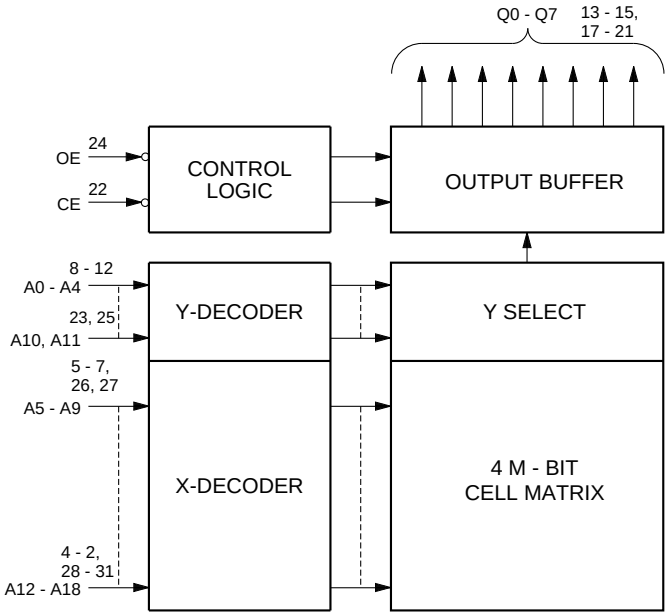
C-MOS 4 M (512 K × 8)-BIT ERASABLE PROM

—TOP VIEW—





INPUT

A0 - A18 ; ADDRESS
$\overline{CE}$; CHIP ENABLE
$\overline{OE}$; OUTPUT ENABLE

OUTPUT

Q0-Q7 ; DATA

OTHER

VPP ; PROGRAM POWER SUPPLY

MODE \ TERMINAL	$\overline{CE}$	$\overline{OE}$	A0	A9	VPP	OUTPUT
READ	0	0	×	×	+5 V	D OUT
OUTPUT DISABLE	0	1	×	×	+5 V	HI-Z
STANDBY (TTL)	1	×	×	×	+5 V	HI-Z
STANDBY (CMOS)	VDD±0.3 V	×	×	×	+5 V	HI-Z
PROGRAM	0	1	×	×	+12.5 V	D IN
PROGRAM VERIFY	1	0	×	×	+12.5 V	D OUT
PROGRAM INHIBIT	1	×	×	×	+12.5 V	HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
× ; DON'T CARE
HI-Z ; HIGH IMPEDANCE