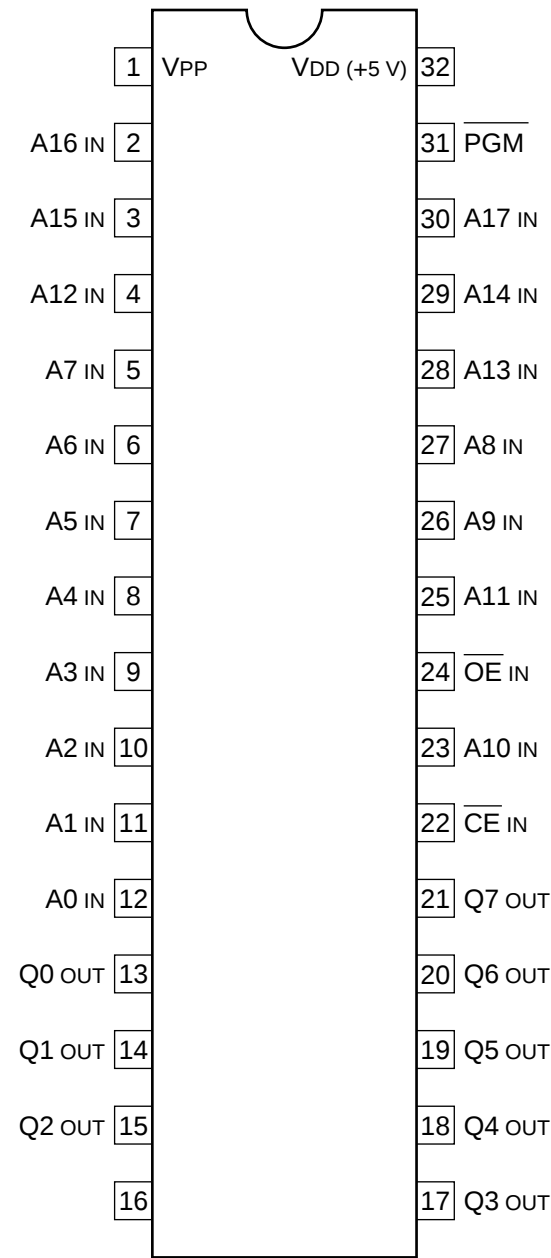
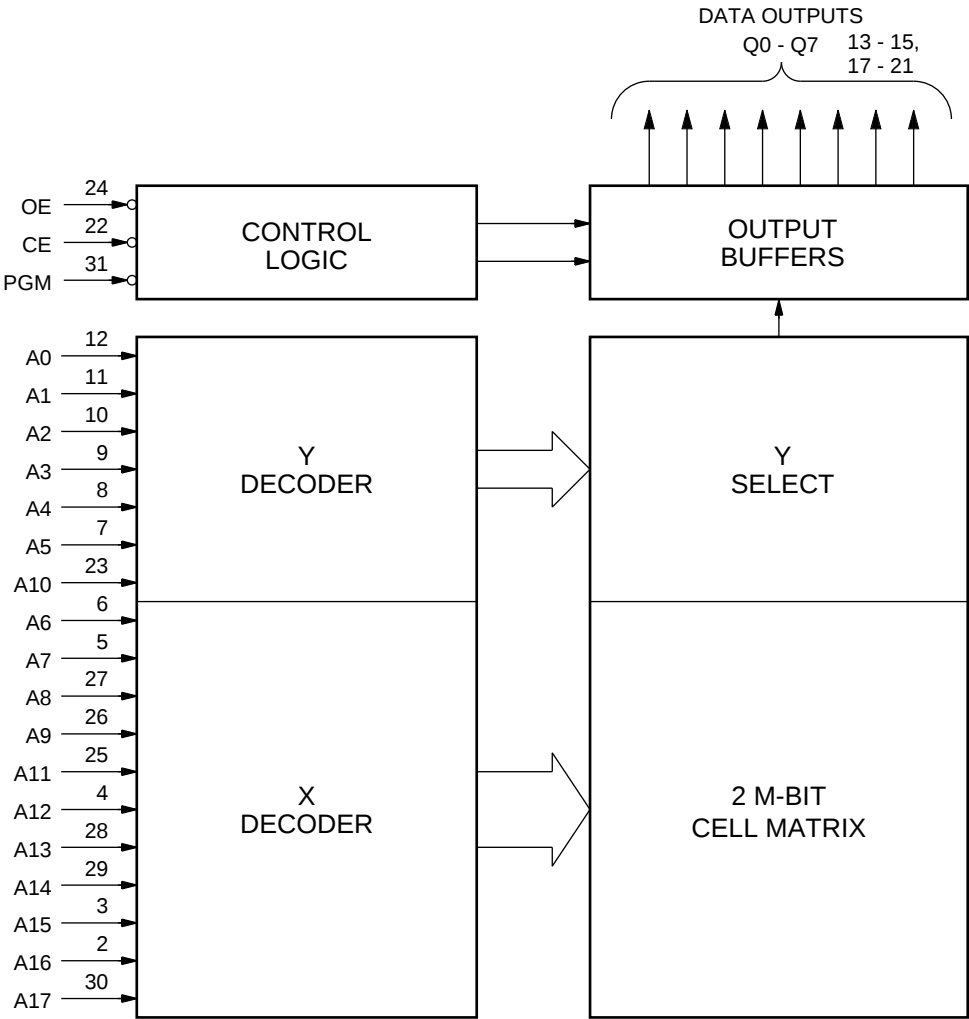

C-MOS 2 M (256 K × 8)-BIT ERASABLE PROM
—TOP VIEW—



- INPUT**
A0 - A17 ; ADDRESS
CE ; CHIP ENABLE
OE ; OUTPUT ENABLE
PGM ; PROGRAM ENABLE
- OUTPUT**
Q0 - Q7 ; DATA
- OTHER**
VPP ; PROGRAM POWER SUPPLY



TERMINAL MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	A0	A9	V _{PP}	OUTPUT
READ	0	0	x	x	x	+5 V	D OUT
OUTPUT DISABLE	0	1	x	x	x	+5 V	HI-Z
STANDBY (TTL)	1	x	x	x	x	+5 V	HI-Z
STANDBY (CMOS)	V _{DD} ±0.3 V	x	x	x	x	+5 V	HI-Z
PROGRAM	0	1	0	x	x	+12.5 V	D IN
PROGRAM VERIFY	0	0	1	x	x	+12.5 V	D OUT
PROGRAM INHIBIT	1	x	x	x	x	+12.5 V	HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
x ; DON'T CARE
HI-Z ; HIGH IMPEDANCE