PRELIMINARY

MX26C1024A

1M-BIT [64K x 16] CMOS MULTIPLE-TIME-PROGRAMMABLE ROM

FEATURES

- 64K words by 16-bit organization
- +5V operating power supply
- Electric erase instead of UV light erase
- +12V±5% program/erase voltage
- Fast access time: 70/90/100/120 ns
- Low power consumption
  - 40mA maximum active current
  - 100uA maximum standby current
- Command - driven program/erase mode
  - chip program 3 seconds typical
  - chip erase 3 seconds typical
- 100 minimum erase/program cycles
- Compatible with JEDEC-standard word-wide EPROM pinouts
- Package type:
  - 44-pin PLCC
  - 40-pin 10 x 14mm TSOP(I)
  - 40-pin PDIP

PATENTED TECHNOLOGY

GENERAL DESCRIPTION

The MX26C1024A is a 1M-bit MTP ROM™ (Multiple-Time Programmable Read Only Memory) organized as 64K words of 16 bits each. MXIC's MTP ROMs offer the most cost-effective and reliable read/write non-volatile random access memory. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard MX26C1024A offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX26C1024A has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

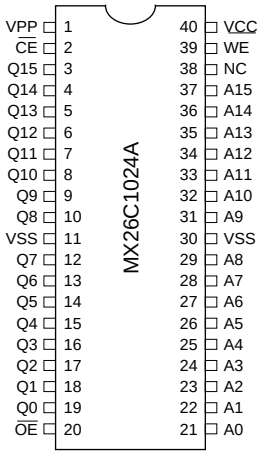
MXIC's MTP ROMs augment EPROM functionality with in-circuit electrical erasure and programming. The MX26C1024A uses a command register to manage this functionality, while maintaining entirely compatible to EPROM/OTP pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC MTP ROM™ technology reliably stores memory contents after 100 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX26C1024A uses a 12.0V ± 5% VPP supply to perform the Program/Erase algorithms.

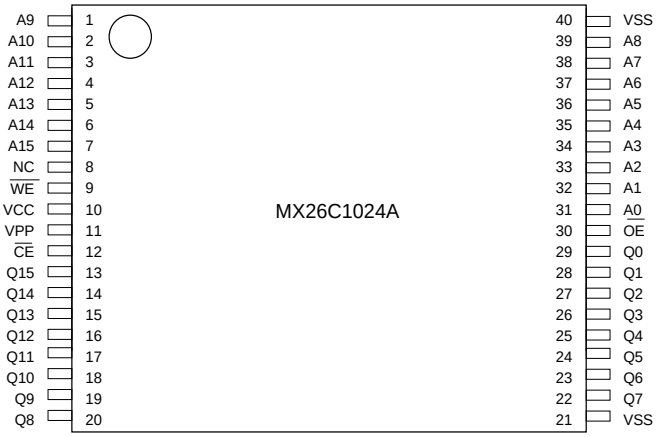
The MX26C1024A MTP ROM™ is available in industry standard 40 pin dual-in-line package, 44 lead PLCC, 40 TSOP (I) package.

PIN CONFIGURATIONS

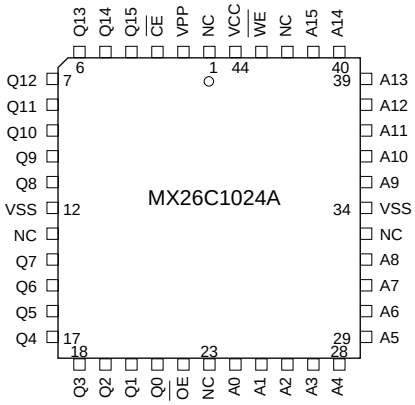
40 PDIP



40 TSOP(1)



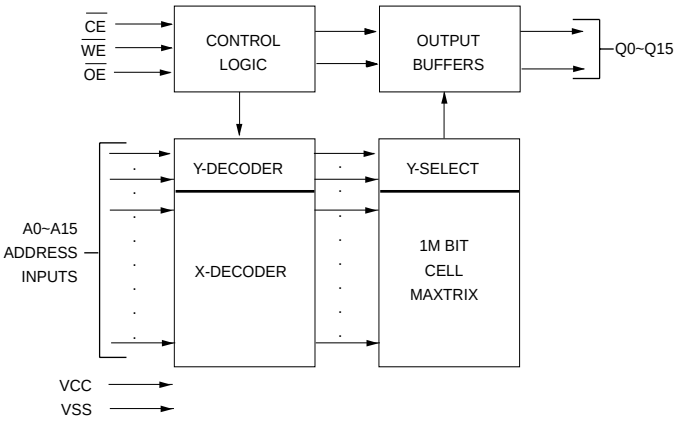
44 PLCC



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A15	Address Input
Q0~Q15	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Pin
VPP	Program Supply Voltage
VCC	Power Supply Pin (+5V)
VSS	Ground Pin
NC	No Internal Connection

BLOCK DIAGRAM



COMMAND DEFINITIONS

When low voltage is applied to the VPP pin, the contents of the command register default to 0000H, enabling read-only operation.

Placing high voltage on the VPP pin enables read/write/erase operations. Device operations are selected by writing specific data patterns into the command register. Table 1 defines these MX26C1024A register commands. Table 2 defines the bus operations of MX26C1024A.

TABLE 1. COMMAND DEFINITIONS

COMMAND	BUS	FIRST BUS CYCLE			SECOND BUS CYCLE		
	CYCLES	OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA
Read Memory	1	Write	X	XX00H			
Read Identified codes	2	Write	X	XX90H	Read	IA	ID
Setup Erase/ Erase	2	Write	X	XX20H	Write	X	XX20H
Setup program/ program	2	Write	X	XX40H	Write	PA	PD
Reset	2	Write	X	XXFFH	Write	X	XXFFH

Note:

IA = Identifier address

PA = Address of memory location to be programmed

ID = Data read from location IA during device identification(Manufacture code = 00C2H, Device code = 00E3H)

PD = Data to be programmed at location PA

X = X can be VIH or VIL

TABLE 2. MX26C1024 BUS OPERATIONS

OPERATION		VPP(1)	A0	A9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Q0-Q15
READ-ONLY	Read	VPPL	A0	A9	VIL	VIL	VIH	Data Out
	Output Disable	VPPL	X	X	VIL	VIH	VIH	Tri-State
	Standby	VPPL	X	X	VIH	X	X	Tri-State
READ/WRITE	Read	VPPH	A0	A9	VIL	VIL	VIH	Data Out(4)
	Standby(5)	VPPH	X	X	VIH	X	X	Tri-State
	Output Disable	VPPH	X	X	VIL	VIH	VIH	Tri-State
	Write	VPPH	A0	A9	VIL	VIH	VIL	Data In(6)

NOTES:

1. VPPL may be grounded, a no-connect with a resistor tied to ground, or ≤ VCC + 2.0V. VPPH is the programming voltage specified for the device. When VPP = VPPL, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1. All other addresses are low.
3. Read operations with VPP = VPPH may access array data or Silicon ID codes.
4. With VPP at high voltage, the standby current equals ICC + IPP (standby).
5. Refer to Table 1 for valid Data-In during a write operation.
6. X can be VIL or VIH.

READ COMMAND

While VPP is high, for erasure and programming, memory contents can also be accessed via the read command. The read operation is initiated by writing XX00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon VPP power-up is 0000H. This default value ensures that no spurious alteration of memory contents occurs during the VPP power transition. Where the VPP supply is hard-wired to the MX26C1024A, the device powers up and remains enabled for reads until the command register contents are changed.

SILICON-ID-READ COMMAND

MTP-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system.

The MX26C1024A contains a Silicon-ID-Read operation to supplement traditional PROM-programming methodology. The operation is initiated by writing XX90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 00C2H. A read cycle from address 0001H returns the device code of 00E3H.

A Reset command should be issued in order to terminate the Silicon-ID-Read operation.

SET-UP CHIP ERASE/ERASE COMMANDS

Set-up Chip Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing XX20H to the command register.

To commence chip erasure, the erase command (XX20H) must again be written to the register. After the second write of erase command, an internal latch will be triggered to maintain the erase mode. The microprocessor must count the erase time. After valid erase time (tEW) is reach, the microprocessor must toggle the $\overline{CE}$ and $\overline{WE}$ again to abort the internal latch, thus exit the erase mode.

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the VPP pin. In the absence of this high voltage, memory contents are protected against erasure.

ERASE-VERIFY

After each erase operation, all words must be verified. Verification should be performed on the erased bits to detemine that they were correctly erased. The verification should be perfomed with $\overline{OE}$ and $\overline{CE}$ at VIL, and VPP at its erase voltage.

The MX26C1024A applies an internally generated margin voltage to the addressed word. Reading FFFFH from the addressed word indicates that all bits in the word are erased.

The process continues for each word in the array until a word does not return FFFFH data, or the last address is accessed.

SET-UP PROGRAM/PROGRAM COMMANDS

Set-up program is a command-only operation that stages the device for byte programming. Writing XX40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ pulse. Data is internally latched on the rising edge of the $\overline{WE}$ pulse. After the second $\overline{WE}$ pulse, an internal latch will be triggered to maintain the programming mode. The microprocessor must count the programming time. After valid programming time(tPW) is reach, the microprocessor must toggle the $\overline{CE}$ a nd $\overline{WE}$ again to abort the internal latch, thus exit the programming mode.

PROGRAM-VERIFY

The MX26C1024A is programmed on a word-by-word basis. Word programming may occur sequentially or at random. Following each programming operation, the word just programmed must be verified.

Verification should be performed on the programed bits to detemine that they were correctly programed. The verification should be perfomed with $\overline{OE}$ and $\overline{CE}$ at VIL, and VPP at its programming voltage. The program-verify stages the device for verification of the byte last programmed. No new address information is latched.

The 26C1024A applies an internally-generated margin voltage to the word. A microprocessor read cycle outputs the data. A successful comparison between the programmed word and true data means that the word is successfully programmed. To gurranttee better margin for change-retention, one more pulse for programming is necessary. Programming then proceeds to the next desired word location. The programming timing waveform, illustrates how commands are combined with bus operations to perform word programming.

RESET COMMAND

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of XXFFH will safely abort the operation. Memory contents will not be altered. Should program-fail or erase-fail happen, two consecutive writes of XXFFH will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

POWER-UP SEQUENCE

The MX26C1024A powers up in the read only mode. In addition, the memory contents may only be altered after successful completion of a two-step command sequence. At least, one of $\overline{CE}$, $\overline{OE}$ or address pins should be toggled in order to sucessfully complete the first data read during power-up.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND, and between VPP and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on MTP memory arrays, a 4.7uF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
VPP	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

CAPACITANCE TA = 25°C, f = 1.0 MHz(Sampled only)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		8	8	pF	VIN = 0V
COUT	Output Capacitance		8	12	pF	VOUT = 0V
CVPP	VPP Capacitance		25	50	pF	VPP= 0V

READ OPERATION

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%, VPP = GND to VCC

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current	-10		10	uA	VIN = GND to VCC
ILO	Output Leakage Current	-10		10	uA	VOUT = GND to VCC
IPP1	VPP Current		1	100	uA	VPP = 5.5V
ISB1	VCC Standby current			1	mA	$\overline{CE}$ = VIH
ISB2	VCC Power-Down Current		1	100	uA	$\overline{CE}$ = VCC + 0.3V
ICC1	VCC Active Current			40	mA	IOUT = 0mA, f=5MHz
VIL	Input Low Voltage	-0.3(NOTE 1)		0.8	V	
VIH	Input High Voltage	2.4		VCC + 0.3	V	(NOTE 2)
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH	Output High Voltage	2.4			V	IOH = -400mA

NOTES:

1. VIL min. = -1.0V for pulse width £ 50 ns.
   VIL min. = -2.0V for pulse width £ 20 ns.
2. VIH max. = VCC + 1.5V for pulse width £ 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS TA = 0ºC to 70ºC, VCC = 5V ± 10%, VPP = GND to VCC

		26C1024A-70		26C1024A-90		26C1024A-10		26C1024A-12			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		70		90		100		120	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		70		90		100		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		35		45		50		60	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note1)	0	20	0	25	0	30	0	35	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

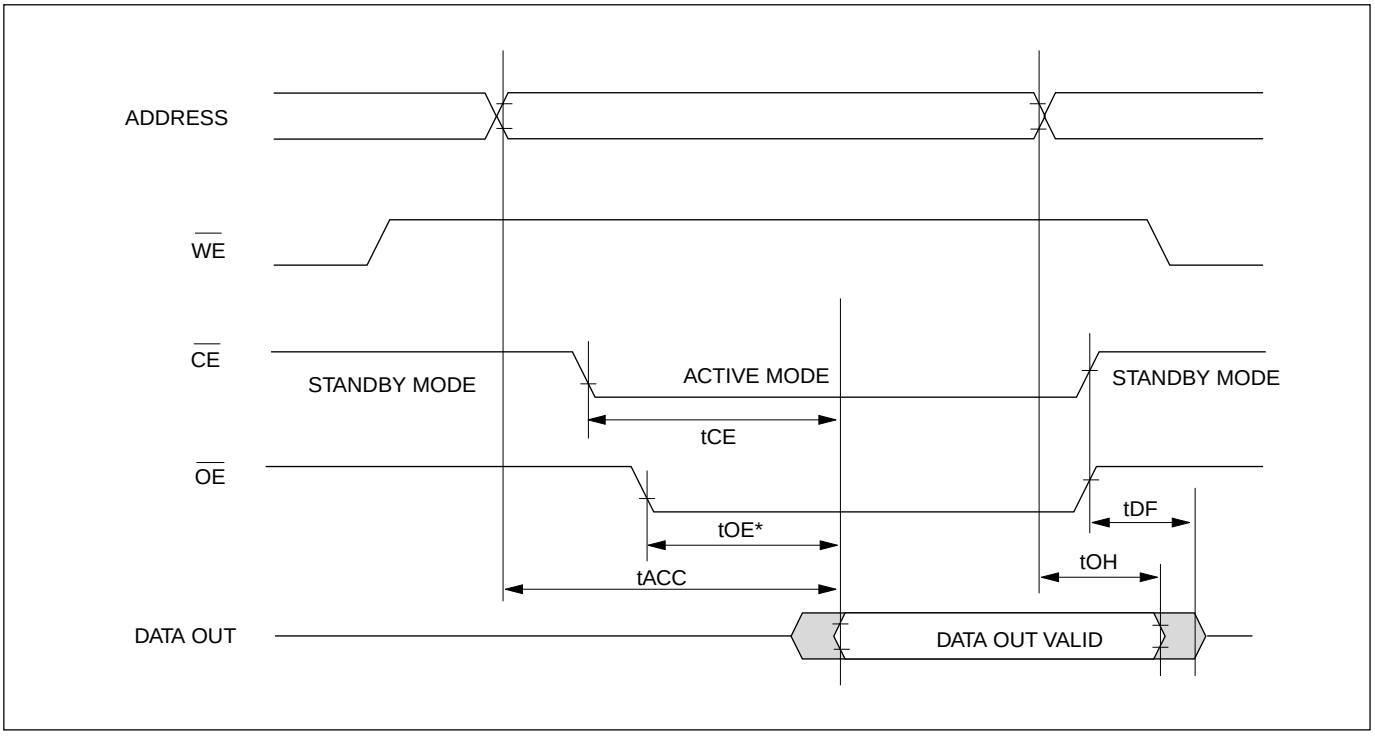
TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times: ≤10ns
- Output load: 1 TTL gate + 100pF (Including scope and jig)
- Reference levels for measuring timing: 0.8V, 2.0V

NOTE:

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

READ TIMING WAVEFORMS



* If $\overline{CE}$ is kept low and address pins are kept at constant during power-up, the time period between $\overline{OE}$ going low and data out valid shoud be treated as tACC instead of tOE.

COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%, VPP = 12.0V ± 5%

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current	-10		10	mA	VIN=GND to VCC
ILO	Output Leakage Current	-10		10	mA	VOUT=GND to VCC
ISB1	VCC Standby current			1	mA	$\overline{CE}$=VIH
ISB2			1	100	mA	$\overline{CE}$=VCC ± 0.5V
ICC1 (Read)	VCC Operating Current			30	mA	IOUT=0mA, f=1MHz
ICC2 (Program)				50	mA	In Programming
ICC3 (Erase)				50	mA	In Erase
ICC4 (Program Verify)				50	mA	In Program Verify
ICC5 (Erase Verify)				50	mA	In Erase Verify
IPP1 (Read)	VPP Current			100	mA	VPP=12.6V
IPP2 (Program)				50	mA	In Programming
IPP3 (Erase)				50	mA	In Erase
IPP4 (Program Verify)				50	mA	In Program Verify
IPP5 (Erase Verify)				50	mA	In Erase Verify
VIL	Input Low Voltage	-0.3 (Note 5)		0.8	V	
VIH	Input High Voltage	2.0		VCC+0.5V	V	
VOL	Output LowVoltage			0.45	V	IOL=2.1mA
VOH	Output High Voltage	2.4			V	IOH=-400mA

NOTES:

1. VCC must be applied before VPP and removed after VPP.
2. VPP must not exceed 14V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while VPP=12V.
4. Do not alter VPP either VIL to 12V or 12V to VIL when $\overline{CE}$=VIL.
5. VIL min. = -0.6V for pulse width ≤ 20ns.
6. All currents are in RMS unless otherwise noted.(Sampled, not 100% tested.)

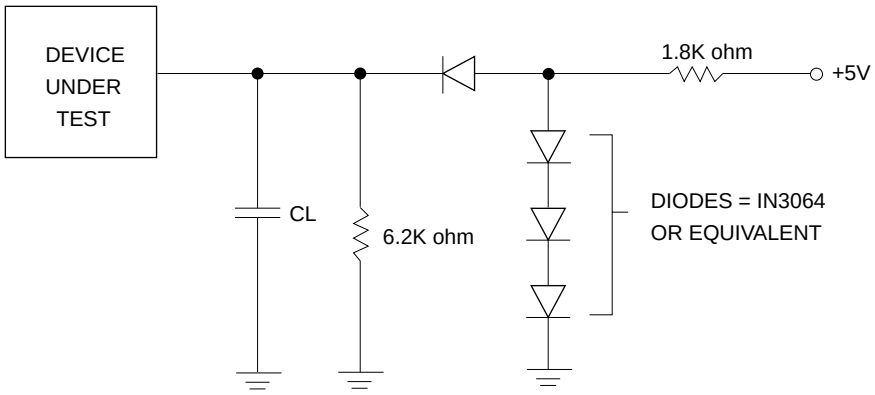
AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%, VPP =12V ± 5%

		26C1024A-70/90/100/120			
SYMBOL	**PARAMETER**	**MIN.**	**MAX.**	**UNIT**	**CONTIONS**
tVPS	VPP setup time	2.0		us	
tOES	$\overline{OE}$ setup time	2.0		us	
tCWC	Command programming cycle	90		ns	
tCEP	$\overline{WE}$ programming pulse width	45		ns	
tCEPH1	$\overline{WE}$ programming pluse width High	20		ns	
tAS	Address setup time	0		ns	
tAH	Address hold time	45		ns	
tDS	Data setup time	45		ns	
tDH	Data hold time	10		ns	
tCES	$\overline{CE}$ setup time	0		ns	
tVPH	VPP hold time	100		ns	
tDF	Output disable time (Note 3)		20	ns	
tEV	Erase verify access time		90	ns	
tPV	Program verify access time		90	ns	
tCH	$\overline{CE}$ Hold Time	0		ns	
tCS	$\overline{CE}$ setup to $\overline{WE}$ going low	0		ns	
tPW	Program Pulse Width	20	30	us	
tPR	Program Reovery Time	2		us	
tEW	Erase Pulse Width	0.95	1.05	s	
tER	Erase Recovery Time	0.5		s	
tEVSL	Erase Verify Setup Pulse Width Low	50		ns	
tEVSH	Erase Verify Setup Pulse Width High	2		us	
tPVS	Program Verify Setup Time	0		us	

NOTES:

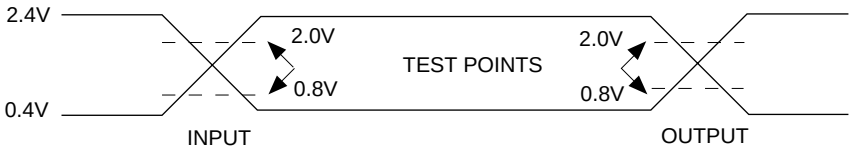
1. $\overline{CE}$ and $\overline{OE}$ must be fixed high during VPP transition from 5V to 12V or from 12V to 5V.
2. Refer to read operation when VPP=VCC about read operation while VPP 12V.
3. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.

SWITCHING TEST CIRCUITS



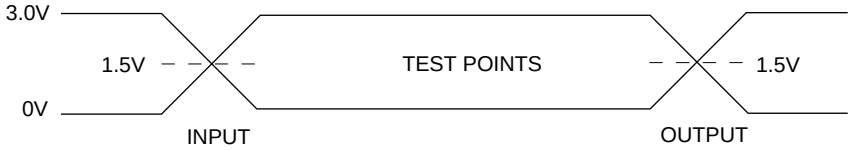
CL = 100 pF including jig capacitance(30pF for 70 ns parts)

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are <20ns.

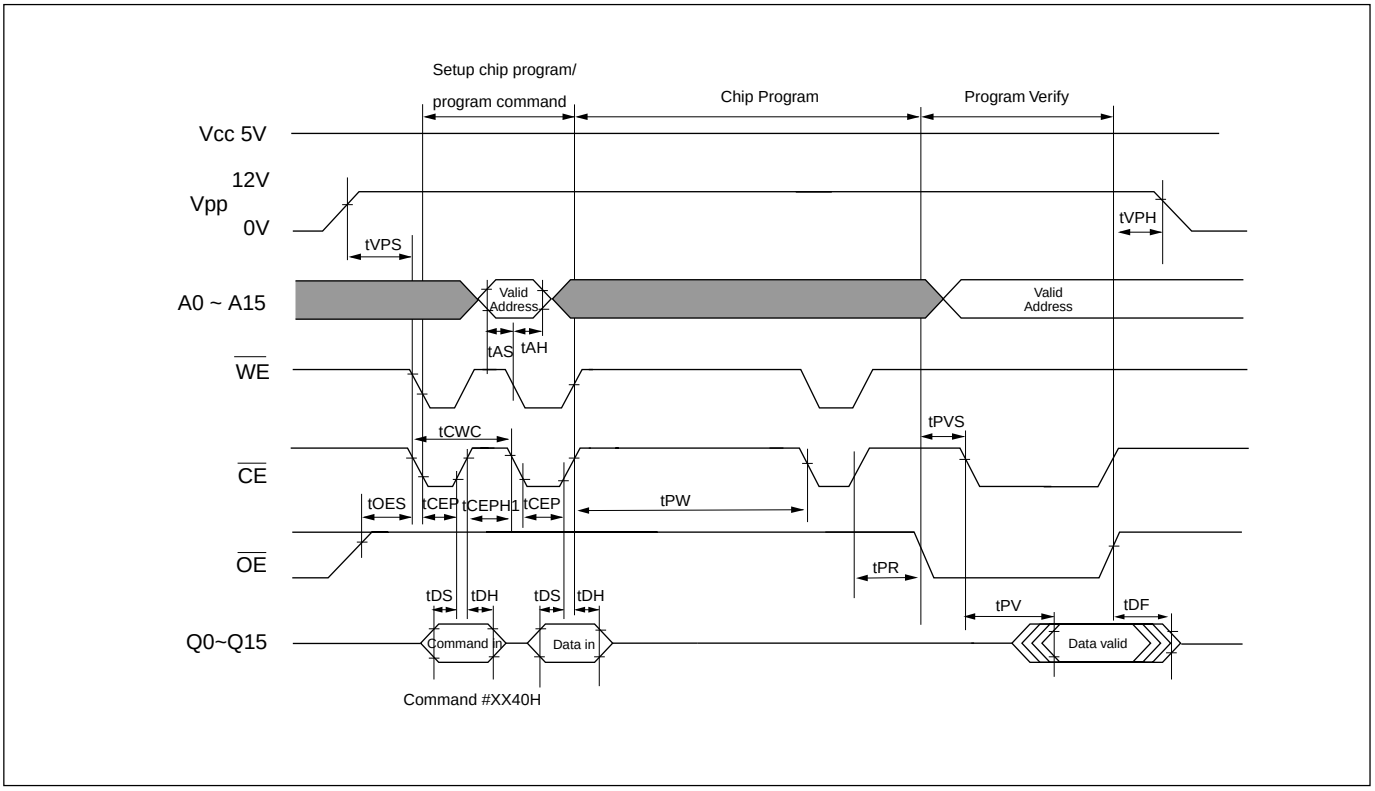
SWITCHING TEST WAVEFORMS



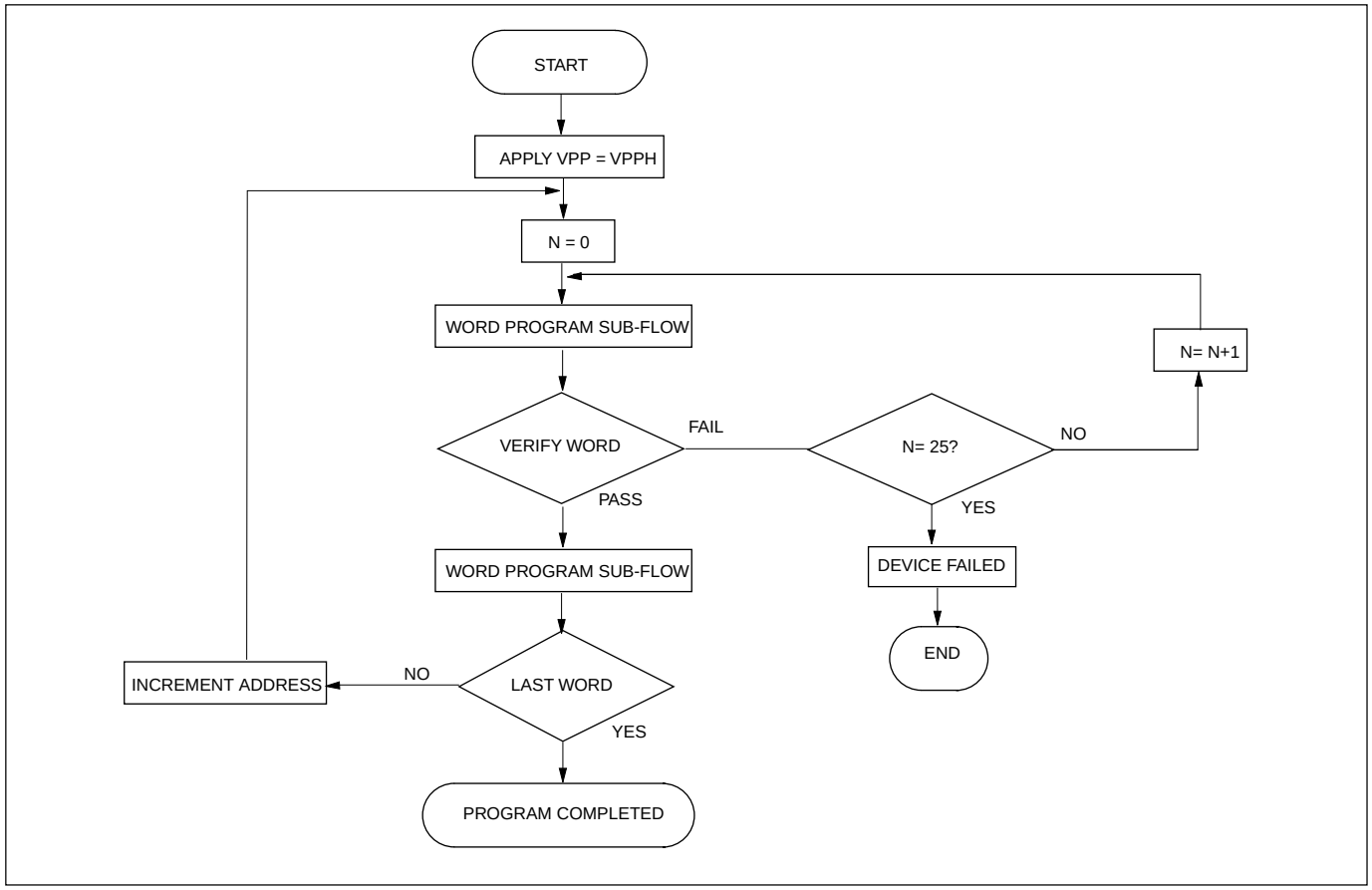
AC TESTING: (1) Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are ≤ 10ns.
(2) For MX26C1024A-70 only

PROGRAMMING TIMING WAVEFORM

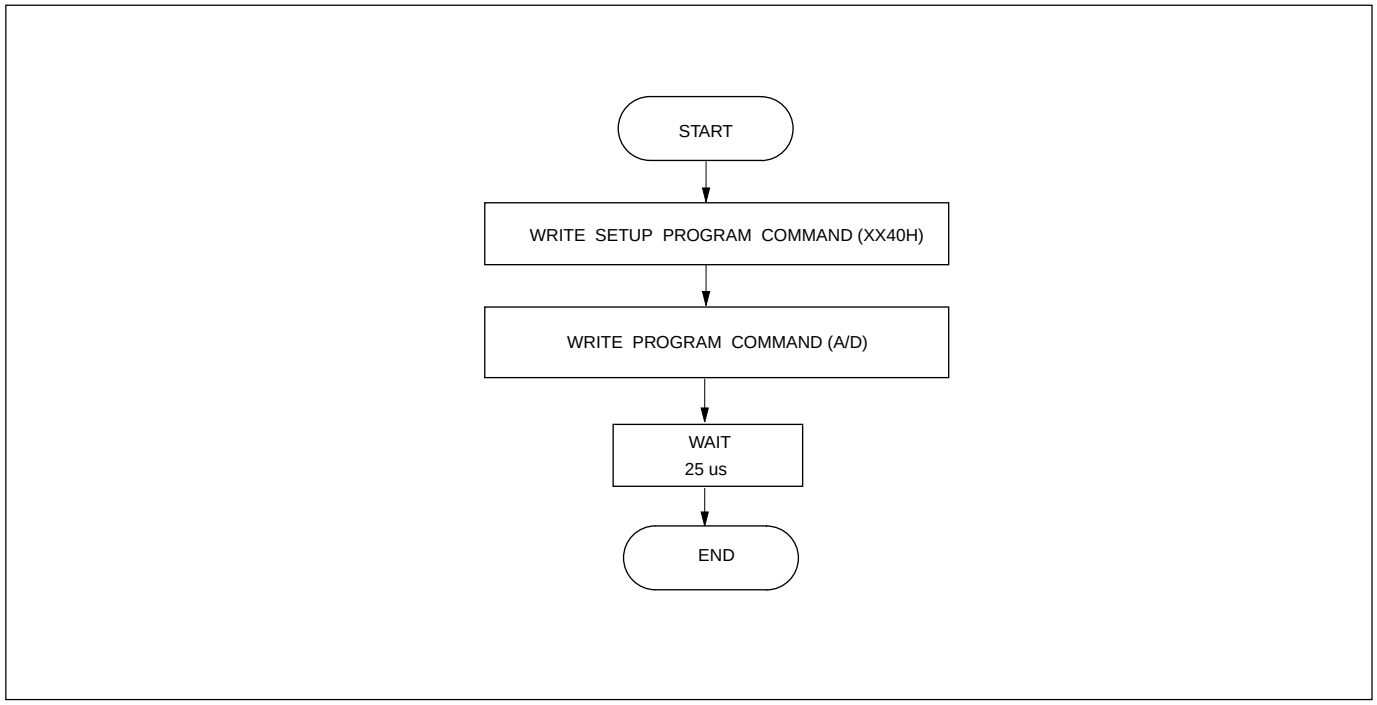
One word data is programmed. Control verification and additional programming externally according to programming flow chart.



PROGRAMMING FLOW CHART

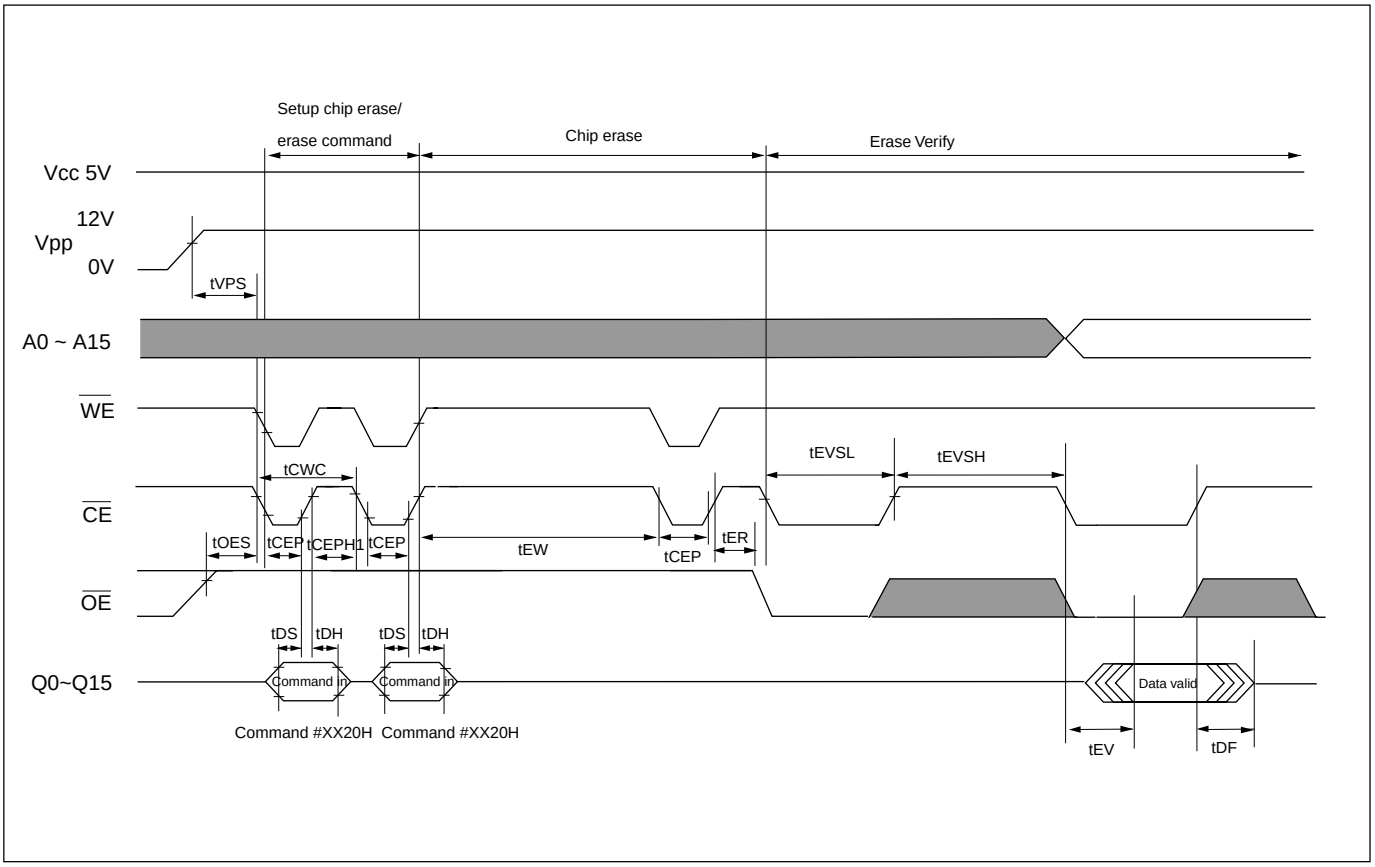


WORD PROGRAM SUB-FLOW

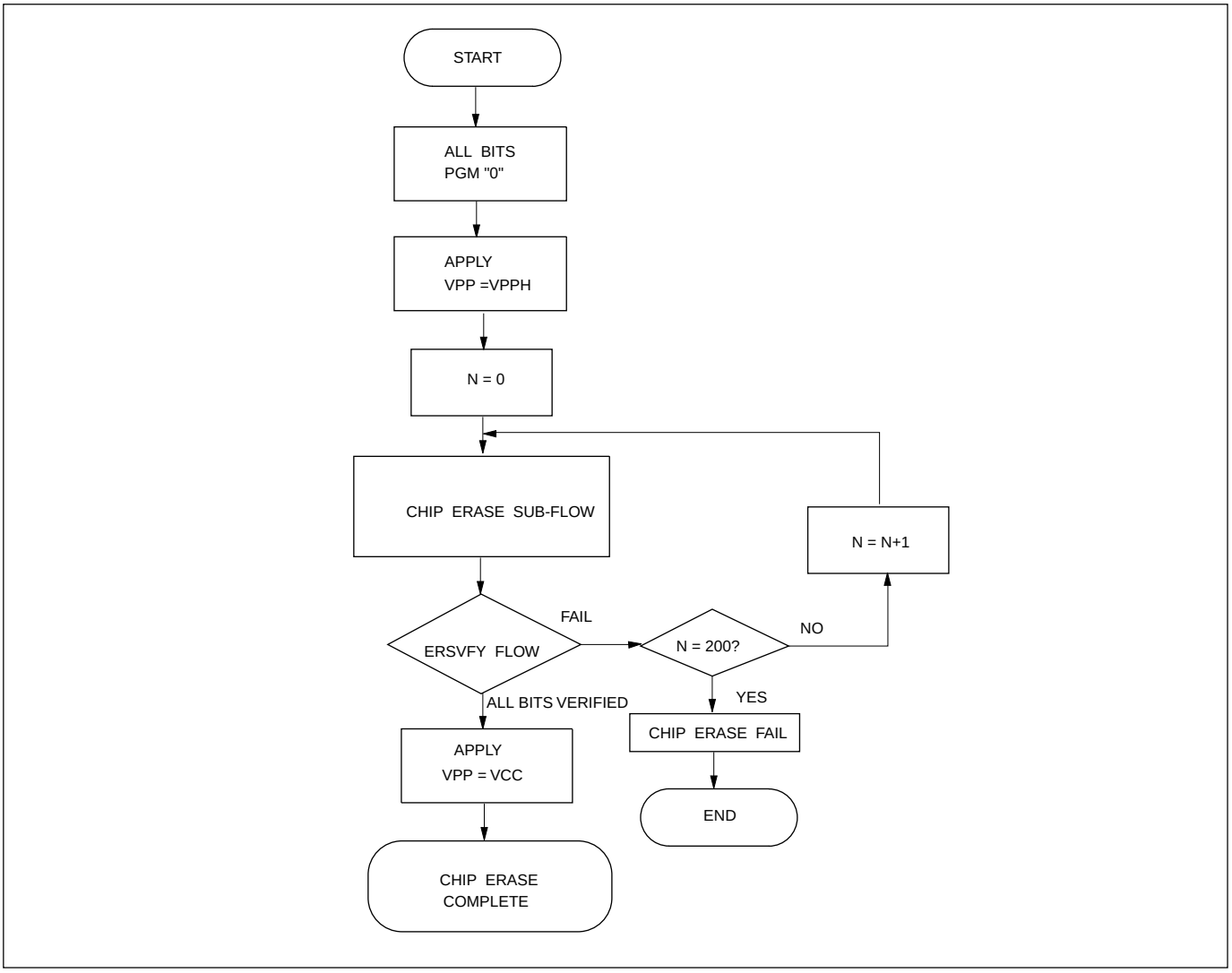


CHIP ERASE TIMING WAVEFORM

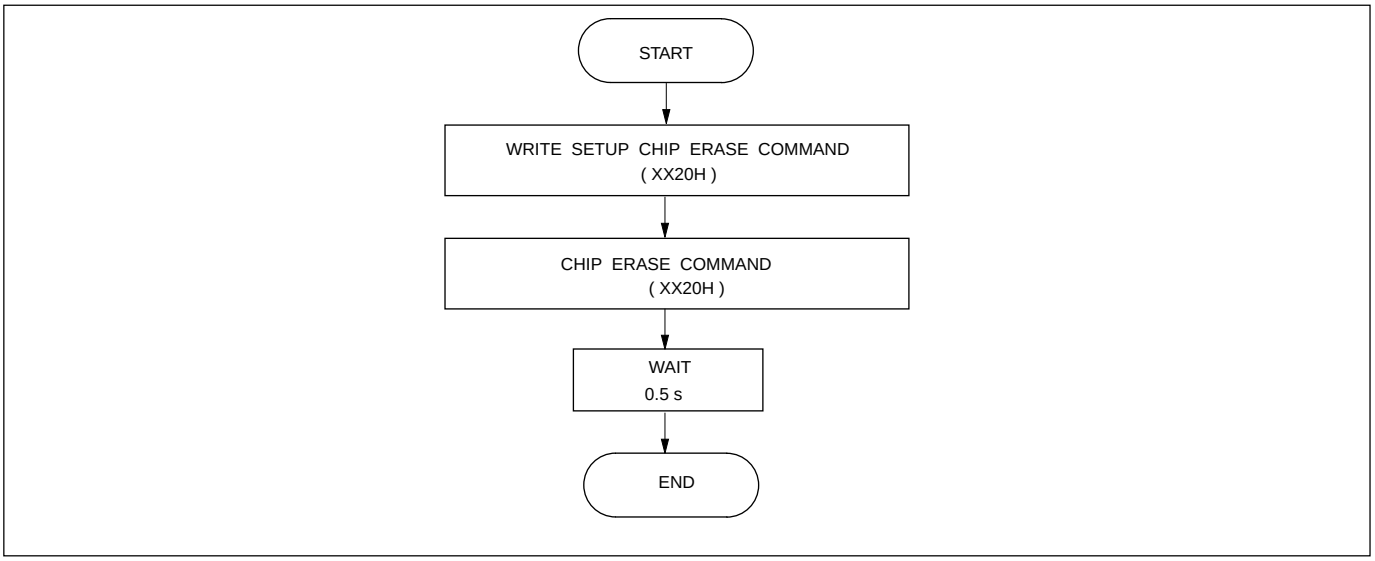
All data in chip are erased. Control verification and additional erasure externally according to chip erase flowchart.



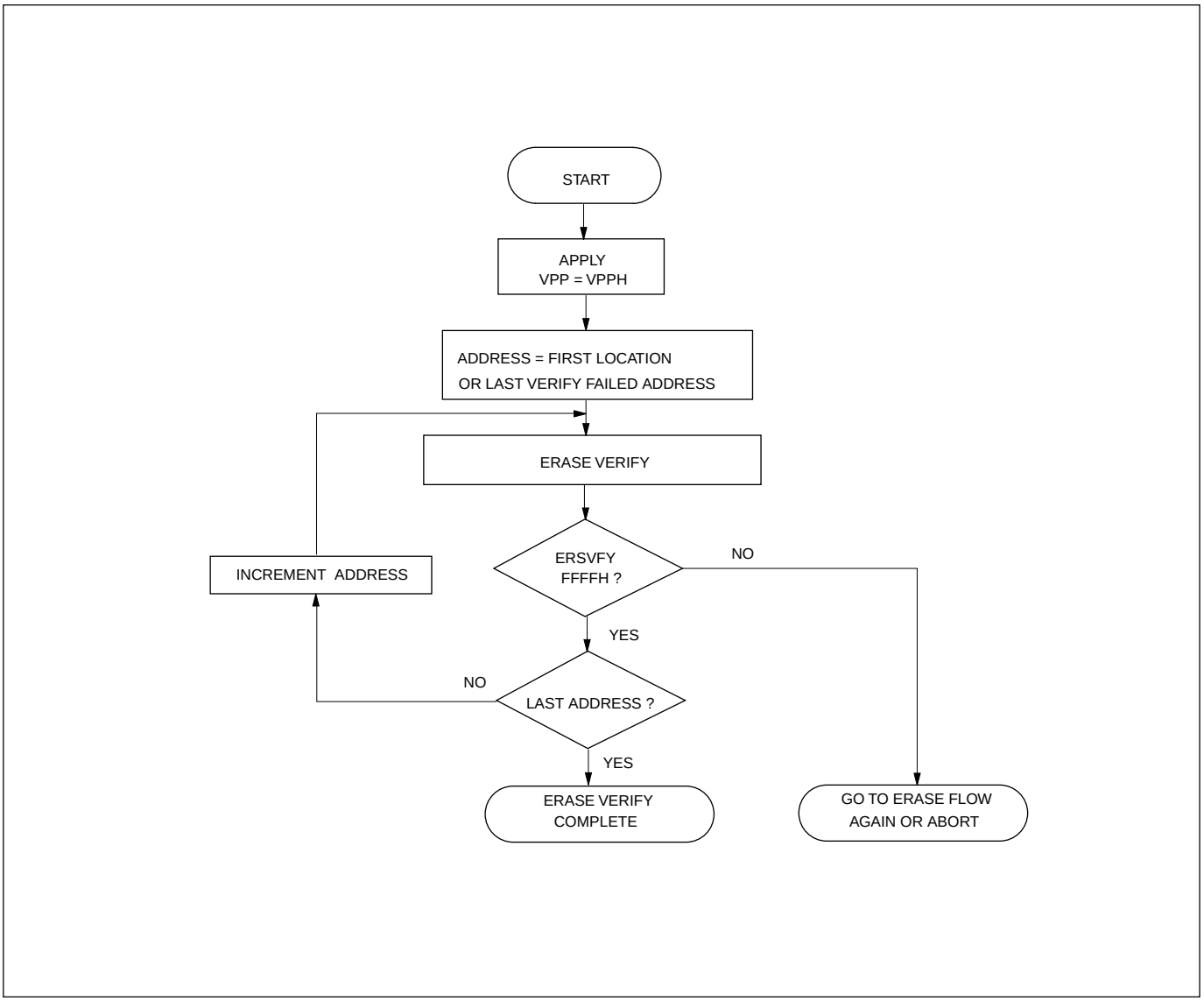
CHIP ERASE FLOWCHART



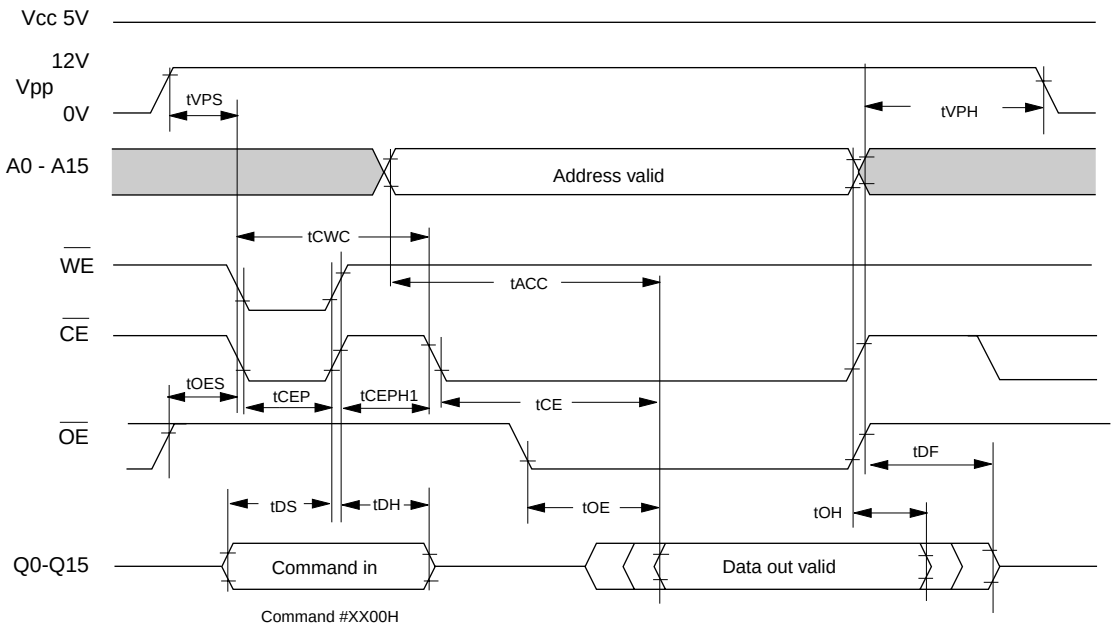
CHIP ERASE SUB-FLOW



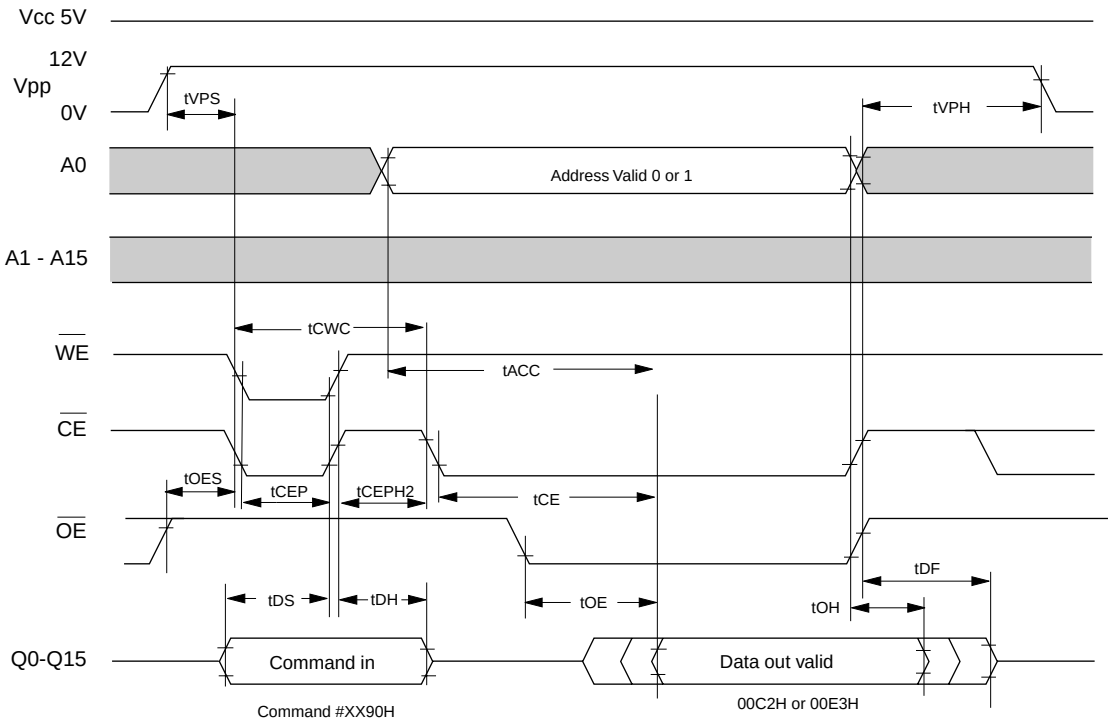
ERASE VERIFY FLOW



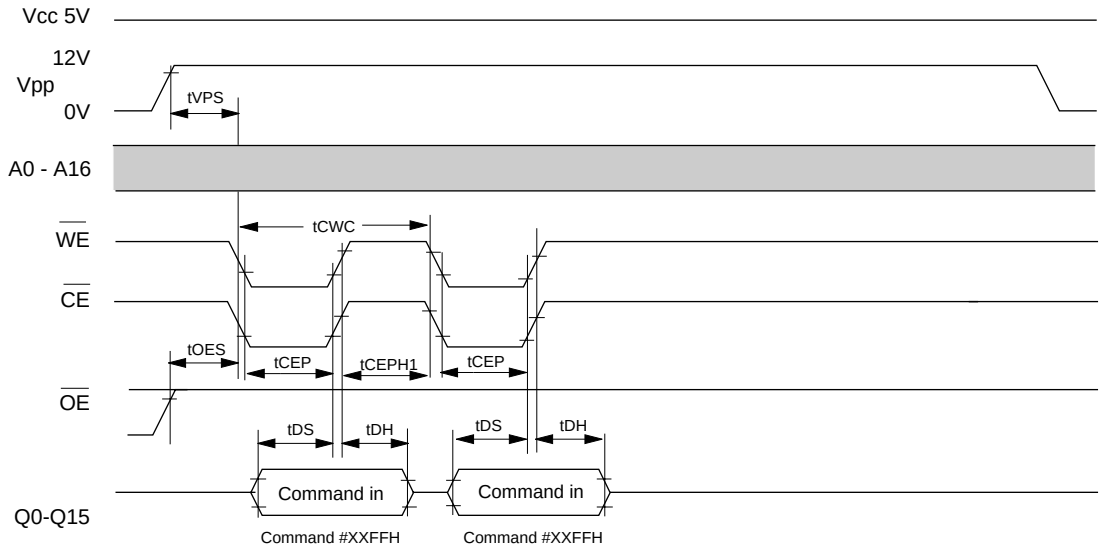
VPP HIGH READ TIMING WAVEFORM



VPP HIGH ID CODE READ TIMING WAVEFORM



RESET TIMING WAVEFORM



ORDERING INFORMATION PLASTIC PACKAGE

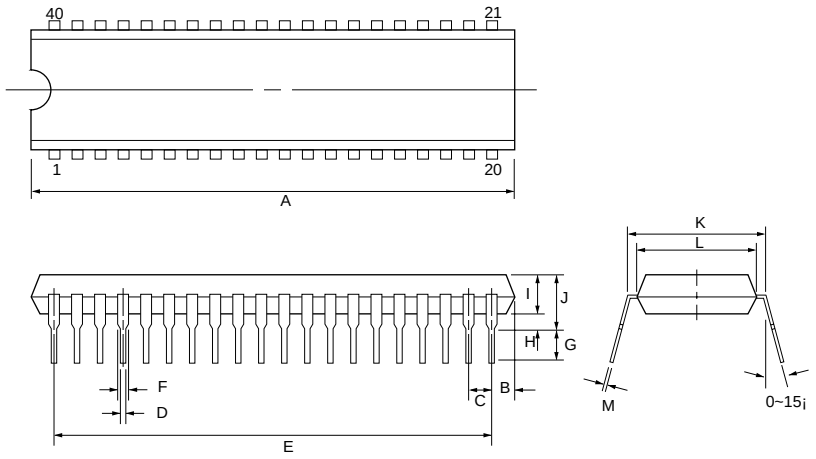
PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE	ERASE/PROGRAM CYCLE MIN.(time)
MX26C1024APC-70	70	40	100	40 Pin PDIP	100
MX26C1024AQC-70	70	40	100	44 lead PLCC	100
MX26C1024ATC-70	70	40	100	40 lead TSOP	100
MX26C1024APC-90	90	40	100	40 Pin PDIP	100
MX26C1024AQC-90	90	40	100	44 lead PLCC	100
MX26C1024ATC-90	90	40	100	40 lead TSOP	100
MX26C1024APC-10	100	40	100	40 Pin PDIP	100
MX26C1024AQC-10	100	40	100	44 lead PLCC	100
MX26C1024ATC-10	100	40	100	40 lead TSOP	100
MX26C1024APC-12	120	40	100	40 Pin PDIP	100
MX26C1024AQC-12	120	40	100	44 lead PLCC	100
MX26C1024ATC-12	120	40	100	40 lead TSOP	100

PACKAGE INFORMATION

40-PIN PLASTIC DIP

ITEM	MILLIMETERS	INCHES
A	52.54 max.	2.070 max.
B	0.76 [REF]	.030 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	50.76	2.000
F	1.27 [Typ.]	.050 [Typ.]
G	3.30 ± . 25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ±. 25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.97± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

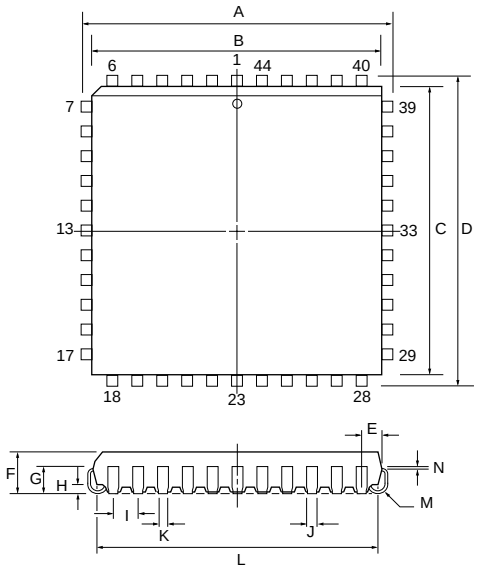
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	17.53 ± .12	.690 ± .005
B	16.59 ± .12	.653 ± .005
C	16.59 ± .12	.653 ± .005
D	17.53 ± .12	.690 ± .005
E	1.95	.077
F	4.70 max.	.185 max
G	2.55 ± .25	.100 ± .010
H	.51 min.	.020 min.
I	1.27 [Typ.]	.050 [Typ.]
J	.71 ± .10	.028 ± .004
K	.46 ± .10	.018 ± .004
L	15.50 ± .51	.610 ± .020
M	.63 R	.025 R
N	.25 [Typ.]	.010 [Typ.]

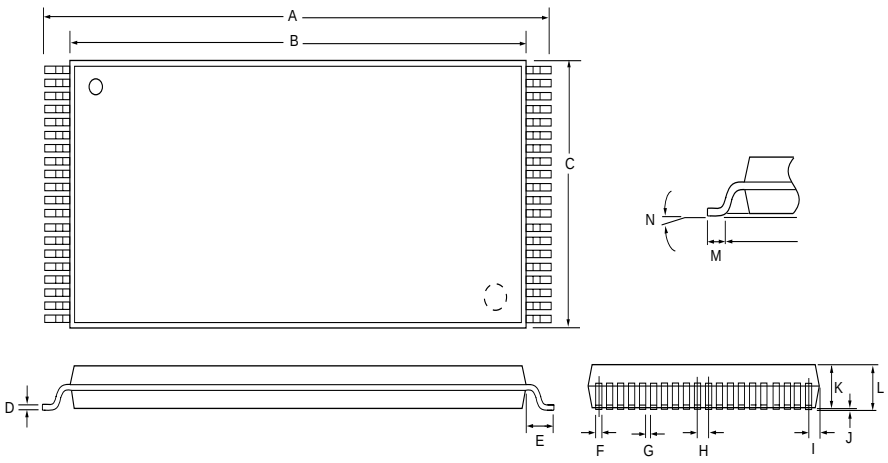
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



40-PIN PLASTIC TSOP

ITEM	MILLIMETERS	INCHES
A	14.0 ± .20	0.551 ± .008
B	12.4 ± .10	0.488 ± .004
C	10.1 max.	0.398 max.
D	0.125 [Typ.]	0.005 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20 ±.10	.008 ± .004
G	.30 ± .10	.012 ± .004
H	.50 [Typ.]	.020[Typ.]
I	.45 max.	0.18 max.
J	0 ~.20	0 ~ .008
K	1.00 ± .10	.039 ± .004
L	1.2 max.	0.047 max.
M	.50	.020
N	0 ~ 10°	0 ~ 10°

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



Revision History

Revision #	Description	Page	Date
1.2	Chip erase timing waveform: $\overline{OE}$ toggle during erase verify. Change Part Name: 26C1024 ---> 26C1024A. Delete SOP package.		11/05/1997
1.3	Modify $\overline{CE}$ and $\overline{OE}$ waveforms for chip erase timing waveform. Delete tEVS spec and add tEVSL and tEVSH spec for AC characteristics.	P13 P9	12/10/1997
1.4	Modify AC CHARACTERISTICS	P7	02/18/1998
1.5	1.modify the silicom-ID-Read command description 2.modify the power-Up SEQUENCE description 3.Add comment on READ TIMING WAVEFORMS 4.correct the AC characteristics of tER		06/11/1998
1.6	Modify $\overline{CE}$ and $\overline{OE}$ waveforms for Program Verify of programming timing waveform.	P11	10/27/1998
1.7	1.Correct active current to 40mA in page 6 and page 18 2.modify the power-up sequence description and CVPP value	P6,P18 P5,P6	12/07/1998

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