In-Circuit Programming of the MX26C1024A 1M-Bit (64Kx16) CMOS Multiple-Time-Programmable ROM

Application Note 09/16/97

This application note describes how to erase and program the MX26C1024A, **1M-bit MTP ROM™ (Multiple Time Programmable Read Only Memory** while installed **in-circuit in its application**. This is known as *in-circuit programming* (ICP) as opposed to *on-board programming* (OBP). The distinction between the two is *OBP* requires an external board programmer to erase and program the memory while *ICP* utilizes the on-board controller and hardware to perform the same functions.

In-Circuit Programming Considerations

Since this memory devices will be installed in applications where V_{CC} is typically set to 5-volts only, a brief discussion regarding programming margins will be discussed first.

When using a commercially available programmer for programming, V_{CC} is usually raised to 6.25-volts for both programming and verifying data. The programmed threshold voltage (Vt) of previously erased memory cells will be raised from a nominal 2.0-volts to 6.5-volts or greater thus providing a minimum of 1.5-volts of operating margin when V_{CC} is lowered to its normal operating voltage of 5.0-volts. If programming is done in-circuit using the standard algorithm with V_{CC} left at 5.0-volts, the programmed Vt might only be raised to 5.5-volts. A Vt of 5.5-volts does not provide sufficient cell margin for the memory device to work reliably after programming. The MX26C1024A is designed to provide an internally generated margin voltage to stress each cell during program verify and erase verify modes. This guarantees some additional cell Vt margin, but a modified programming algorithm is also recommended (see Figure 1 below) that provides one additional programming pulse (over-programming pulse) to boost the programmed cell Vt above the 6.5-volt range. This extra programming pulse will ensure that normal Vt margins will be achieved and reliable in-circuit operation can be expected. A similar extra pulse is used during the erase algorithm as shown in Figure 2 to ensure that erased cells have their threshold voltages reduced to the 1.0 to 2.0-volt range.

Hardware Considerations

If the user is planning to use the MX26C1024A to replace standard EPROMs or 5-volt only flash memory devices, there will be some hardware and design issues to consider. These issues will be covered next.

Standard EPROM and 5-volt only flash memory devices do not require 12-volts for operation, and this voltage may not even be available on some existing applications, but it is required to program and erase the MX26C1024A MTP™ ROM while in-circuit. This voltage is only required during the programming and erase algorithms and may be returned to 5.0-volts during normal read operations. If the user chooses not to switch VPP, it may be hardwired to 12-volts and the device will still operate correctly.

EPROMs do not use the WE/ pin while in-circuit so this pin is normally tied to V_{CC}. The MX26C1024A MTP™ ROM requires this pin to be active and controllable by the programming algorithms.

The following five PC board layout and design rules should be followed to provide optimum performance and ensure in-circuit program/erase reliability:

Design Rule 1: Position 0.1uF ceramic capacitors, one each for V_{CC} and V_{PP} and as close to these pins and GND as possible.

Design Rule 2: Position one 4.7uF electrolytic capacitor between V_{CC} and GND as well as V_{PP} and GND for each set of eight memory devices. This bulk capacitor will maintain even voltage to the memory array.

Design Rule 3: Use a single ground plane to eliminate potential ground current loops.

Design Rule 4: Use short and wide traces for V_{CC} and V_{PP} power paths (0.08" minimum width preferred).

Design Rule 5: Keep the traces for Data lines (D7-D0) as wide as possible (0.012" minimum width) to reduce their impedance. This will reduce the harmful switching spikes that occur when driving heavily loaded data buses.

Firmware Considerations

The use of hardware interval timers is preferred over software loops when providing timing for programming and erase pulse duration. Both timing methods will work, but software loops must be readjusted if a processor upgrade or system clock speed change is made.

If the programming algorithms reside in the memory device being programmed or erased, they must be moved to RAM before being executed. The reason is: once a programming or erase cycle begins, no other data or instructions may be fetched from that memory device until the cycle is complete.

Byte Programming

Refer to Figure 1 while following the 6 steps listed below:

Program Step 1.

The first step in the programming algorithm should be to read the manufacturer ID code and device type to make sure the proper devices have been installed in the application (see Table 1 for the command definitions).

Program Step 2.

Apply 12-volts to the memory V_{PP} pin (skip this step if V_{PP} is hardwired to 12-volts).

Program Step 3.

Issue the setup Program/Program' command sequence as shown in Table 1. This command requires two bus cycles. The first bus cycle sets up the program mode by writing the code 40h to the command register. The second bus cycle writes the program data to the desired address location. This address location is latched internally by the memory on the falling edge of WE/, the data is latched on the rising edge of WE/, and in internal latch is set to activate the programming pulse. The length of this programming pulse must be timed externally and terminated after tPW is reached. Termination is accomplished by writing any data to any address location in the device. This rite' is ignored by the device and only serves to reset the internal latch controlling the programming pulse.

Program Step 4.
Read and verify the just programmed data word. If verified, then proceed to step 5. Steps 3 and 4 may be repeated up to twenty five times before the programming attempt is considered a failure. Note that an internally generated margin voltage is applied during the verify read cycle to ensure proper programming margins are achieved.

Program Step 5.
Repeat step 3 once to provide additional cell program margin. This is recommended because programming is being done with V_{CC} set to 5.0-volts (see In-Circuit Programming Consideration above).

Program Step 6
After all desired locations have been programmed successfully, V_{PP} may optionally be returned to 5.0-volts or left at 12-volts. If left at 12-volts, write a 00h (Read Command) to the command register. This terminates the generation of the internal margin voltage normally used during the program verify mode and returns the device to the normal read state. Note that returning V_{PP} to 5.0-volts automatically returns the device to the normal read state.

Erasing
Refer to Figure 2 while following the 5 steps listed below:

Erase Step 1.
Prior to erasing, **all memory locations must be written to 00h first**! This is not an optional step - it must be performed to prevent over-erasing cells. The erase function provides a chip erase that returns all cells in the memory array to FFh when done.

Erase Step 2.
After verifying all locations read 00h, apply 12-volts to the V_{PP} pin of the memory if it is not already at 12-volts.

Erase Step 3.
Issue the setup Erase/Erase' command to the memory (see Table 1 for command definitions). This command requires two bus cycles and consists of writing 20h in two consecutive bus cycles to initiate the erase cycle. The duration of the erase cycle must be timed externally and terminated after tEW time has been reached. Termination is accomplished by writing any data to any address location in the device. The rite' is ignored by the device and only serves to reset the internal latch controlling the erase pulse.

Erase Step 4.
While maintaining 12-volts on V_{PP}, read every location in the memory array and check for FFh data. The MX26C1024A applies an internally generated margin voltage to the addressed words to help verify complete erasure of each cell. If any location fails to read FFh data, repeat steps 2 and 3 up to two hundred times. After verifying the erased state for all locations, proceed to step 5.

Erase Step 5
Repeat step 3 to provide one additional erase cycle for margin purposes, and the erase function is complete.

Erase Step 6
After successfully erasing the device, V_{PP} may optionally be returned to 5.0-volts or left at 12-volts. If left at 12-volts, write a 00h (Read Command) to the command register. This terminates the generation of the internal margin voltage normally used during the erase verify mode and returns the device to the normal read state. Note that returning V_{PP} to 5.0-volts automatically returns the device to the normal read state.

Summary
The programming algorithms described above are simple to implement in software or firmware. With the additional programming and erase cycles provided for by the recommended algorithms, cell threshold voltage (Vt) margins will be adequate even though the memory was programmed with V_{CC} set to only 5.0-volts. Hardware changes may be required to provide an active WE, but this change should be relatively easy to implement and it gives the user the flexibility of loading or modifying data held by the MTP™ memory while still in-circuit. For additional data security, the user may choose to return V_{PP} to 5-volts during normal device operation. This requires additional on-board hardware to switch the V_{PP} voltage, but it guarantees that no accidental programming or erasures can occur.

Table 1. Command Definitions

Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Reset	2	Write	X	FFH	Write	X	FFH
Read Memory	1	Write	X	00H			
Read ID Codes	2	Write	X	90H	Read	IA	ID
Setup Erase/Erase	2	Write	X	20H	Write	X	20H
Terminate Erase Pulse	1	Write	X	XXH			
Setup Program/Program	2	Write	X	40H	Write	PA	PD
Terminate Program Pulse	1	Write	X	XXH			

Note:
IA = Identifier address (00 = manufacturer code; 01 = device code)
PA = Address of memory location to be programmed
ID = Data read from location IA during device identification
PD = Data to be programmed at location PA

Figure 1. BYTE PROGRAMMING ALGORITHM

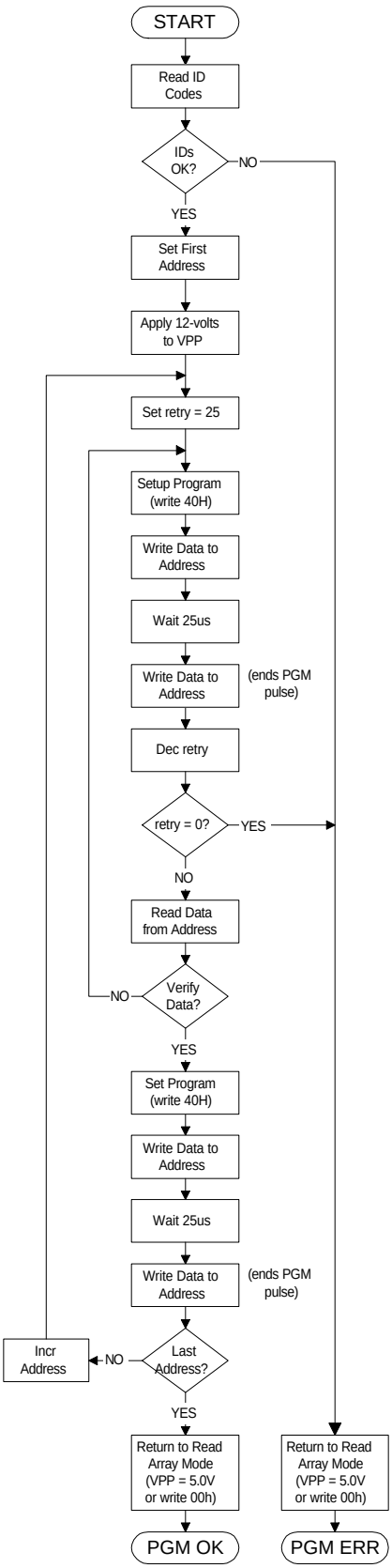

Figure 2. ERASE ALGORITHM