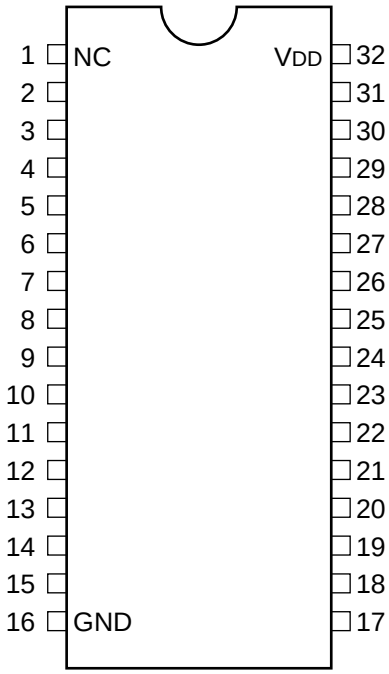
C-MOS 4 M (512 K × 8)-BIT MASK ROM

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	NC	17	O	Q3
2	I	A16	18	O	Q4
3	I	A15	19	O	Q5
4	I	A12	20	O	Q6
5	I	A7	21	O	Q7
6	I	A6	22	I	CE/$\overline{CE}$
7	I	A5	23	I	A10
8	I	A4	24	I	OE/$\overline{OE}$
9	I	A3	25	I	A11
10	I	A2	26	I	A9
11	I	A1	27	I	A8
12	I	A0	28	I	A13
13	O	Q0	29	I	A14
14	O	Q1	30	I	A17
15	O	Q2	31	I	A18
16	—	GND	32	—	VDD

A0 - A18 ; ADDRESS INPUTS
CE/$\overline{CE}$; CHIP ENABLE INPUT
OE/$\overline{OE}$; OUTPUT ENABLE
Q0 - Q7 ; DATA OUTPUTS