

MV1820

VIDEO PROGRAMME DELIVERY CONTROL INTERFACE CIRCUIT

(Supersedes version in April 1994 Consumer IC Handbook, HB3120 - 2.0)

The MV1820 is a high speed CMOS receiver for Programme Delivery Control (PDC) messages broadcast in World System Teletext (WST) Format Two Broadcast Service Data Packets (BSDP). The PDC message can be read on an I²C bus with data format similar to standard Video Programming Service (VPS) decoders. Additional data is appended to include new PDC features.

It is intended for use in Video Cassette Recorders to provide automatic recording of suitably labelled Television programmes requested by the user.

FEATURES

- On chip data slicing
- Low external component count
- I²C bus for low cost interfacing
- Advanced CMOS technology gives low power dissipation and high reliability

ABSOLUTE MAXIMUM RATINGS

Supply voltage	0.3V to 7V
All inputs	-0.3 to V _{DD} +0.3V
Operating temperature	0 to +70°C
Storage temperature	-55 to 125°C

ORDERING INFORMATION

MV1820E/CG/DPAS

MV1820E/CG/MPES

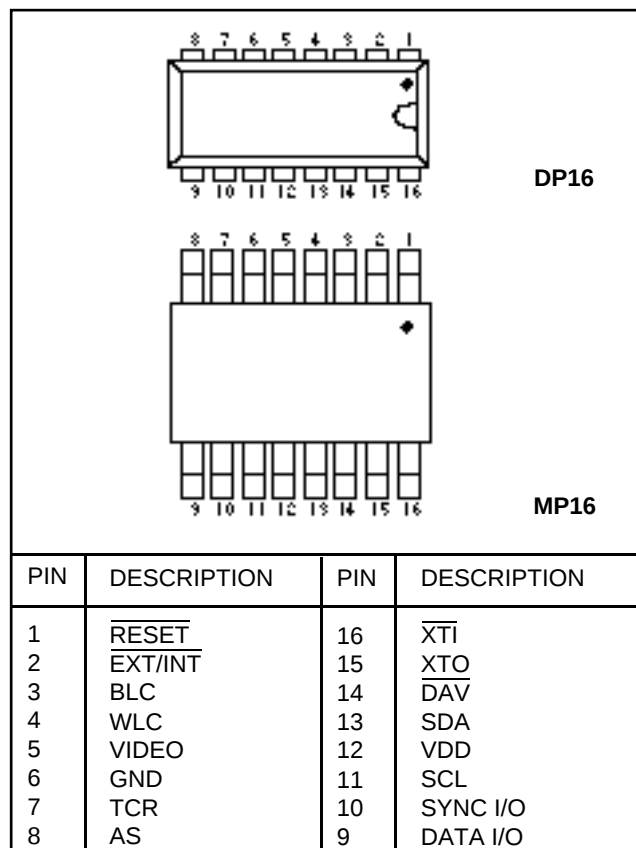


Fig.1 Pin connections - top view

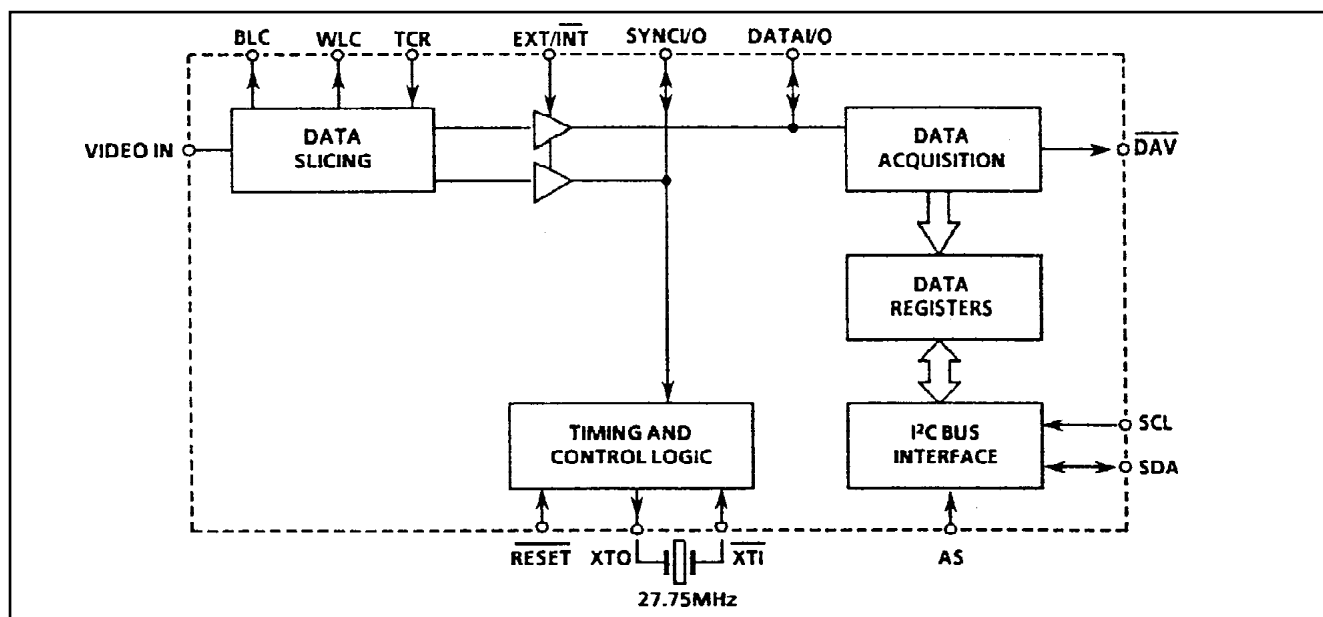


Fig.2 MV1820 block diagram

MV1820

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

$T_{amb} = 0 \text{ to } 70^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	12	4.5	5.0	5.5	V	
Supply current	12		20	25	mA	
Video input	5					
Video amplitude		0.8		3.0	V _{pp}	Bottom of sync to white (pk to pk)
Source impedance				250	W	
TCR input	7					
External resistance		4.7	4.7	200	kW	Connected to V _{DD}
BLC and WLC	3 & 4					
Capacitor value			10		nF	Connected to GND
Capacitor tolerance		-10%		+10%		
Effective series resistance				5	W	1MHz
DATA I/O and SYNC I/O	9 & 10					
Output voltage High		V _{DD} -1.0	4.5		V	I _{OH} = -1.2mA
Output voltage Low			0.2	0.4	V	I _{OL} = 2.4mA
Input voltage Low		0		0.8	V	
Input voltage High		V _{DD} -1.0		V _{DD}	V	
Input current		-30		+30	μA	V _{IN} = V _{SS} or V _{DD}
EXT/INT	2					100k (nom) pull-down resistor
Input voltage Low		0		0.8	V	
Input voltage High		V _{DD} -1.0		V _{DD}	V	
Input current Low		-10		+10	μA	V _{IN} = V _{SS}
Input current High		22	50	220	μA	V _{IN} = V _{DD}
AS	8					100k (nom) pull-down resistor
Input voltage Low		0		1.0	V	
Input voltage High		V _{DD} -1.0		V _{DD}	V	
Input current Low		-10		+10	μA	V _{IN} = V _{SS}
Input current High		22	50	220	μA	V _{IN} = V _{DD}
X _{TI} Input	16					
Input current Low		-0.5	-5.0	-20	μA	-0.3 < V _{IN} < V _{IL} max
Input current High		0.5	5.0	20	μA	V _{IHmin} < V _{IN} < (V _{DD} + 0.3)
XTO Output	15					
Output voltage High		V _{DD} -1.0	4.5		V	I _{OH} = -1.0mA
Output voltage Low			0.2	0.4	V	I _{OL} = 2.0mA
Frequency			27.750		MHz	±100ppm

ELECTRICAL CHARACTERISTICS (continued)

These characteristics are guaranteed over the following conditions (unless otherwise stated)

$T_{amb} = 0 \text{ to } 70^{\circ}\text{C}$, $V_{DD} = 5V \pm 10\%$

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
I2C bus	11, 13	0		1.5	V	Not clamped when $V_{DD} = 0V$
SCL, SDA Schmitt inputs						
Input voltage Low						
Input voltage High						
Output voltage Low	11	3.5	0.1	0.4	V	$I_{OL} = 3.0mA$
SCL clock frequency						
$\overline{DAV}$ data available						
Output voltage low						
$\overline{RESET}$ Schmitt input	1					100k (nom) pull-up resistor
Input voltage Low						
Input voltage High						
Input current Low						
Input current High						

NOTE

Input voltage low and input voltage high for $\overline{EXT/INT}$, AS and $\overline{XTI}$ are as specified for DATA I/O.

PIN DESCRIPTION	Pin	Pin Name and Description
Symbol	Pin	Pin Name and Description
$\overline{RESET}$	1	Active Low Reset. Includes a 100kW pull - up resistor
$\overline{EXT/INT}$	2	Control Pin for SYNC I/O and DATA I/O. Includes a 100kW pull - down resistor. When low or not connected, internal SYNC and DATA are used, pins 9 and 10 are outputs. When high, supply SYNC and DATA from an external source, pins 9 and 10 are inputs.
BLC	3	Black level capacitor.
WLC	4	White level capacitor.
VIDEO	5	Input for composite video signal with negative going syncs
GND	6	Ground 0 volts.
TCR	7	Time constant resistor. Controlling discharge rate of black and white level capacitor voltages.
AS	8	Address select for I²C bus. [0010 0001] with AS set high, or [0010 0011] with AS set low. Includes 100kW pull - down resistor.
DATA I/O	9	Data input/output.
SYNC I/O	10	Sync input/output.
SCL	11	I²C bus serial clock.
VDD	12	Positive supply voltage +5V $\pm$ 10%
SDA	13	I²C bus bi-directional data port.
$\overline{DAV}$	14	Active low open drain output data available signal to microprocessor. Includes 100kW pull - up resistor
XTO	15	Crystal out, 27.75MHz fundamental crystal with on-chip 1MW resistor to $\overline{XTI}$.
$\overline{XTI}$	16	Crystal input.

MV1820

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency 27.750000MHz. AT cut.
Tolerance at -10°C to 60°C ± 50 ppm.
Tolerance overall ± 100 ppm.

Nominal load capacitance 20pF.
Equivalent series resistance <20W.

FUNCTIONAL DESCRIPTION

The video signal is sliced to produce data and synchronising signals. Timing circuits monitor the sync signal to enable the MV1820 to lock onto the broadcast signal. A timing window, for the Vertical Blanking Interval (VBI) lines 6 - 22 and 318 - 335, is established to enable the acquisition circuit to monitor the sliced data signal for valid teletext data.

The framing code is checked for valid World System Teletext (WST) data. Magazine, packet and designation code bytes are checked and valid Broadcast Service Data Packets (BSDP) format two type only are accepted. These are known as packet 8/30. Format two is signalled by byte six, data bit two being set high and bits 3 and 4 set low. Bytes 13 to 25 inclusive are Hamming decoded (8,4) and stored in seven registers each of eight bits. If the complete message is correctly received with no uncorrectable Hamming errors, an interrupt to the microprocessor is signalled by the DAV (bar) pin going low. At the same time the data is transferred to a second bank of registers, reorganised with original numbered bytes 14, 15, 24, 25 and 13 placed after byte 23, to be read out on the I²C bus when so requested. Subsequent valid messages will continue to be transferred to the output registers overwriting any existing data. In this way the output registers always contain the latest PDC message.

The MV1820 is configured as an I²C bus slave transmitter with a selectable address. The I²C bus address is 0010 0001 (20 + 1 hex) with the address select (AS) pin set high, or 0010 0011 (22 + 1 hex) with the AS pin set low. The read bit (LSB) must always be set, it is not possible to write to the MV1820.

On recognising its address, the MV1820 will send an acknowledge and then transmit on the SDA line the first byte from the output registers (decoded byte 16 and 17) most

significant bit (MSB) first. It will then monitor the SDA line for an acknowledge from the microprocessor. If the microprocessor does NOT send an acknowledge, the MV1820 will release the data line to allow the microprocessor to send a stop condition. If the microprocessor does send an acknowledge, the following bytes of the message will be output provided each byte is acknowledged. The final data will be byte 13 followed by the four '1's.

When readout is complete, the DAV (bar) pin is reset high and the output registers are all set high. If the microprocessor continues to send clocks on the SCL line, the MV1820 will output FF bytes on the SDA line. Also, if the MV1820 is re-addressed before another PDC message is received, the MV1820 will output FF bytes on the SDA line. The microprocessor can prematurely stop the message by NOT sending an Acknowledge followed by a STOP condition after any byte has been sent by the MV1820. The registers will then be reset to FF bytes and the DAV pin will be reset high.

To prevent any corruption of the data in the output registers during I²C bus activity, valid PDC messages are held in the incoming registers until I²C bus activity ceases. Here they may be overwritten by new PDC messages until the I²C bus activity ceases and they can then be transferred to the output registers.

System clock is provided by an on - chip 27.75MHz oscillator together with an external parallel resonant fundamental frequency AT cut crystal.

Following a reset, RESET pulled low, the output I²C bus registers will contain FF bytes and the DAV pin will be set high. When the power supply is removed, the I²C bus will not be clamped to ground, leaving it free for other I²C bus traffic.

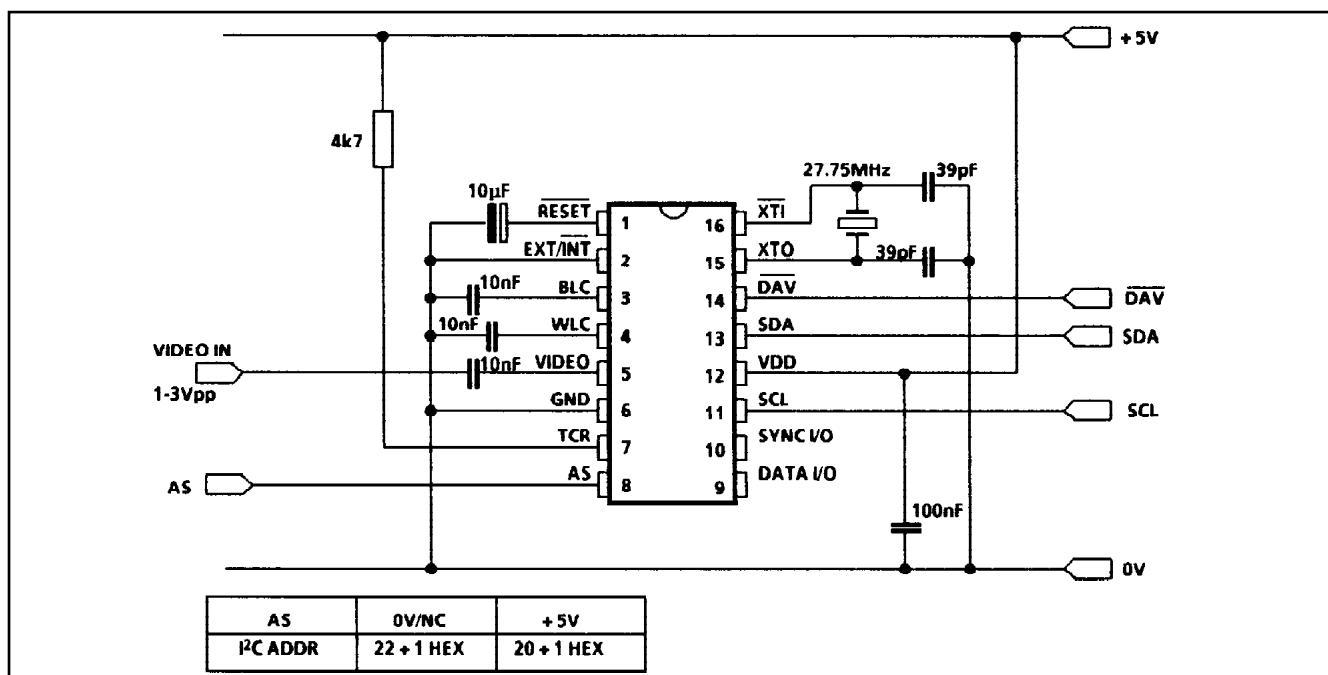


Fig.3 Typical application diagram

ORDER OF DATA OUTPUT ON THE I²C BUS

Bit Order	EBU Numbering	Bit Value	VPS Equivalence
byte 1	bit 7	____reserved	[byte 11
	bit 6	64 network (or programme provider)	
	bit 5	16	
	bit 4	8	
	bit 3	4 day	
	bit 2	2	
	bit 1	1	
	bit 0	8	
byte 2	bit 7	4	[byte 12
	bit 6	2 month	
	bit 5	1	
	bit 4	16	
	bit 3	8	
	bit 2	4 hour	
	bit 1	2	
	bit 0	1	
byte 3	bit 7	32	[byte 13
	bit 6	16	
	bit 5	8	
	bit 4	4 minute	
	bit 3	2	
	bit 2	1	
	bit 1	8	
	bit 0	4	
byte 4	bit 7	2 country	[byte 14
	bit 6	1	
	bit 5	32	
	bit 4	16	
	bit 3	8 network (or programme provider)	
	bit 2	4	
	bit 1	2	
	bit 0	1	
byte 5	bit 7	2 status (define the analog sound	[byte 5
	bit 6	1 transmission system)	
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
byte 6	bit 7	128	[byte 15
	bit 6	64	
	bit 5	32	
	bit 4	16 programme type	
	bit 3	8	
	bit 2	4	
	bit 1	2	
	bit 0	1	
byte 7	bit 7	2 Label Channel Identifier	
	bit 6	1 Interleave up to four PIL messages	
	bit 5	1 Label Update Flag (LUF)	
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		

NOTE: Data is output on the
I²C bus **MSB** first

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