

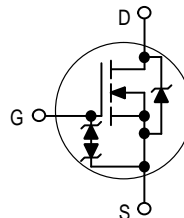
*Product Preview*

**HDTMOS E-FET™**

**Power Field Effect Transistor**  
**N-Channel Enhancement-Mode Silicon Gate**

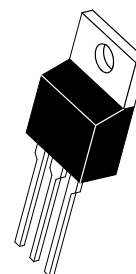
This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor-Absorbs High Energy in the Avalanche Mode
- ESD Protected. 400 V Machine Model Level and 4000 V Human Body Model Level.



**MTP35N06ZL**

**TMOS POWER FET**  
**35 AMPERES**  
**60 VOLTS**  
**R<sub>DS(on)</sub> = 26 mΩ**



**CASE 221A-06, Style 5**  
**TO-220AB**

**MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	60	Vdc
Drain-to-Gate Voltage (R <sub>GS</sub> = 1.0 MΩ)	V <sub>DGR</sub>	60	Vdc
Gate-to-Source Voltage — Continuous	V <sub>GS</sub>	±15	Vdc
— Non-Repetitive (t <sub>p</sub> ≤ 10 ms)	V <sub>GSM</sub>	±20	Vpk
Drain Current — Continuous @ T <sub>C</sub> = 25°C	I <sub>D</sub>	35	Adc
— Continuous @ T <sub>C</sub> = 100°C	I <sub>D</sub>	22.8	
— Single Pulse (t <sub>p</sub> ≤ 10 μs)	I <sub>DM</sub>	105	Apk
Total Power Dissipation @ T <sub>C</sub> = 25°C	P <sub>D</sub>	94	Watts
Derate above 25°C		0.63	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy — Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 25 Vdc, V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 5.0 Vdc, Peak I <sub>L</sub> = 35 Apk, L = 0.3 mH, R <sub>G</sub> = 25 Ω)	E <sub>AS</sub>	184	mJ
Thermal Resistance — Junction to Case	R <sub>θJC</sub>	1.6	°C/W
— Junction to Ambient	R <sub>θJA</sub>	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

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# MTP35N06ZL

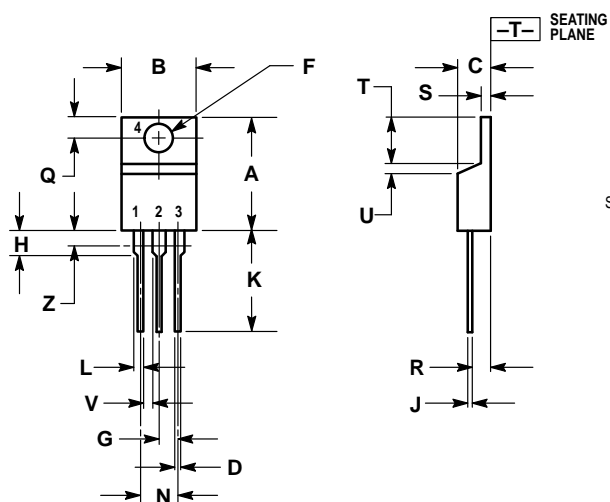
## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Cpk ≥ 3.0) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 —	— 52	— —	Vdc mV/°C	
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	— —	— —	10 100	μAdc	
Gate-Body Leakage Current (V <sub>GS</sub> = ±15 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS</sub>	—	—	5.0	μAdc	
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (Cpk ≥ 3.0) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 —	1.5 4.0	2.0 —	Vdc mV/°C	
Static Drain-to-Source On-Resistance (Cpk ≥ 2.0) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 11.5 Adc)	R <sub>DS(on)</sub>	—	22	26	mΩ	
Drain-to-Source On-Voltage (V <sub>GS</sub> = 5.0 Vdc) (I <sub>D</sub> = 23 Adc) (I <sub>D</sub> = 11.5 Adc, T <sub>J</sub> = 125°C)	V <sub>DS(on)</sub>	— —	0.78 0.7	1.1 1.0	Vdc	
Forward Transconductance (V <sub>DS</sub> = 4.0 Vdc, I <sub>D</sub> = 11.5 Adc)	g <sub>FS</sub>	10	12	—	mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	—	1600	pF	
Output Capacitance		C <sub>oss</sub>	—	560		
Transfer Capacitance		C <sub>rss</sub>	—	140		
SWITCHING CHARACTERISTICS (2)						
Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 23 Adc, V <sub>GS(on)</sub> = 5.0 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	—	40	ns	
Rise Time		t <sub>r</sub>	—	250		
Turn-Off Delay Time		t <sub>d(off)</sub>	—	130		
Fall Time		t <sub>f</sub>	—	170		
Gate Charge (See Figure 8)	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 23 Adc, V <sub>GS</sub> = 5.0 Vdc)	Q <sub>T</sub>	—	45	nC	
		Q <sub>1</sub>	—	8.0		
		Q <sub>2</sub>	—	22		
		Q <sub>3</sub>	—	19		
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage	(I <sub>S</sub> = 23 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 23 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	— —	0.92 0.81	1.1 —	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 23 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	43	ns	
		t <sub>a</sub>	—	24		
		t <sub>b</sub>	—	20		
Reverse Recovery Stored Charge		Q <sub>RR</sub>	—	0.055	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from drain lead 0.25" from package to center of die)	L <sub>D</sub>	—	3.5 4.5	—	nH	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L <sub>S</sub>	—	7.5	—	nH	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

## PACKAGE DIMENSIONS




STYLE 5:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-06  
ISSUE Y

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