Product Preview

Medium Power Surface Mount Products

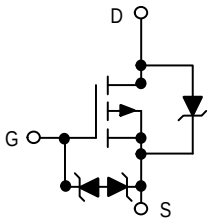
TMOS Dual P-Channel with Monolithic Zener ESD Protected Gate

MMDF2P01Z

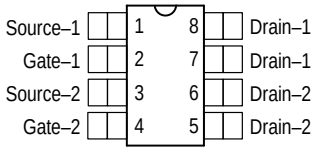
Motorola Preferred Device

DUAL TMOS POWER MOSFET 2.0 AMPERES 20 VOLTS $R_{DS(on)}$ = 0.160 OHM

EZFETs™ are an advanced series of power MOSFETs which utilize Motorola's High Cell Density TMOS process and contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.



CASE 751–05, Style 11
SO–8



- Zener Protected Gates Provide Electrostatic Discharge Protection
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) *

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 8.0	Vdc
Drain Current — Continuous @ T_A = 25°C (1) — Continuous @ T_A = 70°C (1) — Pulsed Drain Current (4)	I_D I_D I_{DM}	2.4 2.0 12	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	2.0 16	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (2) Linear Derating Factor (2)	P_D	1.39 11.11	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C

THERMAL RESISTANCE

Rating	Symbol	Typ.	Max.	Unit
Thermal Resistance — Junction to Ambient, PCB Mount (1) — Junction to Ambient, PCB Mount (2)	$R_{\theta JA}$ $R_{\theta JA}$	— —	62.5 90	°C/W

* Negative sign for P–Channel device omitted for clarity

(1) When mounted on 1 inch square FR–4 or G–10 board (V_{GS} = 10 V, @ 4.5 Seconds)

(2) When mounted on minimum recommended FR–4 or G–10 board (V_{GS} = 4.5 V, @ Steady State)

DEVICE MARKING **ORDERING INFORMATION**

	Device	Reel Size	Tape Width	Quantity
D2P01Z	MMDF2P01ZR2	13″	12 mm embossed tape	2500 units

This document contains information on a new product. Specifications and information are subject to change without notice.

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Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) *

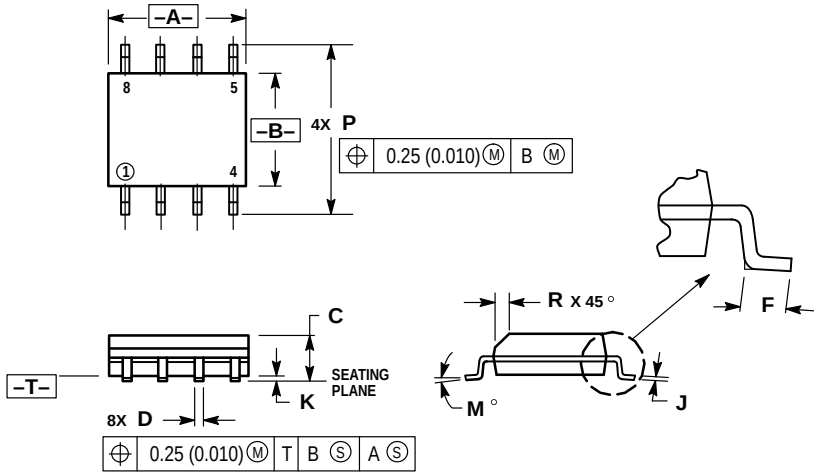
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 0.25 mAdc)			20	—	—	
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc)			—	—	2.0	
(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	10	
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	5.0	
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 0.25 mAdc)			0.7	0.9	1.1	
Threshold Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (3)		$R_{DS(on)}$				mΩ
(V_{GS} = 4.5 Vdc, I_D = 2.4 Adc)			—	120	160	
(V_{GS} = 2.7 Vdc, I_D = 1.2 Adc)			—	170	190	
Forward Transconductance		g_{FS}				Mhos
(V_{DS} = 2.5 Vdc, I_D = 1.0 Adc)			3.0	4.0	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 10 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	345	690	pF
Output Capacitance		C_{oss}	—	360	720	
Transfer Capacitance		C_{rss}	—	125	250	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DS} = 6.0 Vdc, I_D = 2.4 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	60	85	ns
Rise Time		t_r	—	325	455	
Turn–Off Delay Time		$t_{d(off)}$	—	400	560	
Fall Time		t_f	—	485	680	
Turn–On Delay Time	(V_{DS} = 6.0 Vdc, I_D = 2.4 Adc, V_{GS} = 2.7 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	120	170	ns
Rise Time		t_r	—	1060	1490	
Turn–Off Delay Time		$t_{d(off)}$	—	225	315	
Fall Time		t_f	—	530	740	
Gate Charge (see figure 8)	(V_{DS} = 10 Vdc, I_D = 2.4 Adc, V_{GS} = 4.5 Vdc)	Q_T	—	10	14	nC
		Q_1	—	0.65	—	
		Q_2	—	4.8	—	
		Q_3	—	3.3	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 2.4 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.2	1.5	Vdc
	(I_S = 2.4 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	TBD	—	
Reverse Recovery Time	(I_S = 2.4 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	500	—	ns
		t_a	—	150	—	
		t_b	—	350	—	
Reverse Recovery Storage Charge		Q_{RR}	—	2.8	—	μC

* Negative sign for P–Channel device omitted for clarity

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

CASE 751–05
SO–8
ISSUE M

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