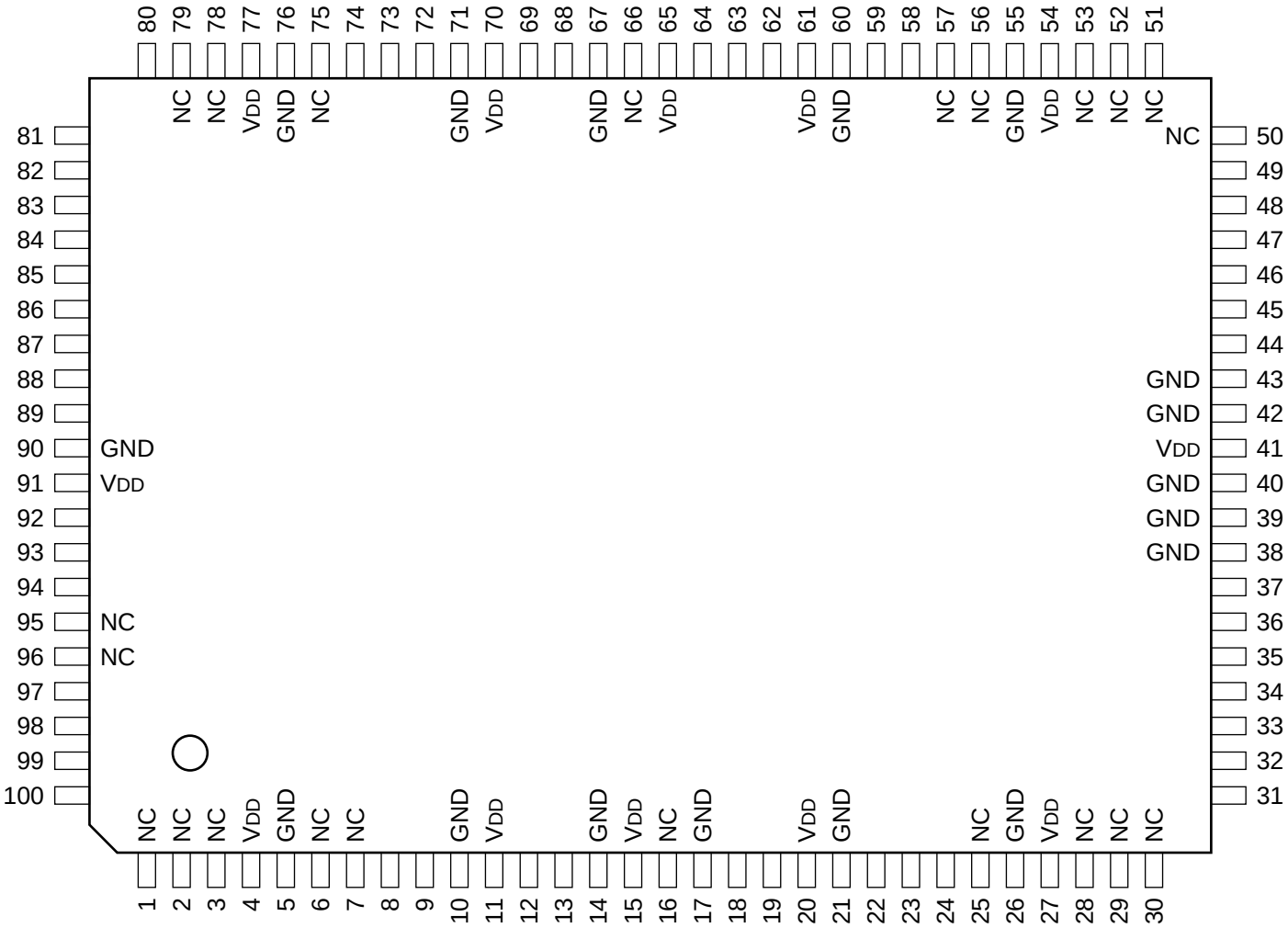
# C-MOS (128 K × 18)-BIT SYNCBURST SRAM

—TOP VIEW—



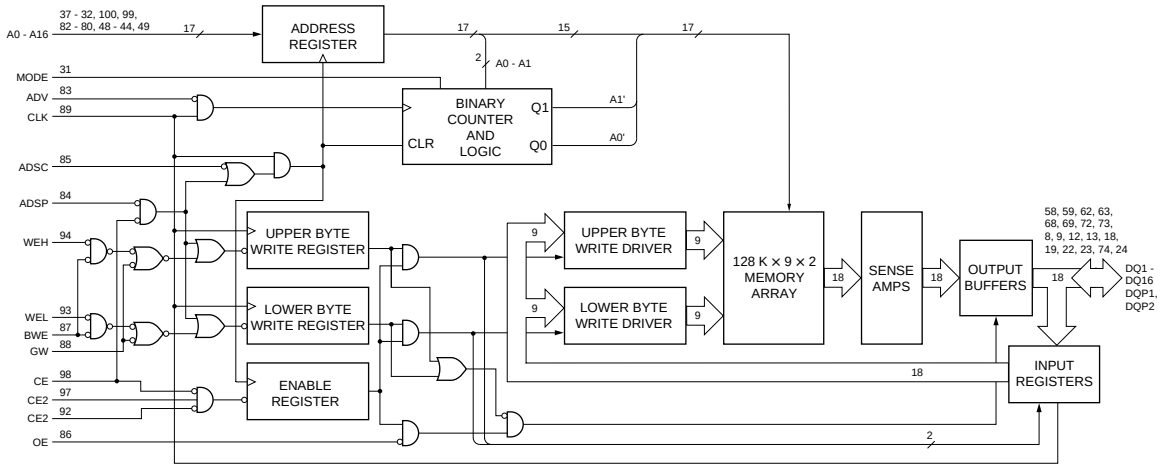
| PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | — | NC | 26 | — | GND | 51 | — | NC | 76 | — | GND |
| 2 | — | NC | 27 | — | $V_{DD}$ | 52 | — | NC | 77 | — | $V_{DD}$ |
| 3 | — | NC | 28 | — | NC | 53 | — | NC | 78 | — | NC |
| 4 | — | $V_{DD}$ | 29 | — | NC | 54 | — | $V_{DD}$ | 79 | — | NC |
| 5 | — | GND | 30 | — | NC | 55 | — | GND | 80 | I | A10 |
| 6 | — | NC | 31 | I | MODE | 56 | — | NC | 81 | I | A9 |
| 7 | — | NC | 32 | I | A5 | 57 | — | NC | 82 | I | A8 |
| 8 | I/O | DQ9 | 33 | I | A4 | 58 | I/O | DQ1 | 83 | I | $\overline{ADV}$ |
| 9 | I/O | DQ10 | 34 | I | A3 | 59 | I/O | DQ2 | 84 | I | $\overline{ADSP}$ |
| 10 | — | GND | 35 | I | A2 | 60 | — | GND | 85 | I | $\overline{ADSC}$ |
| 11 | — | $V_{DD}$ | 36 | I | A1 | 61 | — | $V_{DD}$ | 86 | I | $\overline{OE}$ |
| 12 | I/O | DQ11 | 37 | I | A0 | 62 | I/O | DQ3 | 87 | I | $\overline{BWE}$ |
| 13 | I/O | DQ12 | 38 | — | GND | 63 | I/O | DQ4 | 88 | I | $\overline{GW}$ |
| 14 | — | GND | 39 | — | GND | 64 | I | ZZ | 89 | I | CLK |
| 15 | — | $V_{DD}$ | 40 | — | GND | 65 | — | $V_{DD}$ | 90 | — | GND |
| 16 | — | NC | 41 | — | $V_{DD}$ | 66 | — | NC | 91 | — | $V_{DD}$ |
| 17 | — | GND | 42 | — | GND | 67 | — | GND | 92 | I | $\overline{CE2}$ |
| 18 | I/O | DQ13 | 43 | — | GND | 68 | I/O | DQ5 | 93 | I | $\overline{WEL}$ |
| 19 | I/O | DQ14 | 44 | I | A15 | 69 | I/O | DQ6 | 94 | I | $\overline{WEH}$ |
| 20 | — | $V_{DD}$ | 45 | I | A14 | 70 | — | $V_{DD}$ | 95 | — | NC |
| 21 | — | GND | 46 | I | A13 | 71 | — | GND | 96 | — | NC |
| 22 | I/O | DQ15 | 47 | I | A12 | 72 | I/O | DQ7 | 97 | I | CE2 |
| 23 | I/O | DQ16 | 48 | I | A11 | 73 | I/O | DQ8 | 98 | I | $\overline{CE}$ |
| 24 | I/O | DQP2 | 49 | I | A16 | 74 | I/O | DQP1 | 99 | I | A7 |
| 25 | — | NC | 50 | — | NC | 75 | — | NC | 100 | I | A6 |

**INPUT**

| | | |
|---|---|---|
| A0 - A16 | : | SYNCHRONOUS ADDRESS |
| ADSC | : | SYNCHRONOUS ADDRESS STATUS CONTROLLER |
| ADSP | : | SYNCHRONOUS ADDRESS STATUS PROCESSOR |
| ADV | : | SYNCHRONOUS ADDRESS ADVANCE |
| BWE | : | BYTE WRITE ENABLE |
| CE, CE2 | : | SYNCHRONOUS CHIP ENABLE |
| CLK | : | CLOCK |
| GW | : | GLOBAL WRITE |
| MODE | : | LINEAR BURST/INTERLEAVED BURST SELECT |
| OE | : | OUTPUT ENABLE |
| WEH, WEL | : | SYNCHRONOUS BYTE WRITE ENABLES |
| ZZ | : | SNOOZE ENABLE |

**INPUT/OUTPUT**

| | | |
|---|---|---|
| DQ1 - DQ16 | : | SRAM DATA |
| DQP1, DQP2 | : | PARITY DATA |


37 - 32, 100, 99,
82 - 80, 48 - 44, 49
A0 - A16
17
ADDRESS REGISTER
17
15
17
2
A0 - A1
MODE
31
ADV
83
CLK
89
BINARY COUNTER AND LOGIC
CLR
Q1
Q0
A1'
A0'
ADSC
85
ADSP
84
WEH
94
WEL
93
BWE
87
GW
88
CE
98
CE2
97
CE2
92
OE
86
UPPER BYTE WRITE REGISTER
LOWER BYTE WRITE REGISTER
ENABLE REGISTER
9
UPPER BYTE WRITE DRIVER
LOWER BYTE WRITE DRIVER
9
9
128 K × 9 × 2 MEMORY ARRAY
18
SENSE AMPS
18
OUTPUT BUFFERS
18
58, 59, 62, 63,
68, 69, 72, 73,
8, 9, 12, 13, 18,
19, 22, 23, 74, 24
DQ1 - DQ16
DQP1, DQP2
18
INPUT REGISTERS
2