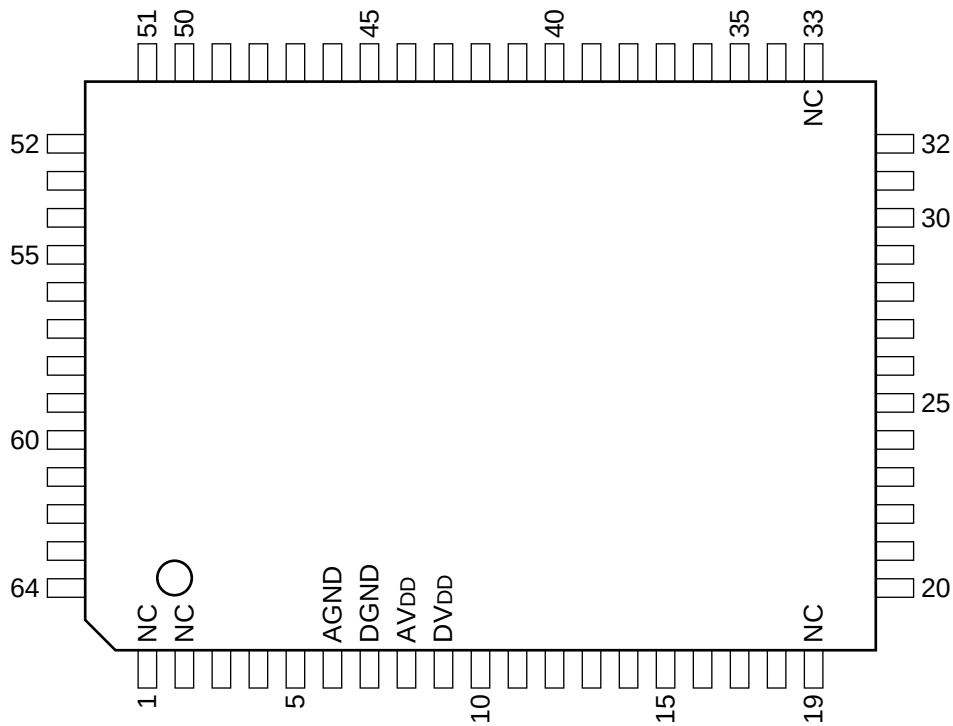


C-MOS VOICE SYNTHESIS

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	NC	14	I	RND	27	I	A2	40	I	D7	53	O	RA12
2	—	NC	15	I	XT/CR	28	I	TEST3	41	O	RA0	54	O	RA13
3	O	BUSY	16	I	CPU	29	I	RESET	42	O	RA1	55	O	RA14
4	O	NAR	17	I	TEST2	30	O	CE	43	O	RA2	56	O	RA15
5	O	AOUT	18	O	IBUSY	31	I	RCS	44	O	RA3	57	O	RA16
6	—	AGND	19	—	NC	32	I	D0	45	O	RA4	58	O	RA17
7	—	DGND	20	O	STANDBY	33	—	NC	46	O	RA5	59	O	RA18
8	—	AVDD	21	I	SW0	34	I	D1	47	O	RA6	60	O	RA19
9	—	DVDD	22	I	SW1	35	I	D2	48	O	RA7	61	O	RA20
10	I	XT/OSC1	23	I	SW2	36	I	D3	49	O	RA8	62	O	RA21
11	O	XT/OSC2	24	I	SW3	37	I	D4	50	O	RA9	63	O	RA22
12	O	OSC3	25	I	A0	38	I	D5	51	O	RA10	64	I	STBY
13	I	TEST1	26	I	A1	39	I	D6	52	O	RA11			

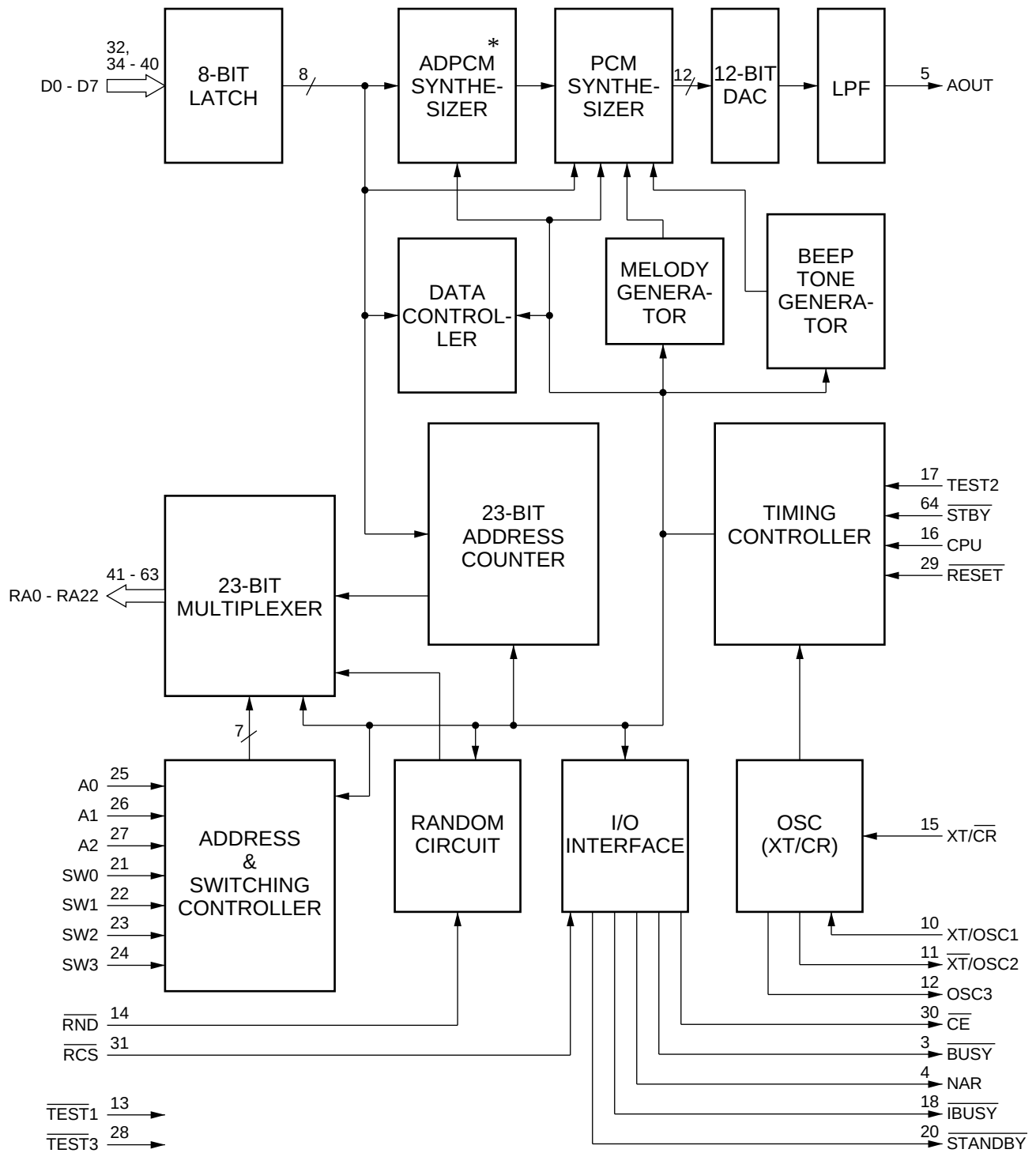
40	D7	AOUT	5
39	D6		
38	D5	RA22	63
37	D4	RA21	62
36	D3	RA20	61
35	D2	RA19	60
34	D1	RA18	59
32	D0	RA17	58
		RA16	57
27	A2	RA15	56
26	A1	RA14	55
25	A0	RA13	54
24	SW3	RA12	53
23	SW2	RA11	52
22	SW1	RA10	51
21	SW0	RA9	50
14	RND	RA8	49
31	RCS	RA7	48
15	XT/CR	RA6	47
10	XT/OSC1	RA5	46
64	STBY	RA4	45
16	CPU	RA3	44
29	RESET	RA2	43
13	TEST1	RA1	42
17	TEST2	RA0	41
28	TEST3		
		XT/OSC2	11
		OSC3	12
		CE	30
		BUSY	3
		NAR	4
		IBUSY	18
		STANDBY	20

INPUT

A0 - A1	; AUDIO PHRASE
CPU	; MICROCOMPUTER INTERFACE
D0-D7	; DATA
RCS	; ADDRESS OUTPUT SELECT
RESET	; INITIALIZE
RND	; RANDOM AUDIO
STBY	; STANDBY CONTROL
SW0 - SW3	; AUDIO PHRASE
TEST1, 3	; TEST
TEST2	; TEST
XT/CR	; OSC. SELECT
XT/OSC1	; OSC. CONNECTION

OUTPUT

AOUT	; ANALOG AUDIO
BUSY	; BUSY
CE	; MEMEORY WRITE ENABLE
IBUSY	; AUDIO EMITTING STATUS
NAR	; REGISTER STATUS
OSC3	; CR OSC. CONNECT
RA0 - RA22	; ADDRESS (TO MEMORY)
STANDBY	; STANDBY STATUS
XT/OSC2	; OSC. CONNECTION



* ADPCM ; ADAPTIVE DIFFERENTIAL PULSE CODE MODULATION