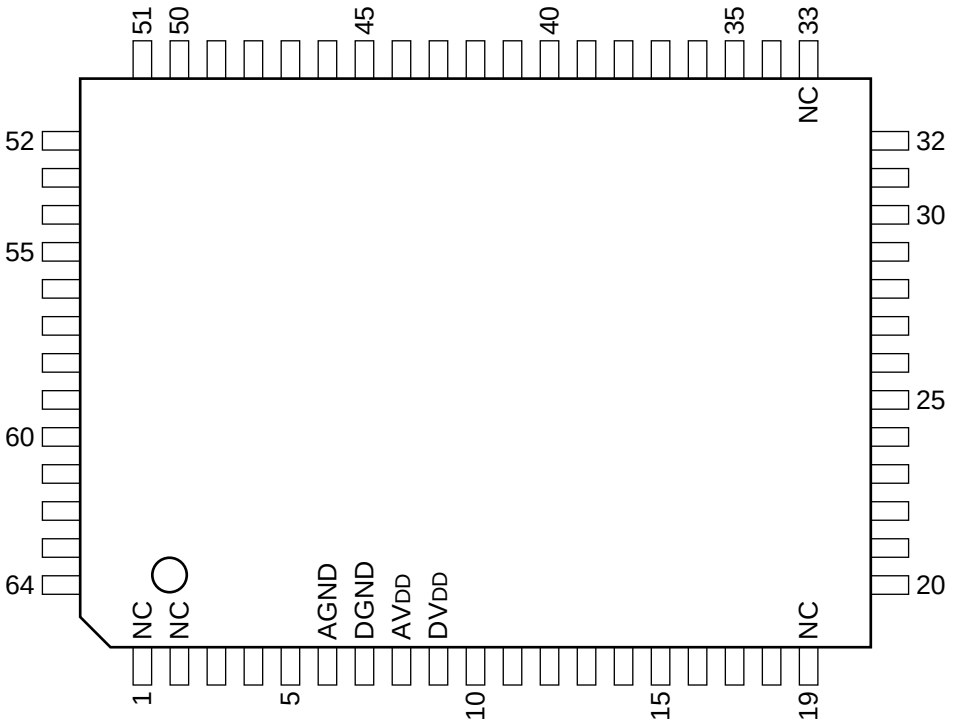
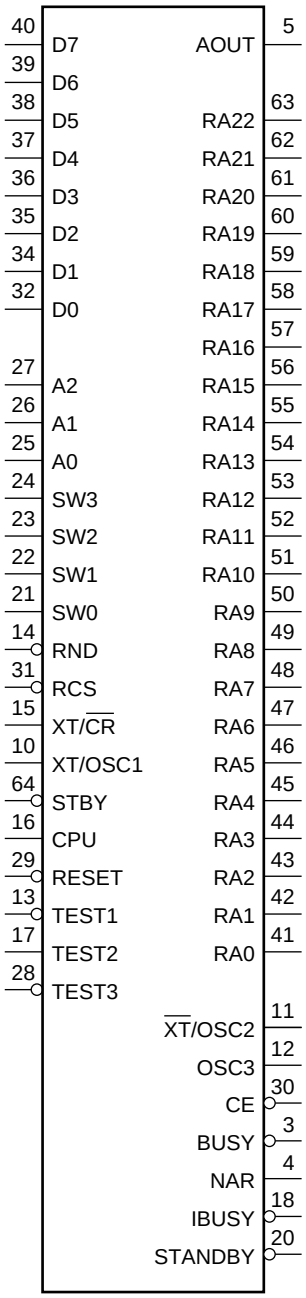
C-MOS VOICE SYNTHESIS

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	NC	14	I	$\overline{\text{RND}}$	27	I	A2	40	I	D7	53	O	RA12
2	—	NC	15	I	XT/$\overline{\text{CR}}$	28	I	$\overline{\text{TEST3}}$	41	O	RA0	54	O	RA13
3	O	$\overline{\text{BUSY}}$	16	I	CPU	29	I	$\overline{\text{RESET}}$	42	O	RA1	55	O	RA14
4	O	NAR	17	I	TEST2	30	O	$\overline{\text{CE}}$	43	O	RA2	56	O	RA15
5	O	AOUT	18	O	$\overline{\text{IBUSY}}$	31	I	$\overline{\text{RCS}}$	44	O	RA3	57	O	RA16
6	—	AGND	19	—	NC	32	I	D0	45	O	RA4	58	O	RA17
7	—	DGND	20	O	$\overline{\text{STANDBY}}$	33	—	NC	46	O	RA5	59	O	RA18
8	—	AV_{DD}	21	I	SW0	34	I	D1	47	O	RA6	60	O	RA19
9	—	DV_{DD}	22	I	SW1	35	I	D2	48	O	RA7	61	O	RA20
10	I	XT/OSC1	23	I	SW2	36	I	D3	49	O	RA8	62	O	RA21
11	O	$\overline{\text{XT}}$/OSC2	24	I	SW3	37	I	D4	50	O	RA9	63	O	RA22
12	O	OSC3	25	I	A0	38	I	D5	51	O	RA10	64	I	$\overline{\text{STBY}}$
13	I	$\overline{\text{TEST1}}$	26	I	A1	39	I	D6	52	O	RA11			

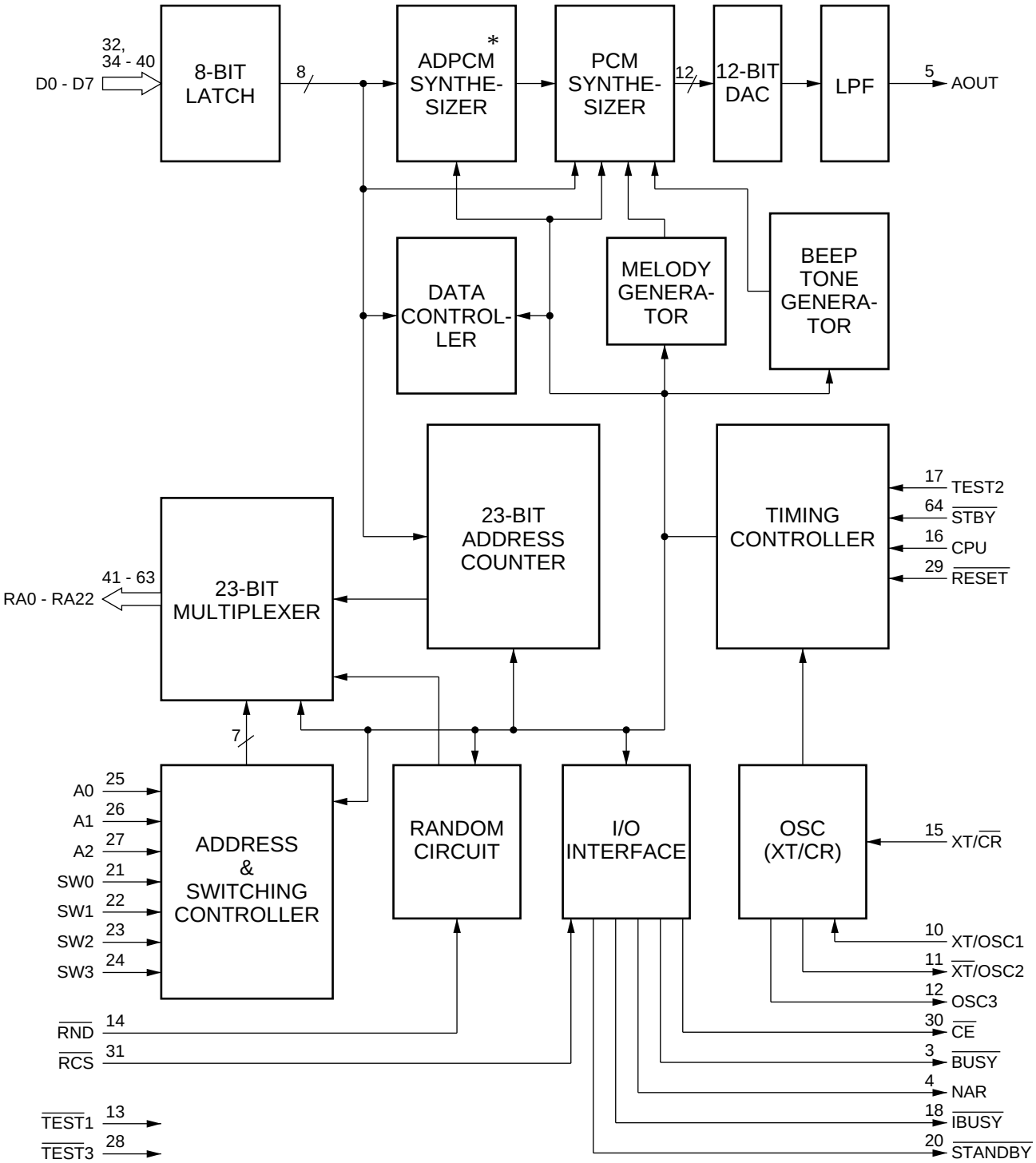


INPUT

A0 - A1	;	AUDIO PHRASE
CPU	;	MICROCOMPUTER INTERFACE
D0-D7	;	DATA
$\overline{RCS}$	;	ADDRESS OUTPUT SELECT
$\overline{RESET}$	;	INITIALIZE
$\overline{RND}$	;	RANDOM AUDIO
$\overline{STBY}$	;	STANDBY CONTROL
SW0 - SW3	;	AUDIO PHRASE
$\overline{TEST}$1, 3	;	TEST
TEST2	;	TEST
XT/$\overline{CR}$	;	OSC. SELECT
XT/OSC1	;	OSC. CONNECTION

OUTPUT

AOUT	;	ANALOG AUDIO
$\overline{BUSY}$	;	BUSY
$\overline{CE}$	;	MEMEORY WRITE ENABLE
$\overline{IBUSY}$	;	AUDIO EMITTING STATUS
NAR	;	REGISTER STATUS
OSC3	;	CR OSC. CONNECT
RA0 - RA22	;	ADDRESS (TO MEMORY)
$\overline{STANDBY}$	;	STANDBY STATUS
$\overline{XT}$/OSC2	;	OSC. CONNECTION



* ADPCM ; ADAPTIVE DIFFERENTIAL PULSE CODE MODULATION