OKI semiconductor

MSM16911

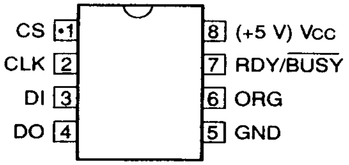
1,024-BIT SERIAL E^{2}PROM

FEATURES

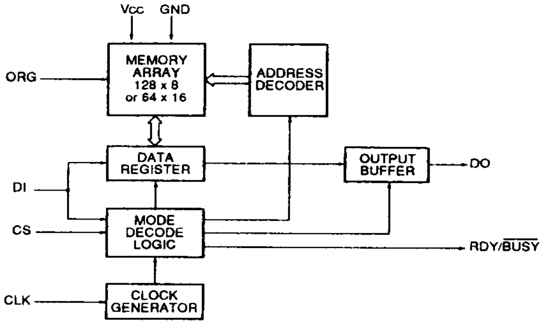
- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 64 x 16 or 128 x 8 user selectable serial memory
- Compatible with GI5911
- Self timed programming cycle with Auto-Erase
- Word and chip erasable
- Operating range 0°C to 70°C
- 10,000 erase/write cycles
- 10 year data retention

PIN CONFIGURATION (TOP VIEW)

8 Pin Dual-In-Line
8 Pin S.O. Package



FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTIONS

CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, an internal pull-up device selects the 64 x 16 organization.
CLK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
Vcc	+5 V Power Supply		
RDY/$\overline{\text{BUSY}}$	Status Output		
GND	Ground		

INSTRUCTION SET							
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x16	128 x 8	64 x16	
READ	1	1000	$A_6 - A_0$	$A_5 - A_0$			Read Address $A_N - A_0$
PROGRAM	1	x100	$A_6 - A_0$	$A_5 - A_0$	$D_7 - D_0$	$D_{15} - D_0$	Program Address $A_N - A_0$
PEN	1	0011	0000000	000000			Program Enable
PDS	1	0000	0000000	000000			Program Disable
ERAL	1	0010	0000000	000000			Erase All Addresses
WRAL	1	0001	0000000	000000	$D_7 - D_0$	$D_{15} - D_0$	Write All Addresses

DI/DO: The Data In and Data Out pins can be tied together, however bus contention can occur if A0 is held at a high level during the required dummy bit (logical 0) that precedes the read operation. Under these conditions, the voltage level on the Data Out pin is undefined and depends on the relative impedance between the signal source driving A0 and the Data Out pin. The higher the current sourcing capability of the signal driving A0, the higher the voltage level is on the Data Out pin.

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until Vcc reaches a level of approximately 3.0 volts. During power-down the source data protection circuitry acts to inhibit all modes when Vcc falls below the voltage range of approximately 3.0 volts.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATING

Rating	Symbol	Conditions	Value	Unit
Supply Voltage	V_{CC}	Ta = 25°C	–0.3 ~ 7	V
Input Voltage	V_I		–0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_O		–0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		–55 ~ + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Conditions	Range	Unit
Supply Voltage	V_{CC}	–	5 ± 10%	V
Temperature Range	Ta	–	0 ~ 70	°C
Data Hold Temperature	Ta	–	0 ~ 70	°C

DC CHARACTERISTICS

(Vcc = 4.5V to 5.5V, Ta = 0°C ~ 70°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Value		Unit	Notes
			Min	Max		
Supply Voltage	V_{CC}	–	4.5	5.5	V	
Power Supply Current	I_{CC1}	V_{CC} = 5.0 V CS = 1	–	3	mA	
	I_{CC2}	V_{CC} = 5.5 V CS, CLK, DI = 0V DO, ORG = OPEN	–	100	μA	
"L" Input Voltage	V_{IL}	–	–0.1	0.8	V	
"H" Input Voltage	V_{IH}	–	2.0	V_{CC}^{+1}	V	
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA	–	0.4	V	
		CMOS I_{OL} = 100 μA	–	0.1	V	
"H" Output Voltage	V_{OH}	TTL I_{OH} = -400 μA	2.4	–	V	
		CMOS I_{OH} = -100 μA	$V_{CC}^{-0.5}$	–	V	
Input Leakage Current	I_{LI}	V_{in} = 5.5 V	–	10	μA	
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0	–	10	μA	

AC CHARACTERISTICS

(Vcc = 4.5V to 5.5V, Ta = 0°C ~ 70°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min	Typ	Max		
CLK Frequency	f_{CLK}	–	0	–	250	kHz	–
CS Setup Time Referenced to CLK Falling	t_{CSS}	–	0.2	–	–	μs	–
CS Hold Time Referenced to CLK Rising	t_{CSH}	–	0.1	–	–	μs	–
DI Setup Time Referenced to CLK Rising	t_{DIS}	–	0.4	–	–	μs	–
DI Hold Time Referenced to CLK Rising	t_{DIH}	–	0.4	–	–	μs	–
CLK Pulse High Time	t_{CPH}	–	1.0	–	–	μs	–
CLK Pulse Low Time	t_{CPL}	–	1.0	–	–	μs	–
Delay Time of DO Rising Referenced to CLK Rising	t_{PD1}	–	–	–	2.0	μs	1
Delay Time of DO Falling Referenced to CLK Rising	t_{PD0}	–	–	–	2.0	μs	1
"L" Time of Status (Programming Time)	t_P	–	–	–	10	ms	–

Note 1: Condition: C_L = 100pF and $V_{OL/OH}$ = 0.8/2.0

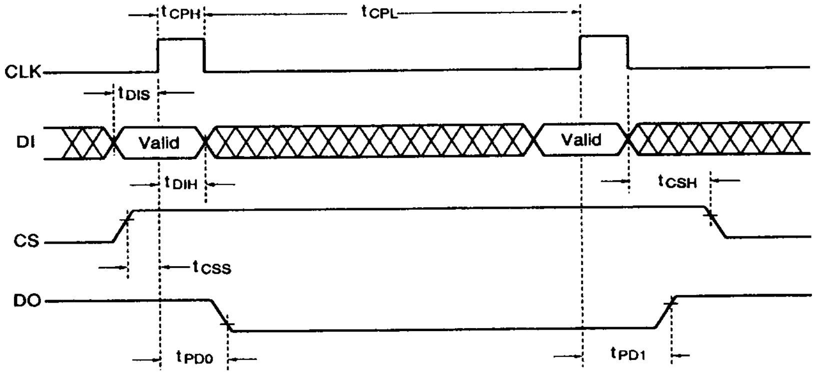


Figure 1. Synchronous Data Timing

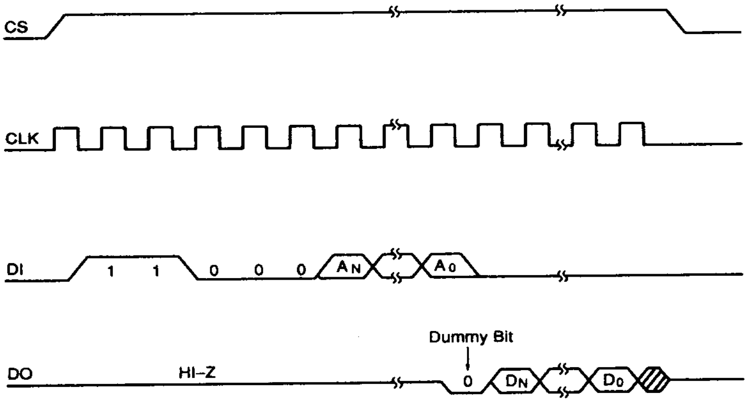


Figure 2. READ

Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

The READ instruction is the only instruction that outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register to a serial-out shift register. A dummy bit (logical 0) procedes the data output string. The output data changes during the high states of the system clock.

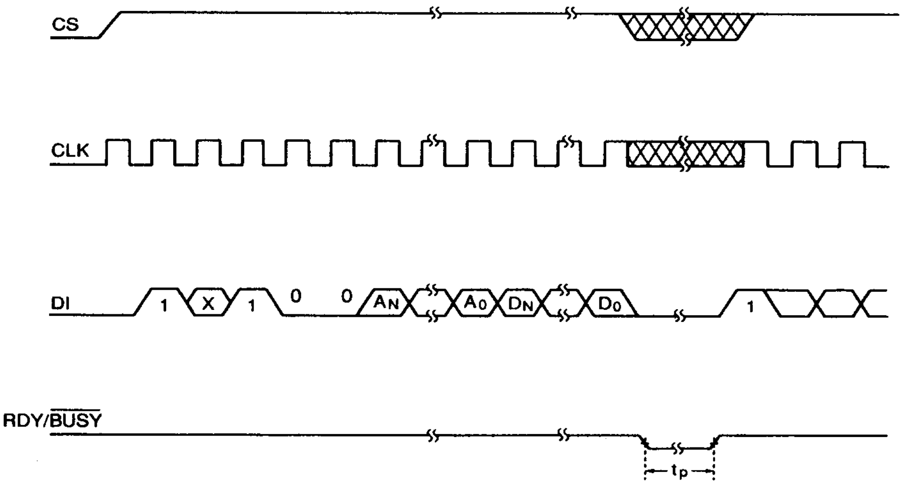


Figure 3. PROGRAM

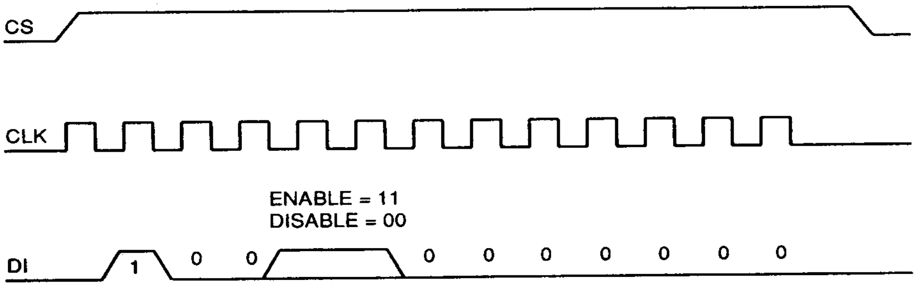
Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

The program instruction is followed by either 8 or 16 bits of data, which are written into the specified address.

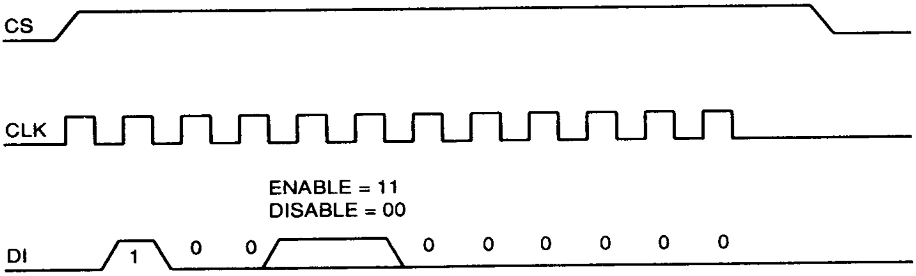
After the last data bit (D0) is shifted into the data register the contents of the specified address are erased and the new data is written to the same address.

During the automatic erase/write sequence the RDY/$\overline{\text{BUSY}}$ output goes low for the duration of the automatic programming cycle as indicated by tp.

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location can be erased by programming that address with all 1's.



PEN AND PDS FOR 128 x 8 ORGANIZATION



PEN AND PDS FOR 64 x 16 ORGANIZATION

Figure 4. PEN (Program Enable) and PDS (Program Disable)

Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction prevents an accidental loss of data. Execution of a READ instruction is independent of both PEN and PDS instructions.

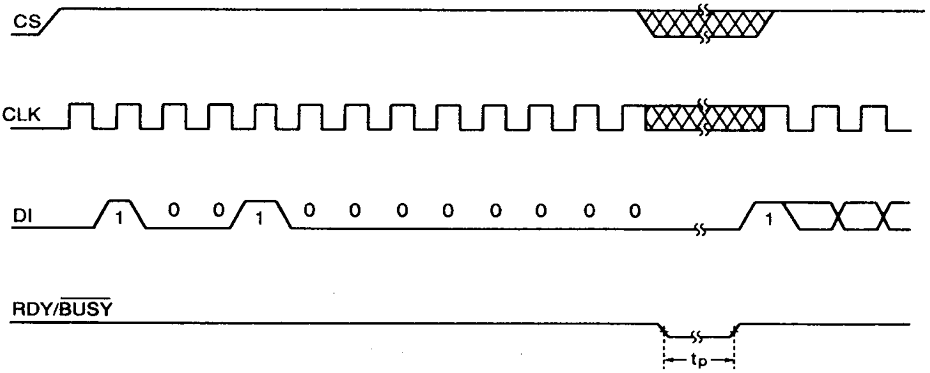
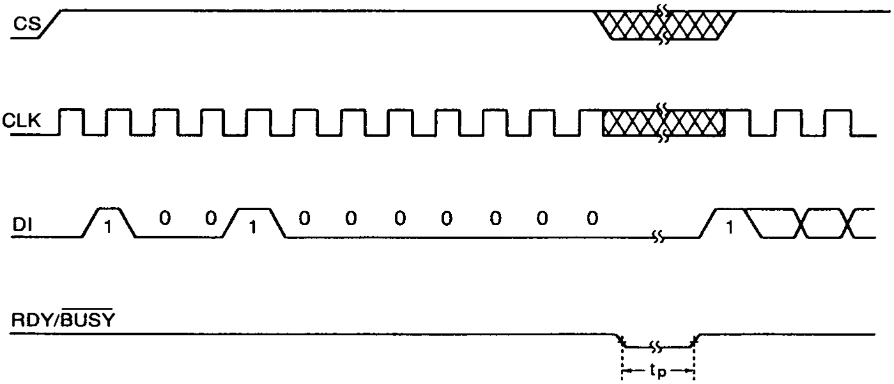


Figure 5. ERAL (Erase All)(128 x 8)



ERAL (Erase All) (64 x 16)

Entire chip erasing is implemented with the ERAL (erase all registers) instruction. Erasing the chip means that all registers in the memory array have each bit set to 1.

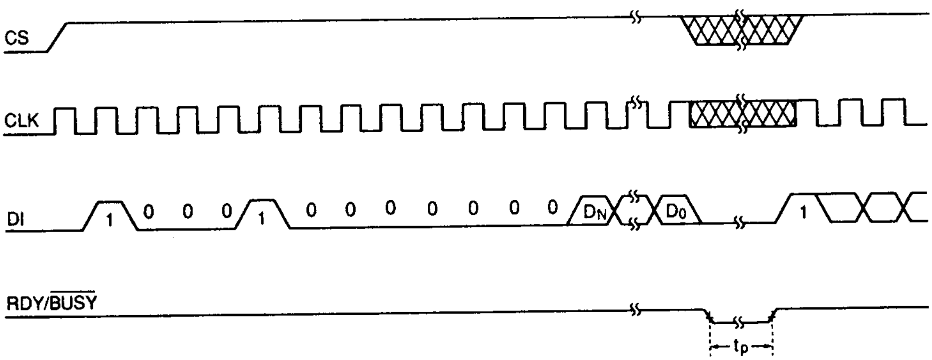
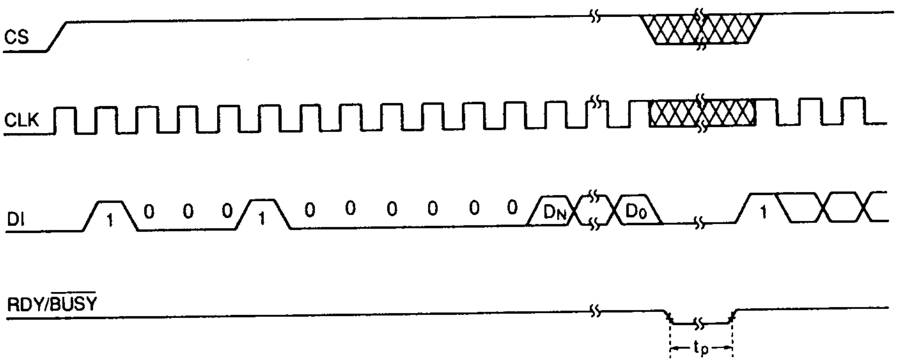


Figure 6. WRAL (Write All) (128 x 8)



WRAL (Write All) (64 x 16)

Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

The Write All (WRAL) instruction writes to all registers simultaneously. The registers must be erased before performing a WRAL instruction. After a WRAL instruction is shifted in, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self timed write sequence starts. The RDY/$\overline{\text{BUSY}}$ pin is a status indicator. It remains low while the chip is programming. It goes high after all bits of the array are set to their proper values.