MSC60028

POWER FACTOR CONTROLLER

The MSC60028 Power Factor Controller allows the construction of a high performance, low-cost off-line regulator with the following advantages:-

(i) Corrects the power factor to near unity across a wide range of load conditions
(ii) Maintains a stabilised dc output voltage
(iii) Substantially reduces peak currents - thus reducing stress on circuit components.

FEATURES

- Regulates Boost Converter output voltage to 390V DC ±5%
- Maintains typical power factor of 0.99
- Requires no current transformer
- Trimmed internal voltage reference
- Overvoltage sensing eliminates output voltage runaway
- May be operated in the continuous current mode to minimise line filtering requirement
- Uncommitted op-amp for extra flexibility*
- Low power CMOS simplifies line-derived power supply
- International voltage operation without selector switches

APPLICATIONS

- Fluorescent lamp ballasts
- Switched Mode Power Supplies
- Uninterruptible Power Supplies
- Motor Control Inverters

ORDERING INFORMATION

MSC60028/IG/DP1S - 18 pin Plastic DIL
MSC60028/IG/NP1S - 20 pin Miniature Plastic DIL SSOP
* MSC60028/IG/DP2S - 14 pin Plastic DIL
(no uncommitted opamp)

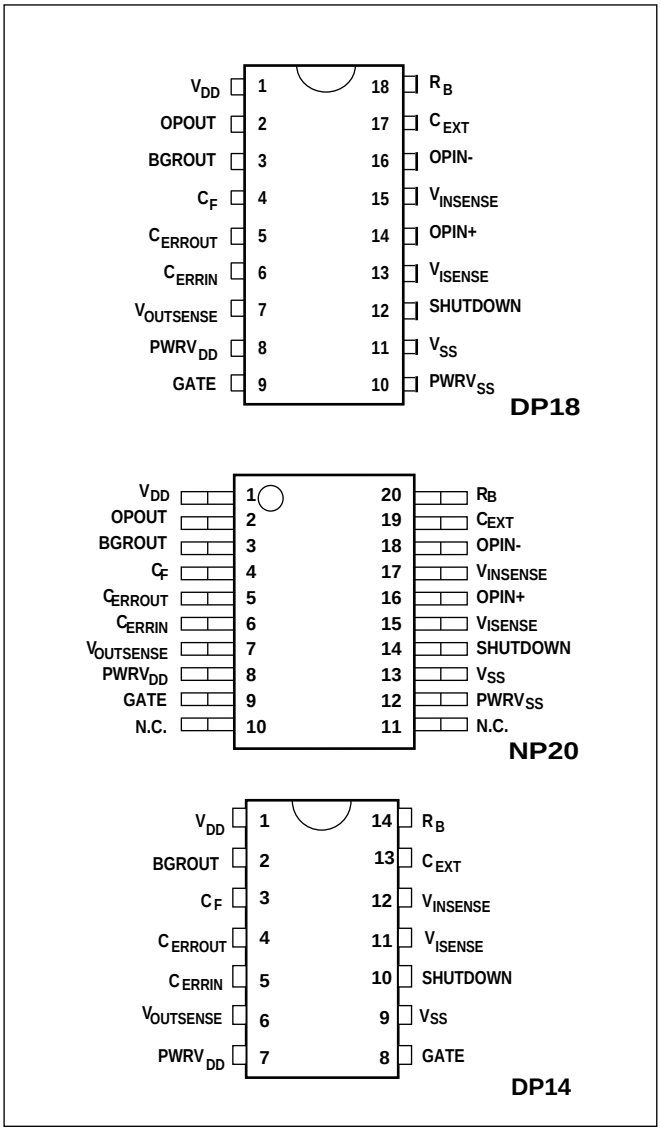


Fig.1 Pin connections (top view)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = –25°C to +85°C, V_{DD} –V_{SS} = +9V to +11V, $PWRV_{DD}$ –$PWRV_{SS}$ = +9V to +11V, V_{SS} –$PWRV_{SS}$ = 0V

Characteristic	Min.	Typ.	Max.	Units
Operating supply voltage	9[1]	10	11	V
Current consumption	9	10	12	mA
Power dissipation[2]	90	100	120	mW
Power factor	-	0.99	-	-
Bandgap reference decoupling voltage	1.21	1.28	1.38	V
Oscillator circuit				
Peak-peak voltage	2.23	2.35	2.44	V
Offset voltage	2.44	2.52	2.52	V
Charging current[6]	229	250	268	µA
Gate driver output				
Output source current[6] V_{GATE} = 8V	150	-	225	mA
Output source current[6] V_{GATE} = 9V	30	-	60	mA
Output sink current[6] V_{GATE} = 2V	-150	-	-225	mA
Output sink current[6] V_{GATE} = 1V	-50	-	-75	mA
GATE-$PWRV_{SS}$ pull-down resistance	-	100	-	kΩ
SHUTDOWN low level input voltage	-	-	0.8	V
SHUTDOWN high level input voltage	3.37	-	-	V
SHUTDOWN pull-down resistance	58	120	300	kΩ
Error amplifier				
Input resistance	157	220	286	kΩ
Gain	137	146	155	
Multiplier circuit				
C_F output impedance	-	30	-	kΩ
Under voltage lockout				
Upper threshold	7.69	8	8.24	V
Lower threshold	6.69	7	7.21	V
Hysteresis	-	1	-	V
Propagation delay	-	500	-	ns
Over voltage protection				
Input offset voltage	-10	-	10	mV
Input common mode range	1.5	-	9.0	V
Hysteresis	-	120	-	mV
Threshold voltage (rising)	5.19	5.36	5.54	V
Propagation delay	-	500	-	ns
Uncommitted Op-amp				
Input offset voltage	-10	-	10	mV
Open loop gain[3]	-	90	-	dB
CMRR	-	28	-	dB
Input common mode range	0	-	5	V
Output sink current[4]	100	-	-	µA
Output source current[5]	-	-	-100	µA
Unity gain bandwidth[7]	-	2.5	-	MHz

NOTES:
1. Except whilst Undervoltage Lockout circuit is active in which case minimum = 7V
2. f_{CLK} = 50kHz
3. Load resistance = 10kΩ
4. V_{GATE} = 1V
5. V_{GATE} = 9V
6. R_B = 200kΩ
7. No load

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min.	Max.	Units
Supply voltage V_{DD} - V_{SS} , $PWRV_{DD}$ - $PWRV_{SS}$	-0.3	12	V
Digital input voltage	V_{SS}-0.3	V_{DD}+0.3	V
Operating temperature	-25	+85	°C
Storage temperature	-55	+150	°C

PIN FUNCTIONS

- 18 Pin DIL (DP18), 20 Pin Shrunk Miniature DIL SSOP (NP20) and 14 Pin DIL (DP14) packages

DP14 Pin	DP18 Pin	NP20 Pin	Name	Function
1	1	1	V_{DD}	10V power supply input to all circuits except Gate Driver
-	2	2	OPOUT	Uncommitted op-amp output
2	3	3	BGROUT	1.28V reference decoupling point for bandgap circuit
3	4	4	C_F	Control loop filter capacitor. Provides facility to filter high frequency PWM from current demand signal
4	5	5	C_{ERROUT}	Error amplifier output. Used to connect low-pass filter capacitor
5	6	6	C_{ERRIN}	Error amplifier input. Used to connect low-pass filter capacitor
6	7	7	$V_{OUTSENSE}$	Output voltage sense input. Monitors dc output voltage for fluctuations
7	8	8	$PWRV_{DD}$	10V power supply to Gate Driver circuit
8	9	9	GATE	Direct MOSFET drive signal
-	-	10	N.C.	Not connected
-	-	11	N.C.	Not connected
9	10	12	$PWRV_{SS}$	0V power supply to Gate Driver circuit
9	11	13	V_{SS}	0V power supply to all circuits except Gate Driver
10	12	14	SHUTDOWN	Logic input- shuts down Gate Driver current sources when high
11	13	15	V_{ISENSE}	Boost regulator current sense input - measures Boost-mode current across in-line resistor
-	14	16	OPIN+	Uncommitted op-amp non-inverting input
12	15	17	$V_{INSENSE}$	Input voltage sense input- monitors bridge rectifier output to give tracking signal
-	16	18	OPIN-	Uncommitted op-amp inverting input
13	17	19	C_{EXT}	External capacitor- defines PWM oscillator frequency
14	18	20	R_B	External bias resistor. Used to define on-chip reference currents

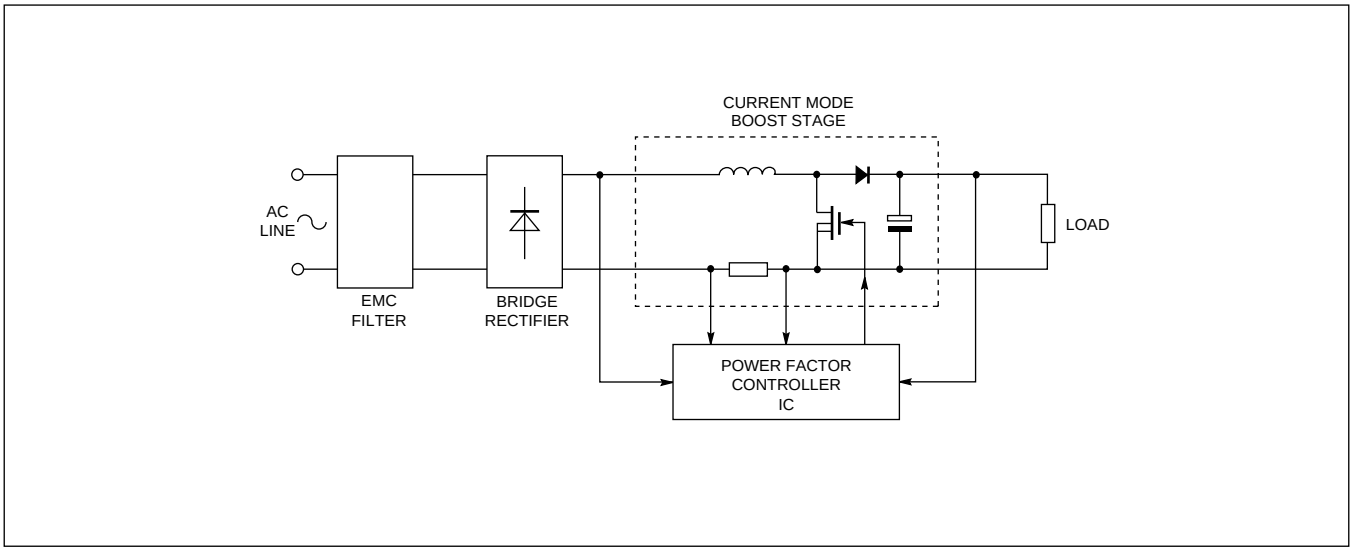


Fig.2 Functional diagram

The MSC60028 uses the Current-Mode Boost method of regulation. This can be set to have a continuous input current characteristic which minimises the level of high frequency filtering required on the line input.

The device monitors both the rectified incoming line voltage and the regulated dc output voltage from which it calculates a current 'demand' signal. This is then compared to a feedback signal representing the input current (derived by a low value in-line resistor) to modify the PWM signal fed to the MOSFET and so maintain the dc output voltage constant.

Since the current demand signal is a function of the rectified line voltage, it forces the MOSFET duty cycle, and therefore the average current, to track the line voltage wave shape. Consequently, the line current and voltage are in phase and the load appears to be resistive to the line distribution network.

When the MOSFET is turned on, the current in the inductor increases and flows back through the low value current sensing resistor. The load current is supplied by the reservoir capacitor during this time since the diode is reverse biased.

When the current demand and current feedback signals reach equilibrium, the MOSFET is turned off. The inductor current then decays by flowing into the reservoir capacitor, thus replenishing its charge in readiness for the next cycle.

The Current-Mode Boost circuit produces dc voltages in excess of the input line voltage. This fact may be exploited to allow international operation across a wide range of line voltages- typically 80V to 270V 50Hz/60Hz without selector switches.

The MSC60028 benefits from comprehensive protection circuitry to ensure reliable operation and extend the life of external components.

During power-up the supply voltage is monitored to ensure that all the circuit elements are operational before enabling the Gate Driver stage. Similarly, during power-down (or if an unacceptably large glitch or sag occurs on the line voltage) the output stage will be turned off if V_{DD} drops below 7V.

To prevent voltage runaway, a high speed comparator continuously monitors the output voltage and shuts down the Gate Driver stage should its value rise 6% above nominal.

When used in fluorescent light ballasts, this system brings about flicker free operation together with reduction of bulk and an increase in lamp efficiency. All applications benefit from improved power factor, current form factor and reduced stress on components.

The opportunity to meet existing and forthcoming legislation covering line current harmonics is also a significant advantage.

FUNCTIONAL BLOCKS

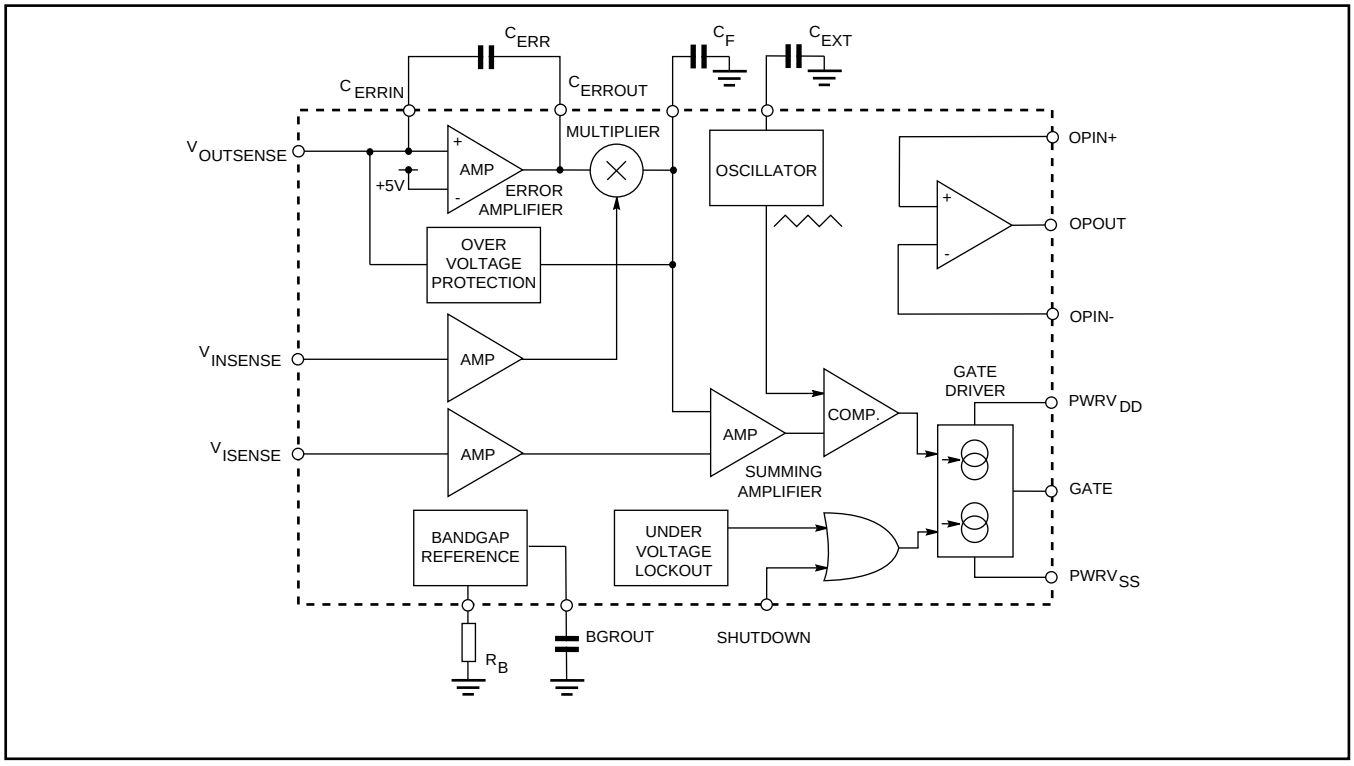


Fig.3 Block diagram

Error Amplifier

The error amplifier compares a reduced-amplitude representation of the dc output voltage to a precision, factory-trimmed 5V reference signal. The loop gain is nomionally -150 at dc and the amplifier is single-ended.

A voltage divider must be placed on the input in order to divide the high-tension rail down to nominally 5V. This must be done with some accuracy in order not to introduce offset errors. It is therefore recommended that 1% resistors be used.

This amplifier stage should have a capacitor tied between its input and output (C_{ERRIN} and C_{ERROUT}) to form a low pass filter. This has the effect of rolling off the gain with increasing frequency in order to reduce the effect of ripple voltage which may be superimposed on the feedback signal. Typically, the pole should be at a frequency of a few Hertz so that the attenuation at 50/60Hz is maximised. However, the pole must not be placed so close to zero that it forms an integrator.

A 220kΩ resistor is included at the input to the error amplifier, giving a pole at:

$$f = \frac{1}{2\pi RC\,|A|}$$

where $R = 220k\Omega$

$|A| = 150$

Beyond this the gain rolls off at -6dB/octave.

Note that a capacitance of at least 500pF is necessary in order that the multiplier circuit will function correctly.

Multiplier

This block multiplies the conditioned error signal by a reduced-amplitude representation of the bridge rectified line input (via $V_{INSENSE}$). A PWM technique is used to perform the multiplication as a result of which a capacitor, C_F, is required to reduce the carrier frequency component.

C_F, in conjunction with the output impedance of the multiplier forms a low pass filter with a -3dB point of:

$$f = \frac{1}{2\pi R_O C_F}$$

where R_O = output resistance of multiplier.

The pole must be placed so that no appreciable attenuation occurs at 100Hz but the PWM frequency is well filtered. A point a little above 120Hz will suffice for both 50Hz and 60Hz supplies (since the bridge rectified voltage signal has a frequency at twice the supply frequency).

A voltage divider must be placed on the $V_{INSENSE}$ input in order to divide the high-tension rail down to nominally 5V. This must be done with some accuracy in order not to introduce offset errors. It is therefore recommended that 1% resistors be used.

Summing Amplifier

This amplifier provides the current feedback to the boost stage by measuring the voltage across an in-line resistor, one side of which is connected to the signal ground.

It is most important that the ground point of this resistor is adjacent to the MOSFET and the measurement point is adjacent to the bridge rectifier and that the current path is as short as possible.

The current demand and current feedback signals are compared and used to modify the PWM duty signal in order to maintain equilibrium.

Gate Driver

The output buffer provides a constant current drive of 150mA -0/+50% to ensure fast, linear charging of the MOSFET gate capacitance. The output current is constant until the voltage rises to within 2V of the supply rail. The current then reduces to 45mA ±33%.

To prevent the MOSFET from operating in the linear region, an Under-Voltage Lockout circuit is employed. During power-up the Gate Driver is held off until V_{DD} reaches 8V ±3%. An internal 100kΩ resistor between GATE and $PWRV_{SS}$ prevents the MOSFET gate from floating during this time.

Similarly, during power-down or large supply glitches/sags, the Under-Voltage Lockout circuit monitors the supply voltage and disables the Gate Driver at 7V ±3%. Again, the internal 100kΩ resistor prevents the MOSFET gate from floating.

The SHUTDOWN pin requires a logic input with low-level and high-level input thresholds of 0.8V (max.) and 3.37V (min.) respectively- enabling it to be used with standard 5V logic signals. This pin is active high and functions to disable the Gate Driver current sources. An internal 100kΩ resistor on the SHUTDOWN pin means that no external components are required if this input is unused. Typically, SHUTDOWN will be used in conjunction with a watchdog or over-current detector or to provide a sleep mode.

Oscillator

This circuit uses a single external capacitor C_{EXT} to define the PWM frequency f_{PWM}. The oscillator produces a triangular waveform with peak to peak amplitude of 2.35V ±4% offset by 2.52V ±4%. To set the PWM frequency the value of C_{EXT} can be read directly from Fig.4 or calculated from: exp (4-loge f_{PWM}) where f_{PWM} is the operating frequency in kHz and C_{EXT} is the timing capacitance in nF.

If required, the triangle waveform on the C_{EXT} pin may be buffered and used externally. Alternatively, the capacitor may be removed completely and the C_{EXT} pin driven from a low impedance source. (The gain stage between the C_{EXT} pin, and the triangle waveform used internally has unity gain).

R_B sets the capacitor charging currents. Its value should be 200kΩ ±1%.

Overvoltage Monitoring

This comparator is incorporated to eliminate the possibility of excessive rises in output voltage which may occur during power up or sudden load changes. It is required since the error amplifier has a bandwidth limited response.

Should the voltage on the $V_{OUTSENSE}$ terminal exceed the preset voltage of 5.36V the PWM switching is disabled immediately. The hysteresis associated with this input is typically 120mV. Therefore the gate output will not be re-enabled until the voltage on $V_{OUTSENSE}$ is reduced to nominally 5.24V.

It is therefore most important that the reservoir capacitor is large enough so that the overvoltage threshold voltage is not exceeded. In fact the ripple must be less than 0.6V pk-pk measured at the $V_{OUTSENSE}$ input. This is equivalent to 14% of the nominal voltage (or 55V pk-pk superimposed on a 390V dc rail).

Uncommitted Op-Amp

Access to all three pins of this op-amp ensures flexibility. Typically this amplifier may be used for over-current protection, lamp dimmer controls or soft starting. It is not available on the 14 pin package variants.

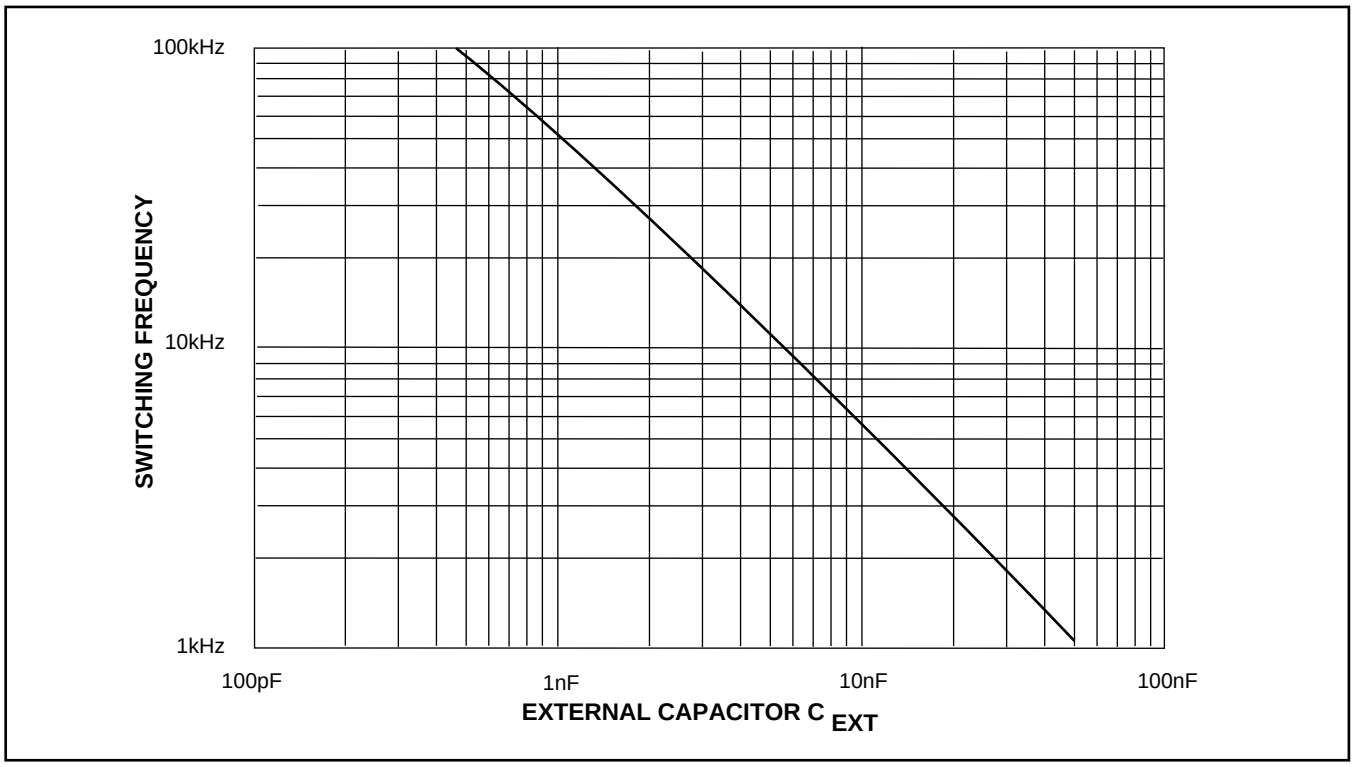


Fig.4 Graph of capacitance C_{EXT} versus switching frequency

APPLICATIONS

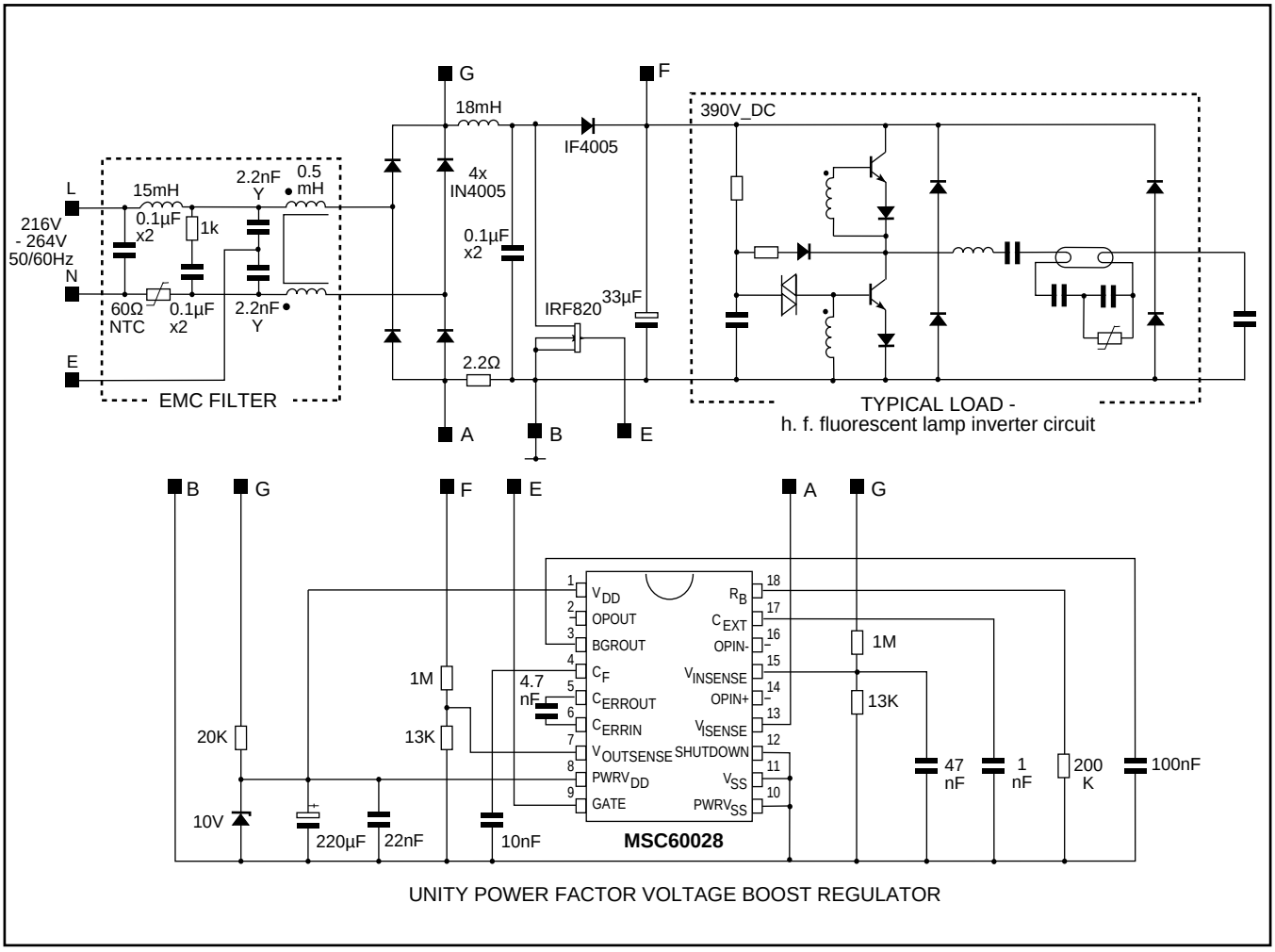


Fig.5 Typical application

Fig.5 shows a typical power factor correction circuit being used to drive a high-frequency fluorescent lamp ballast. Relatively few discrete components are required to produce a fully functional system. This circuit is suitable for loads in the 20W-100W region. Higher powers may be catered for by adding an inrush reducing circuit to ensure that excessive currents do not flow into the capacitor at power-up.

Measured input current harmonics are given in Table 1 based on power levels of 20W to 50W and a voltage of 240V 50Hz. Also given are the maximum allowable harmonic components for the IEC555-2 (Mod 2 Amd 2) specifications.

Fundamental current (A)	Harmonic Component as % of Fundamental							THD	Input Power
	2nd	3rd	5th	7th	9th	11th	13th		
0.11	0.2	4.2	4.2	3.8	0.4	0.7	2.1	7.4	27.5
0.13	0.2	3.3	3.0	3.1	0.6	0.7	1.7	5.8	31.9
0.19	0.1	3.6	1.6	2.8	1.1	0.9	1.6	5.3	44.7
0.24	0.2	1.7	1.0	3.6	0.8	1.2	2.1	4.8	57.4
IEC555-2	5	30x PF	7	4	3	2			

Resistor Values

In order to ensure accurate operation, it is recommended that 1% resistors are used to divide the high-tension signals down to lower potentials. To prevent excessive voltages from being impressed on the MSC60028 in the event of a resistor failure, the network shown in Fig.6 is recommended. With this network, a short circuit or open circuit on any one resistor cannot impress a voltage of more than twice the intended value on the IC.

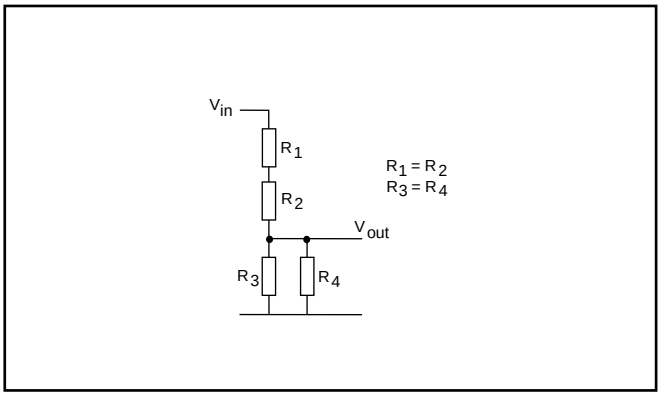


Fig.6 Resistor divider network

DESIGN CONSIDERATIONS

Input Protection

All input terminals except V_{ISENSE} are protected by means of clamping diodes to V_{SS} and V_{DD}.

Because the signal received at V_{ISENSE} goes negative with respect to signal ground, clamping diodes cannot be used for protection. The V_{ISENSE} input is protected by a transistor which breaks down at -12V and exceeding this voltage will permanently damage the device.

Inrush Current Protection

At turn-on of the mains supply the power factor correction circuit has an uncharged reservoir capacitor and a large current pulse is drawn from the supply during the mains cycle. A peak inrush current of the order of 20 to 50A may flow. Such current would cause excessive voltage to appear across the current sense resistor and damage to both the power factor corrector and the resistor would occur.

Two simple solutions for overcoming inrush currents use an NTC thermistor or a diode. A diode in parallel with the current sense resistor (Fig.6a) allows full inrush current to flow but protects the circuit by the clamping action of the diode. If voltages exceeding 0.7V may appear across the current sense resistor in normal operation two diodes may be connected in series. Rectifier diodes can be used for this protection and should be sized on pulsed current ratings.

A second solution using an NTC thermistor connected in series with the neutral supply line (Fig.6b) will reduce the inrush current. There are two problems associated with using NTC thermistors in this approach. An NTC has a resistance that falls exponentially with temperature and will run hot when the circuit is in normal operation. If the circuit is turned off and on before the NTC has time to cool down large inrush currents will result.

Another solution is to use a fixed resistor, bridged by a thyristor, in series with the positive supply line, between the bridge rectifier output and all other circuitry (Fig.6c). The thyristor must receive gate pulses, via an isolating pulse transformer, from the boost converter drive stage. Inrush current at turn-on is then limited by the resistor which is short-circuited by the thyristor when the boost converter starts. Power losses are low and in addition the problem of NTC cooling time is overcome.

AUXILIARY POWER SUPPLY

The circuit in Fig.5 shows the most cost-effective method for generating a 10V supply via a dropper resistor from the rectified line. The resistor feeds a reservoir capacitor and voltage reference diode clamp. This method is less suitable for applications with large variations in line voltage because the dropper resistor must be sized to provide at least 10mA from the lowest line voltage. Excessive power loss at higher line voltages may then occur. Other methods of generating the auxiliary supply are possible but are not so cost effective. Fig.7 shows two methods which use the boost inductor to generate an auxiliary supply. Both methods use a large value resistor R1, from the rectified line to charge a starting capacitor which then supplies the current required to start up the circuit. After the circuit has started the auxiliary power supply takes over.

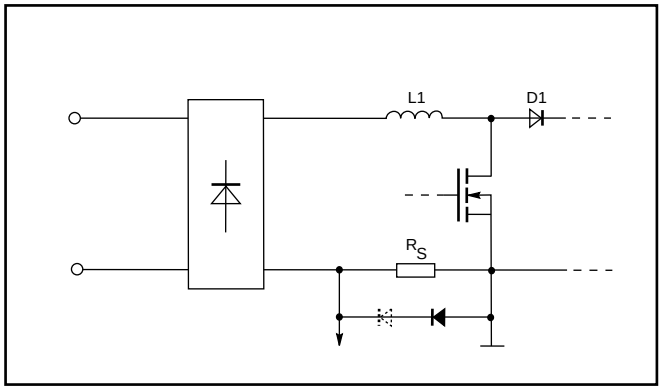


Fig.6a Diode clamping inrush protection

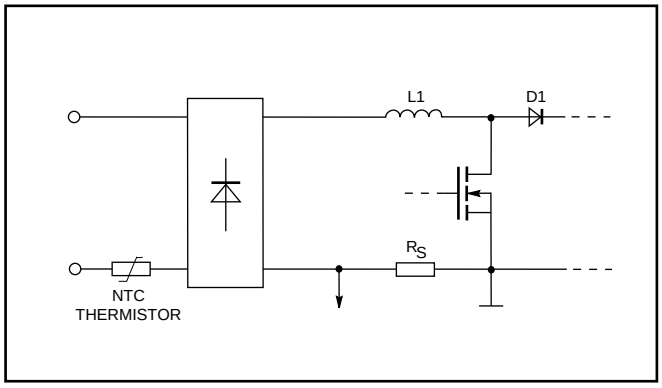


Fig.6b Thermistor inrush current protection

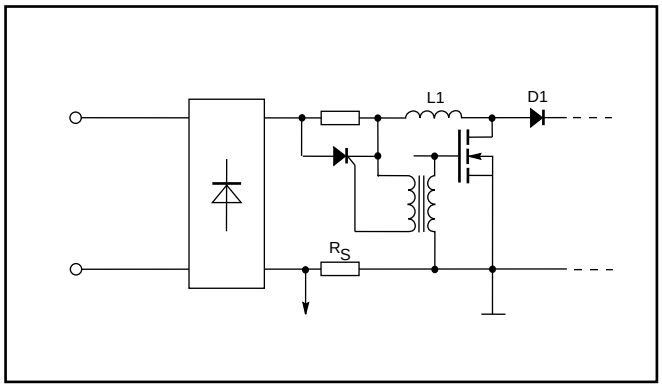


Fig.6c Thyristor inrush current protection

Fig.7a uses an auxiliary winding on the boost inductor L1 which delivers a voltage proportional to the dc output voltage given by:

$$\frac{N_P}{N_S} = \frac{V_{DC}}{10}$$

where N_P = Number of turns on boost inductor

N_S = Number of turns on auxiliary winding

V_{DC} = Boost stage output voltage

The charge pump shown in Fig.7b eliminates the need for an auxiliary winding on boost inductor. This circuit uses charge transfer to generate a constant current which feeds the voltage reference diode Dz. This current is given by:

$$I_Z = (V_{DC} - 10)\, f_{PWM}\, C1$$

where V_{DC} = Boost stage output voltage

f_{PWM} = PWM frequency

The undervoltage lockout circuit has 1 volt hysteresis which means the starting capacitor has to be large enough so the voltage does not fall by more than 1 volt during start-up. The size of the capacitor can be reduced by using the uncommitted op-amp to increase the UVL upper threshold, as shown in Fig.8a.

POWER COMPONENT SELECTION

Current Sense Resistor

The current sense resistor should be chosen to give a peak voltage of 0.3V under minimum load conditions. Peak voltages below this value will degrade the line current waveform drawn by the circuit.

Boost Inductor

The value of the boost inductor determines the amount of hf. ripple current at the input. The value of inductance selected for an application is a 'trade-off' between core size and input rfi filtering requirements. Inductor design starts with the peak current I_P the inductor will carry and this occurs at the peak of the minimum rms working line voltage V_{inmin} at maximum output power P_{outmax} and is given by:

$$I_P = \frac{\sqrt{2} \times P_{outmax}}{V_{inmin}}$$

The maximum value of hf ripple current occurs in a boost converter when the switching duty cycle is 50%. The peak inductor current does not generally occur at this point because the inductor current follows the incoming mains voltage. The peak-to-peak ripple current Δi_L in the inductor is normally chosen so that the boost circuit operates in continuous-mode for most of the mains half cycle. The peak-to-peak ripple current Δi_L is normally chosen between 10% and 30% of the maximum RMS line current. The converter then operates in the continuous-mode for a large fraction of each supply half-cycle. Large ripple currents however, require input filters with higher attenuation. To find the value of the inductor the duty cycle δ_{max} for minimum line voltage is calculated from:

$$\delta_{max} = \frac{V_{out} - V_{inmin}}{V_{out}}$$

and the inductance L is calculated from:

$$L = \frac{V_{inmin} \times \delta_{max}}{f_{PWM} \times \Delta I_L}$$

where f_{PWM} is the switching frequency.

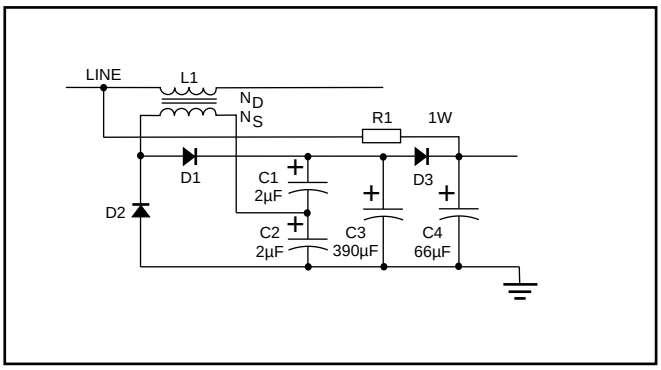


Fig.7a Auxiliary power supply using a tap on boost inductor

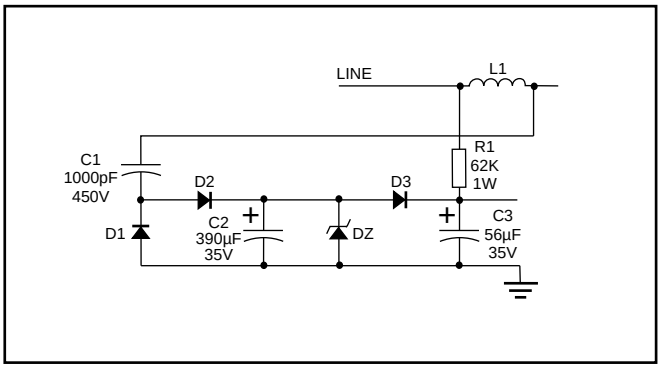


Fig.7b Auxiliary power supply using a charge pump

The hf ripple current is superimposed on the rectified line current and to determine the peak inductor current I_{Lpk} the peak value of ripple current is added to the peak line current. To avoid saturating the inductor the value of current used for calculation should be about 10% to 20% greater than the I_{Lpk}.

The required energy storage of the inductor is given by:

$$\frac{LI^2_{Lpk}}{2}$$

The energy storage of a gapped ferrite core set is determined by the gap width used. The equations below assume that a gapped ferrite core is used and that the reluctance of the air gap is much greater than the reluctance of the core material. The number of turns, N, required is determined from:

$$N = \frac{I_{Lpk} \times L}{B_{max} \times A_e}$$

where B_{max} is the maximum flux density in Tesla of the core before saturation, and A_e is the effective cross sectional area of the core.

The required air gap l_{gap} is given by:

$$l_{gap} = \frac{4\pi \times 10^{-4} \times A_e \times N^2}{L} \text{[mm]}$$

Optimum inductor design can be performed using manufacturers data. The wire used for the winding should be selected to operate at current densities of 5A to 10A per mm^2.

Power Semiconductor Selection

Peak voltages and currents must be known for all operating conditions so that the correct switch and boost diode can be selected. It is usual practice to derate the semiconductors to about 75% of their maximum ratings. For a 390V dc link this implies the use of parts with a voltage rating of about 500V.

Power Switch

The switch can be either a bipolar transistor, an IGBT or a MOSFET. The choice would depend on the switching frequency used. For switching frequencies below about 20kHz a bipolar transistor may be used but for higher frequency operation an IGBT or MOSFET switch is necessary.

The current derating of the switch should be based on the peak inductor current.

The main losses in the switch are the on-state and switching loss. When a switch has been selected the power losses should be estimated to determine the level of heat sinking required. The manufacturers data sheet will provide curves of maximum case temperature versus current.

Suitable IGBTs can be supplied by GEC Plessey Semiconductors - please contact your local Sales Office or Distributor. Popular MOSFETs for use in low power circuits are IRF820, IRF830 and IRF840 which are 500V parts with current ratings of 2.5A, 4.5A and 8A respectively.

Diode Selection

The boost diode should be selected to have a reverse recovery time less than 1% of the circuit switching period. The UF series of diodes having recovery times of 50ns are suitable for use in this application.

The input rectifier requires only diodes with a 'standard recovery' rectifier characteristic. A popular choice are the1N series of diodes. It is recommended that a 100nF decoupling capacitor is connected across the output of the rectifier bridge because of the slow characteristic of the rectifier diodes.

The current derating of the diodes should be based upon the RMS value of maximum input current.

Capacitor Selection

The value of the output capacitor is determined by several application specific requirements, the switching frequency, the ripple voltage and current and the hold-up time.

The hold-up time is the time that the output voltage stays within a specific range after input supply has been removed. The capacitance required to provide a hold-up time of ΔTseconds is given by:

$$C = \frac{2 \times P_{outmax} \times \Delta T}{V^2_{outmax} - V^2_{outmin}}$$

The total current through the capacitor is a combination of supply harmonic ripple current and switching frequency ripple current. Electrolytic capacitors are normally used because of the high voltage and capacitance ratings available. These capacitors have an effective series resistor (ESR) which results in internal power dissipation. The maximum allowed ripple current is a function of the maximum working temperature of the capacitor.

Uncommitted Op-Amp

The uncommitted op-amp may be used for a variety of protection or 'added value' features such as current limit protection, waveform buffering or soft starting. Fig.8 shows some examples of these functions.

Demonstration/Evaluation Boards and Lighting Units

The MSC60028 is available on an evaluation board for customers wishing to evaluate the voltage-boost-converter power factor correction function. A high frequency fluorescent lamp unit is also available from GEC Plessey Semiconductors to allow evaluation of the MSC60028. This is a complete 28W '2D' style lamp housing containing input filters, power factor correction unit incorporating the MSC60028 and high frequency inverter/ lamp driver.

The boards and lighting units are available on short-term loan or for sale at a nominal charge.

Both 110V and 240V units are available and are shipped with a full design manual and applications notes.

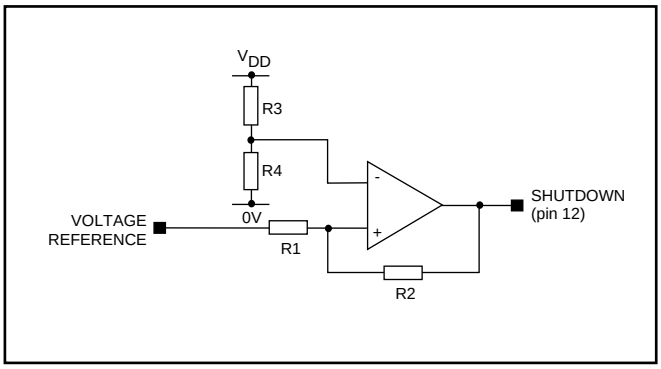


Fig.8a Increasing UVL threshold

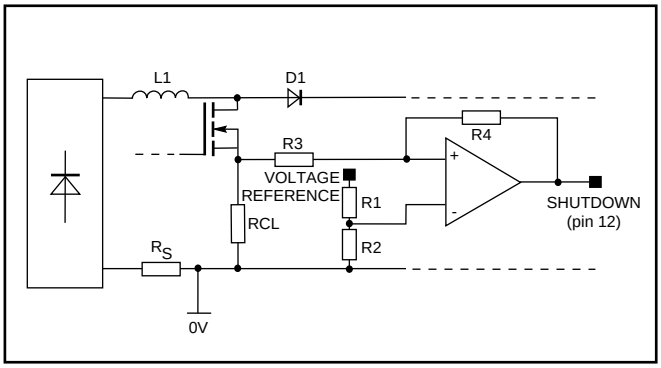


Fig.8b Current limit

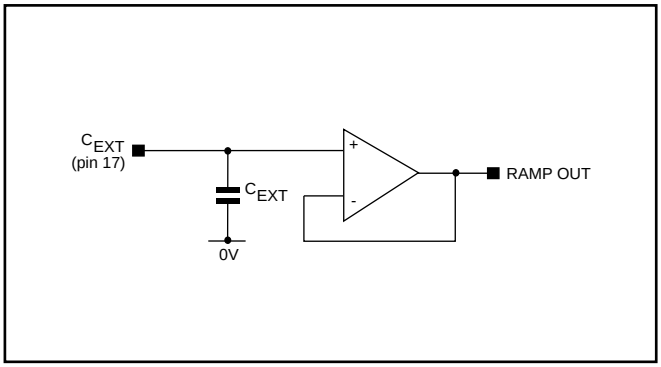


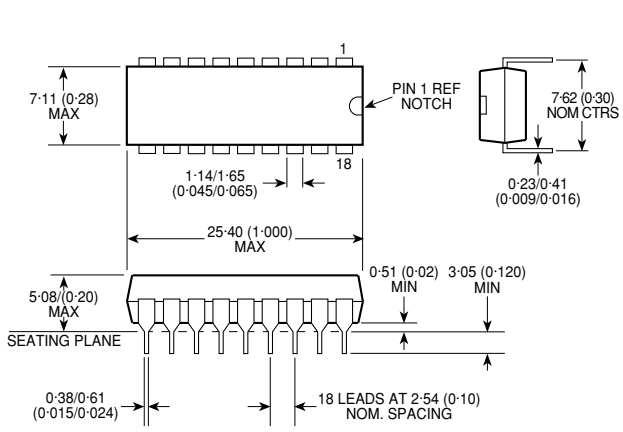
Fig.8c Timing waveform buffered for external use

NOTES

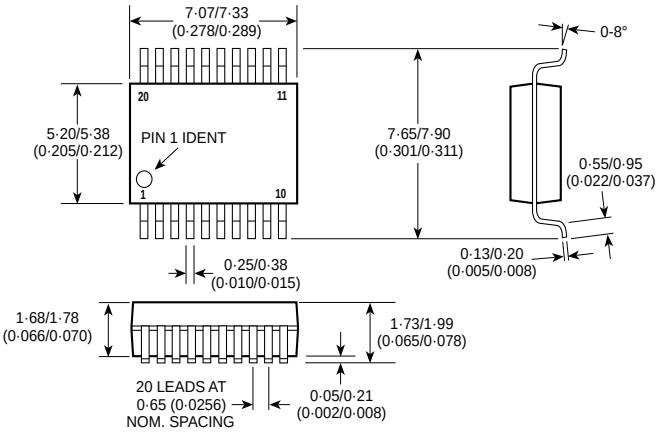
MSC60028

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.

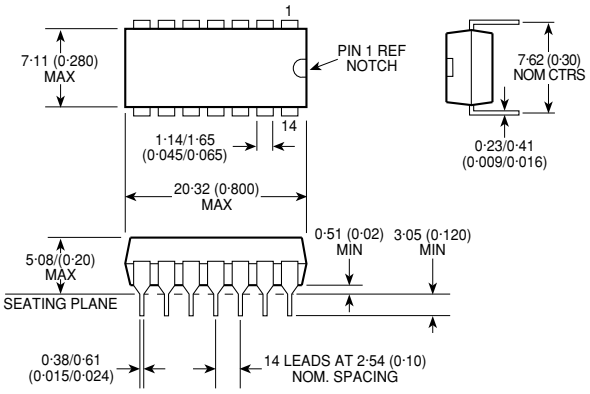


18-LEAD PLASTIC DIL – DP18



20-LEAD SHRUNK MINIATURE PLASTIC DIL (SSOP) - NP20

NOTES
1. Controlling dimensions are inches.
2. These package outline diagrams are for guidance only. Please contact your GPS Customer Service Centre for further information.



14-LEAD PLASTIC DIL – DP14

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