The MRFIC Line

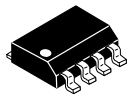
900 MHz Downconverter (LNA/Mixer)

MRFIC2001

900 MHz DOWNCONVERTER LNA/MIXER SILICON MONOLITHIC INTEGRATED CIRCUIT

The MRFIC2001 is an integrated downconverter designed for receivers operating in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2001 include CT-1 and CT-2 cordless telephones, remote controls, video and audio short range links, low cost cellular radios, and ISM band receivers. A power down control is provided to minimize current drain with minimum recovery/turn-on time.

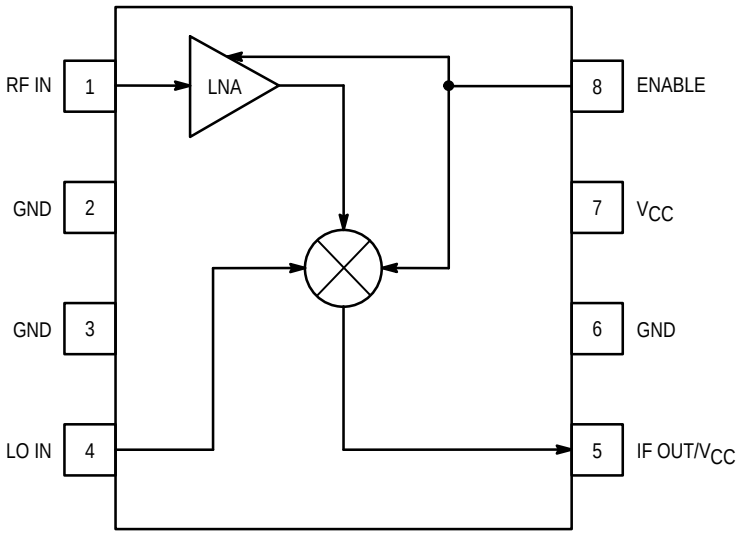
- Conversion Gain = 23 dB (Typ)
- Supply Current = 4.7 mA (Typ)
- Power Down Supply Current = 2.0 μA (Max)
- Low LO Drive = –10 dBm (Typ)
- LO Impedance Insensitive to Power Down
- No Image Filtering Required
- No Matching Required for RF IN Port
- All Ports are Single Ended
- Available in Tape and Reel by Adding R2 Suffix to Part Number. R2 suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2001



CASE 751-05 (SO-8)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.5	Vdc
Control Voltage	ENABLE	5.0	Vdc
Input Power, RF and LO Ports	P_{RF}, P_{LO}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C



Pin Connections and Functional Block Diagram

MOTOROLA

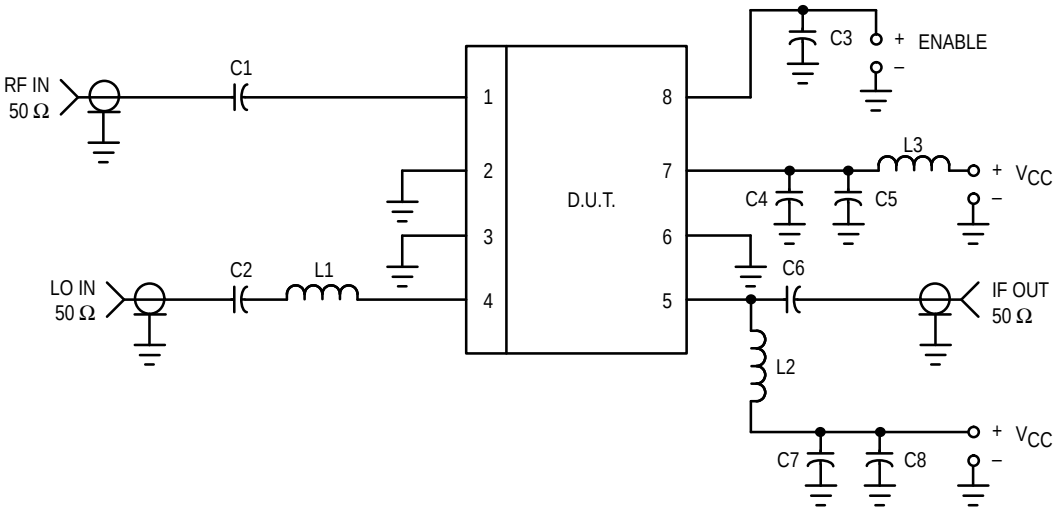
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	2.7 to 5.0	Vdc
Control Voltage Range	ENABLE	0 to 5.0	Vdc
RF Port Frequency Range	f_{RF}	500 to 1000	MHz
IF Port Frequency Range	f_{IF}	0 (dc) to 250	MHz

ELECTRICAL CHARACTERISTICS (V_{CC}, ENABLE = 3.0 V, T_A = 25°C, RF @ 900 MHz, LO @ 1.0 GHz, P_{LO} = –7.0 dBm, IF @ 100 MHz unless otherwise noted)

Characteristic (1)	Min	Typ	Max	Unit
Supply Current: On-Mode	—	4.7	5.5	mA
Supply Current: Off-Mode (ENABLE < 1.0 Volts)	—	0.1	2.0	μA
ENABLE Response Time	—	1.0	—	μs
Conversion Gain	20	23	26	dB
Input Return Loss (RF IN Port)	—	13	—	dB
Single Sideband Noise Figure	—	5.5	—	dB
Input 3rd Order Intercept Point	– 26	– 22.5	—	dBm
Output Power at 1.0 dB Gain Compression	—	–10	—	dBm
LO – RF Isolation (1.0 GHz)	—	37	—	dB
LO – IF Isolation (1.0 GHz)	—	33	—	dB
RF – IF Isolation (900 MHz)	—	4.0	—	dB
RF – LO Isolation (900 MHz)	—	19	—	dB

NOTE:
1. All Electrical Characteristics measured in test circuit schematic shown in Figure 1 below:



C1, C2, C4, C7 — 100 pF Chip Capacitor
C3, C5, C8 — 1000 pF Chip Capacitor
C6 — 6.8 pF Chip Capacitor
L1 — 8.2 nH Chip Inductor
L2 — 270 nH Chip Inductor
L3 — 150 nH Chip Inductor
RF Connectors — SMA Type
Board Material — 0.025″ Thick Duroid, 0.062″ Copper Clad, 0.5 oz. Copper, ϵ_r = 10.2

Figure 1. Test Circuit Configuration

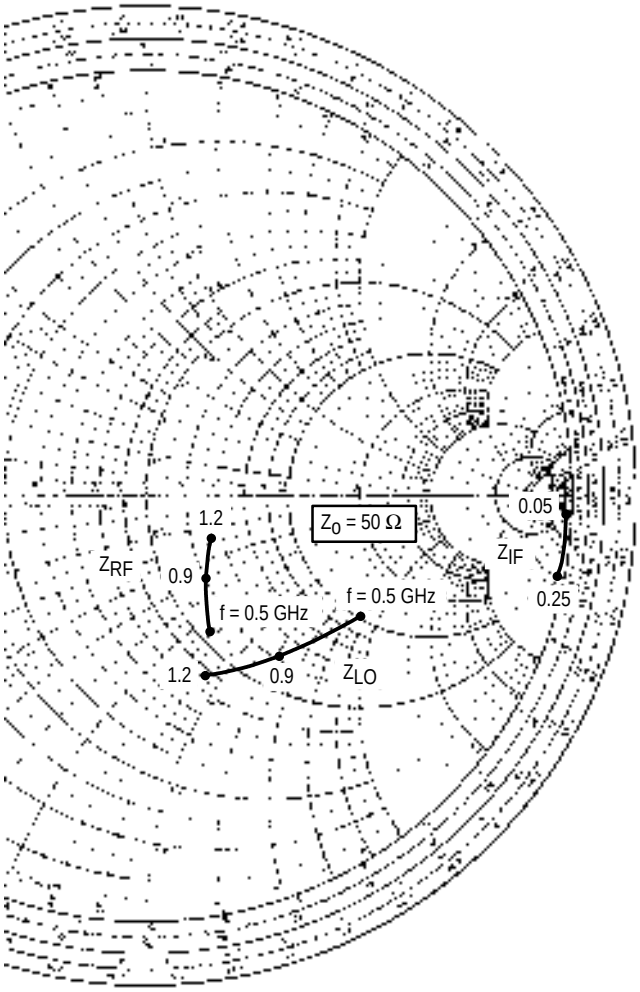


Figure 2. Port Impedances versus Frequency (GHz)

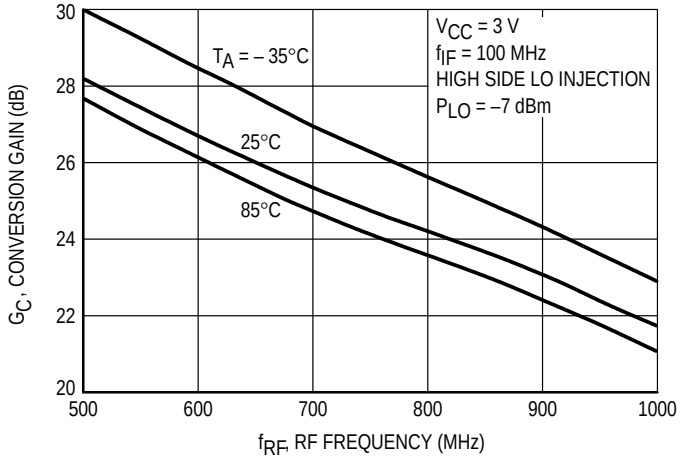


Figure 3. Conversion Gain versus RF Frequency

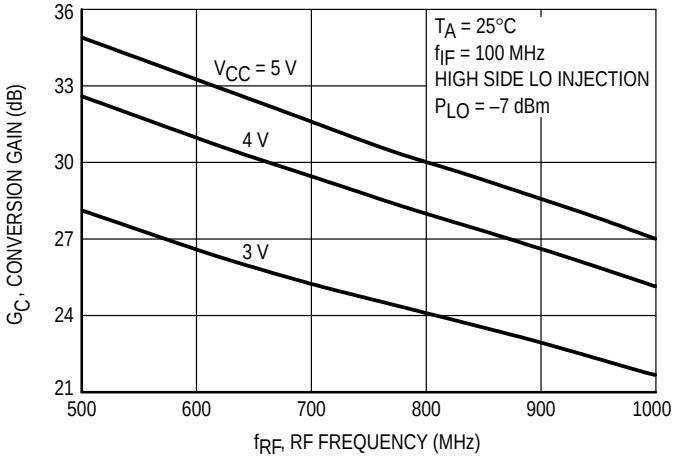


Figure 4. Conversion Gain versus RF Frequency

V_{CC} (Volts)	f (MHz)	Γ_{IF}		Γ_{RF}		Γ_{LO}	
		Mag	∠ϕ Degrees	Mag	∠ϕ Degrees	Mag	∠ϕ Degrees
3.0	50	0.998	– 2.5	—	—	—	—
	100	0.996	– 4.9	—	—	—	—
	150	0.993	– 7.2	—	—	—	—
	200	0.990	–10	—	—	—	—
	250	0.987	–12	—	—	—	—
	500	—	—	0.36	–70	0.58	– 31
	600	—	—	0.32	–70	0.55	– 36
	700	—	—	0.29	– 69	0.53	– 42
	800	—	—	0.26	– 68	0.51	– 48
	900	—	—	0.23	– 63	0.50	– 54
	1000	—	—	0.20	– 58	0.49	– 61
	1100	—	—	0.18	– 51	0.47	– 68
	1200	—	—	0.17	– 44	0.45	– 76

Table 1. Port Reflection Coefficients
(ENABLE = 3.0 V, Z_O = 50 Ω, T_A = 25°C)

TYPICAL CHARACTERISTICS

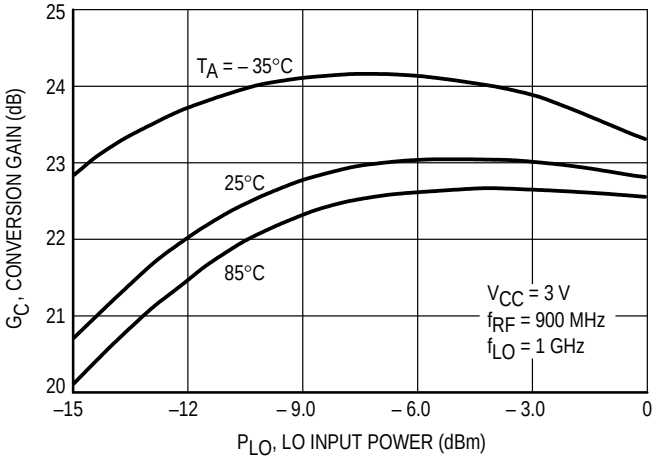


Figure 5. Conversion Gain versus LO Input Power

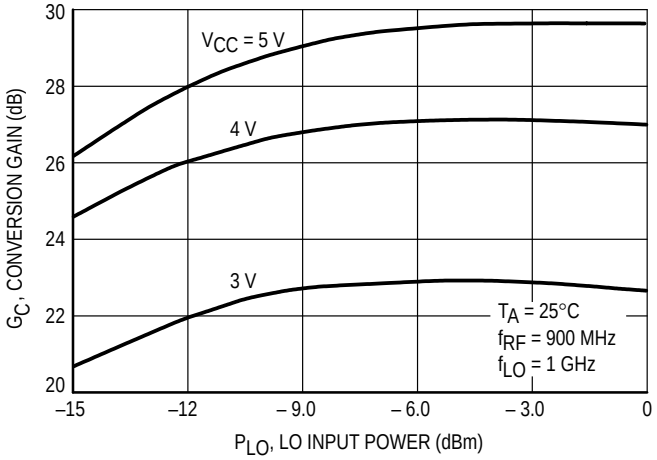


Figure 6. Conversion Gain versus LO Input Power

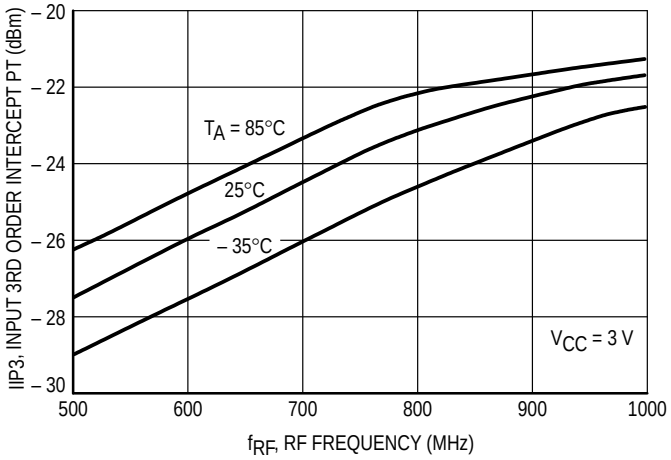


Figure 7. Input Third Order Intercept Point versus RF Frequency

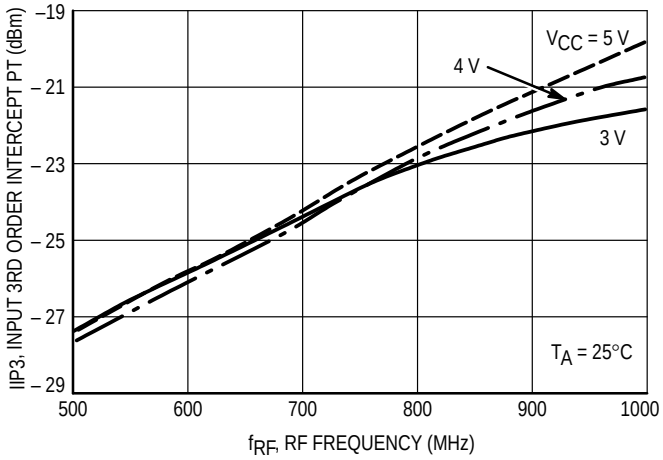


Figure 8. Input Third Order Intercept Point versus RF Frequency

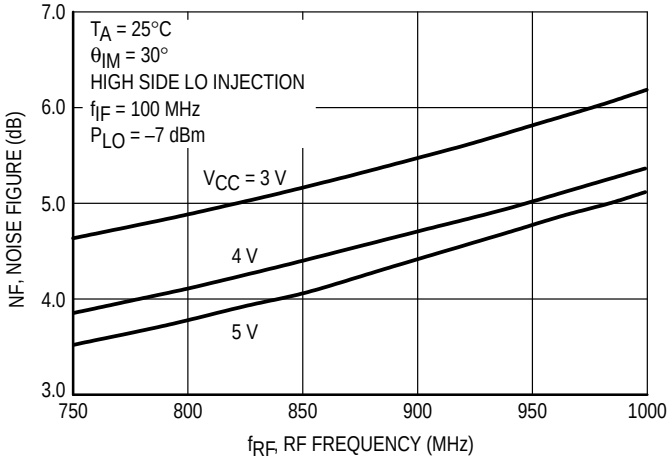


Figure 9. Noise Figure versus RF Frequency

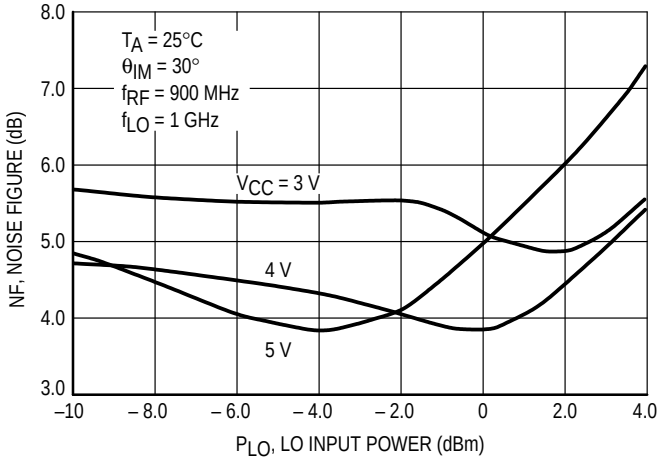


Figure 10. Noise Figure versus LO Input Power

TYPICAL CHARACTERISTICS

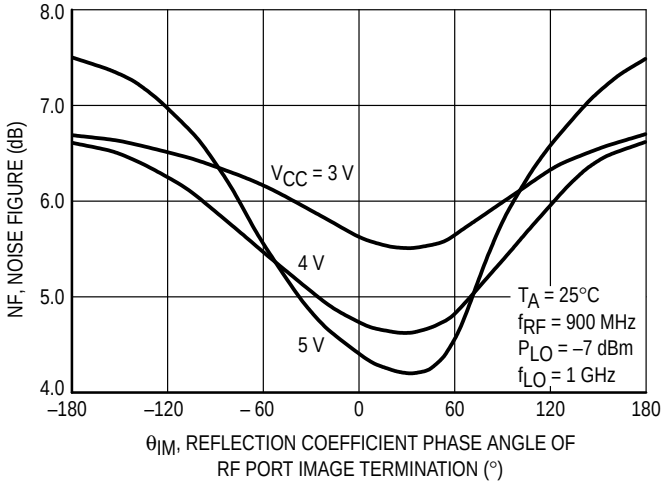


Figure 11. Noise Figure versus Reflection Coefficient Phase Angle of RF Port Image Termination

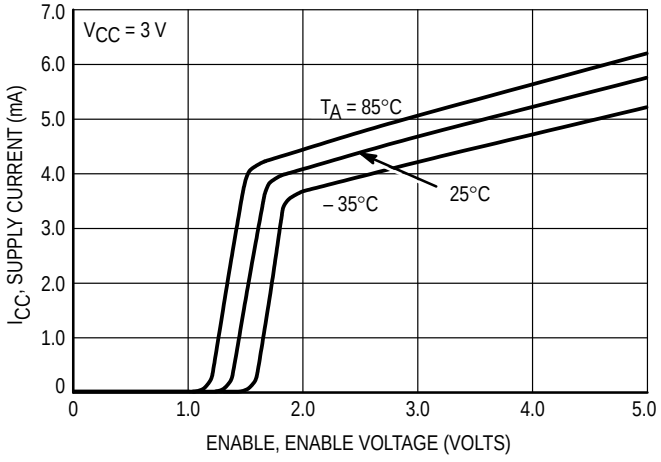


Figure 12. Supply Current versus Enable Voltage

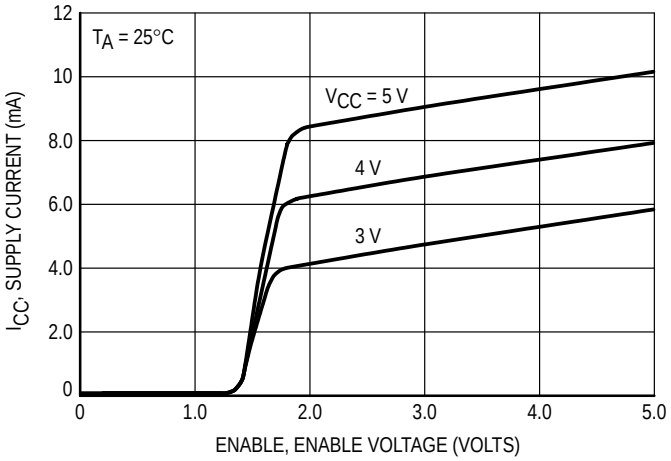


Figure 13. Supply Current versus Enable Voltage

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2001 was designed for low cost, small size, and ease of use. This is accomplished by minimizing the number of necessary external components.

The most significant external component eliminated was an image filter between the LNA and mixer. It was found the ensuing image noise entering the mixer from the LNA could be minimized by optimizing the LNA input termination at the image frequency. Also, a double-balanced mixer was used to reject the IF noise from the LNA. This results in excellent LO and spurious rejection.

To eliminate the need for external baluns or decoupling elements, the unused LO and RF ports of the mixer are decoupled internally. Only one of the IF outputs is used, eliminating the need for an external balun on the IF port as well. Also, the LNA input is matched to 50 ohms internally. External matching is required for the LO and IF ports.

To minimize current drain in various TDD/TDMA systems, the MRFIC2001 has a TTL/CMOS compatible enable pin.

THEORY OF OPERATION

Optimizing the LNA input termination to minimize image noise is quite simple. The optimum LNA input (RF IN pin) termination is $1\angle 30°$ at the image frequency (regardless of what the image frequency is). A reflection coefficient magnitude close to 1 is automatically obtained from a front-end filter, since the image frequency would be in the stop-band. The 30° phase angle can be obtained by rotating the phase angle of the front-end filter with a series 50 ohm transmission line. The dependance of single-sideband noise figure on the image phase angle is shown in Figure 11. As the plot indicates, there is a little over 1.0 dB of variation across all possible phase angles for a 3.0 V supply. Therefore, setting the phase angle is not critical. At higher supply voltages setting the phase angle is more critical (and more rewarding).

Matching the LO port to 50 ohms can be done several ways. The recommended approach is a series inductor as close to the IC as possible. The inductor value is small enough (~8–15 nH depending on LO frequency) to be printed on the board. A DC block is required and should not be placed between the inductor and IC since this will prevent the inductor from being close enough to the IC to provide a good match.

The IF port is an open collector resulting in a very high output impedance. For optimum linearity (IP3), the IF port should be loaded with a 1000 ohm load-line. Since the output requires a bias inductor and blocking capacitor, the IF filter impedance can be transformed to 1000 ohms with these two elements. If a low output VSWR is desired (to reduce IF filter ripple), a 2.0–4.0 K ohm resistor can be placed in parallel with the bias inductor. This will reduce the conversion gain by 1.0–2.0 dB.

The RF port is nearly 55 ohms resistive in series with a small amount of capacitive reactance, which results in a 12–13 dB return loss. If a higher return loss is desired, a 3.0–4.0 nH series inductor printed on the board as close to the IC as possible will improve it to over 20 dB. A DC block is also required.

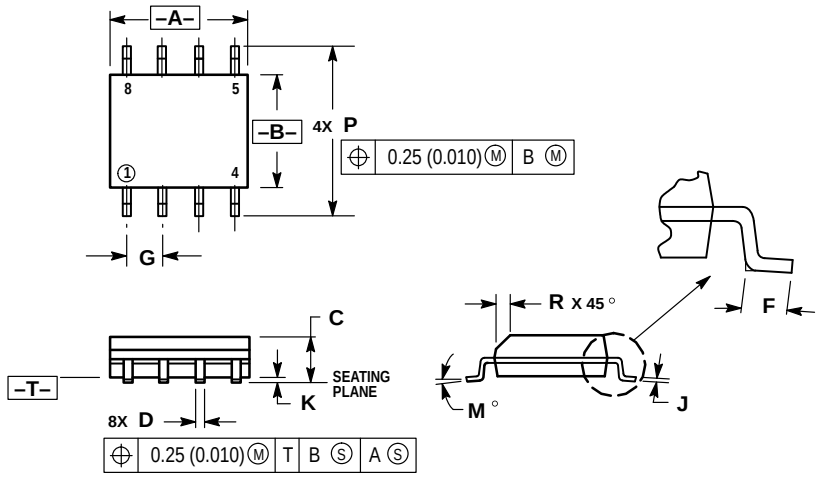
Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. An additional 100 pF capacitor and an RF choke are recommended to keep the LO signal off the supply line.

Enabling/Disabling the MRFIC2001 can be done with its TTL/CMOS compatible Enable pin. The trip point is between 1.0 and 2.0 volts.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced poduct, please contact your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751–05
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