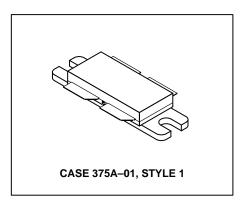
# The RF Line **NPN Silicon RF Power Transistor**

Designed for 26 Volt UHF large-signal, common emitter, Class AB linear amplifier applications in industrial and commercial FM/AM equipment operating in the range 800-960 MHz.

- Specified 26 Volt, 900 MHz Characteristics Output Power = 150 Watts (PEP) Minimum Gain = 8.0 dB @ 900 MHz, Class AB Minimum Efficiency = 35% @ 900 MHz, 150 Watts (PEP) Maximum Intermodulation Distortion −28 dBc @ 150 Watts (PEP)
- Characterized with Series Equivalent Large—Signal Parameters from 800 to 960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, and Rated Output Power
- · Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

## **MRF899**

150 W, 900 MHz **RF POWER TRANSISTOR NPN SILICON** 



#### **MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	VCEO	28	Vdc
Collector–Emitter Voltage	VCES	60	Vdc
Emitter–Base Voltage	VEBO	4.0	Vdc
Collector–Current — Continuous	IC	25	Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	PD	230 1.33	Watts W/°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C

#### THERMAL CHARACTERISTICS

Characteristic		Max	Unit
Thermal Resistance, Junction to Case		0.75	°C/W

### **ELECTRICAL CHARACTERISTICS** (To = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					•
Collector–Emitter Breakdown Voltage (I <sub>C</sub> = 100 mAdc, I <sub>B</sub> = 0)	V(BR)CEO	28	37	_	Vdc
Collector–Emitter Breakdown Voltage (I <sub>C</sub> = 50 mAdc, V <sub>BE</sub> = 0)	V(BR)CES	60	85	_	Vdc
Emitter–Base Breakdown Voltage (I <sub>E</sub> = 10 mAdc, I <sub>C</sub> = 0)	V(BR)EBO	4.0	4.9	_	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 30 Vdc, V <sub>BE</sub> = 0)	ICES	_	_	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I <sub>CE</sub> = 1.0 Adc, V <sub>CE</sub> = 5.0 Vdc)	hFE	30	75	120	_
DYNAMIC CHARACTERISTICS					
					•

Output Capacitance (V<sub>CB</sub> = 26 Vdc, I<sub>E</sub> = 0, f = 1.0 MHz) (1)  $C_{ob}$ NOTE:

1. For information only. This part is collector matched.

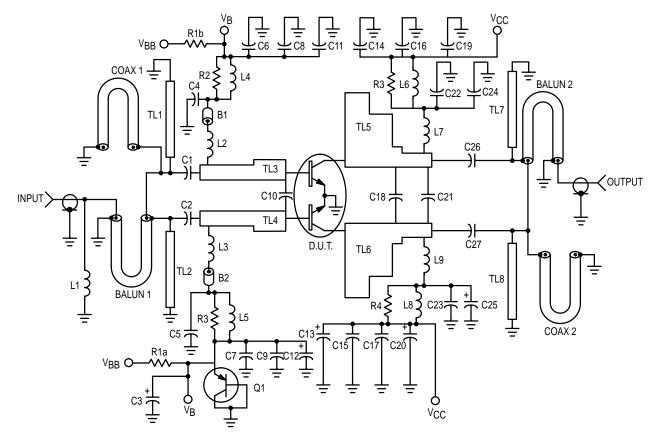
#### REV 6



(continued)

**ELECTRICAL CHARACTERISTICS** — **continued** (T<sub>C</sub> = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Amplifier Power Gain $V_{CC}$ = 26 Vdc, $P_{out}$ = 150 Watts (PEP), $I_{Cq}$ = 300 mA, $f_1$ = 900 MHz, $f_2$ = 900.1 MHz	G <sub>pe</sub>	8.0	9.0	_	dB
Collector Efficiency $V_{CC}$ = 26 Vdc, $P_{out}$ = 150 Watts (PEP), $I_{cq}$ = 300 mA, $f_1$ = 900 MHz, $f_2$ = 900.1 MHz	η	30	40	_	%
3rd Order Intermodulation Distortion $V_{CC}$ = 26 Vdc, $P_{Out}$ = 150 Watts (PEP), $I_{Cq}$ = 300 mA, $f_1$ = 900 MHz, $f_2$ = 900.1 MHz	IMD	_	-32	-28	dBc
Output Mismatch Stress $V_{CC}$ = 26 Vdc, $P_{out}$ = 150 Watts (PEP), $I_{Cq}$ = 300 mA, $f_1$ = 900 MHz, $f_2$ = 900.1 MHz, VSWR = 5:1 (all phase angles)	Ψ	No Degradation in Output Power Before and After Test			



```
B1, B2 — Ferrite Bead, Ferroxcube #56-590-65-3B
                                                                   L1 - 5 Turns 24 AWG IDIA 0.059" Choke, 19.8 nH
C1, C2, C26, C27 — 43 pF, B Case, ATC Chip Capacitor
                                                                   L2, L3, L7, L9 — 4 Turns 20 AWG IDIA 0.163" Choke
C3 - 200 \, \mu F Lytic Capacitor
                                                                   L4, L5, L6, L8 — 12 Turns 22 AWG IDIA 0.140" Choke,
C4, C5, C22, C23 — 100 pF, B Case, ATC Chip Capacitor
                                                                                   on 10-20 \Omega Resistor
C6, C7, C14, C15 — 1000 pF, B Case, ATC Chip Capacitor
                                                                   N1, N2 — Type N Flange Mount, Omni Spectra
C10 — 9.1 pF, A Case, ATC Chip Capacitor
                                                                   Q1 — Bias Transistor BD136 PNP
C13 — 500 µF Electrolytic Capacitor
                                                                   R2, R3, R4, R5 — 4.0 x 39 Ohm 1/8 W Chips in Parallel
C18 — 3.9 pF, B Case, ATC Chip Capacitor
                                                                   R1a, R1b - 56 Ohm 1.0 W
                                                                   TL1-TL8 — See Photomaster
C21 — 0.8 pF, B Case, ATC Chip Capacitor
                                                                   Balun1, Balun2, Coax 1, Coax 2 — 2.20" 50 Ohm 0.088" o.d.
C8, C9, C16, C17 — CDR32BP182AJWS, 1800 pF, AVX Chip
                                                                                                    semi-rigid coax
                    Capacitor
C11, C12, C19, C20, C24, C25 — 10 µF, Electrolytic Capacitor
                                                                   Board — 1/32" Glass Teflon, \varepsilon_r = 2.55" Arlon (GX-0300-55-22)
                                Panasonic
```

Figure 1. 900 MHz Power Gain Test Circuit

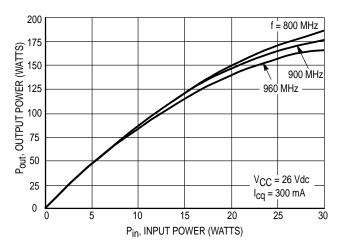


Figure 2. Output Power versus Input Power

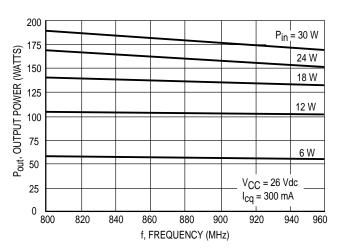


Figure 3. Output Power versus Frequency

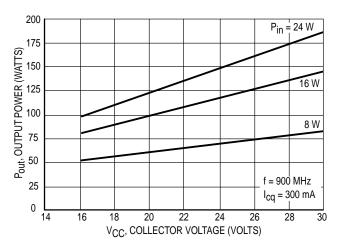


Figure 4. Output Power versus Supply Voltage

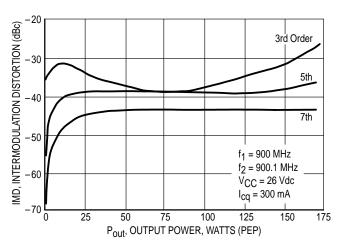


Figure 5. Intermodulation versus Output Power

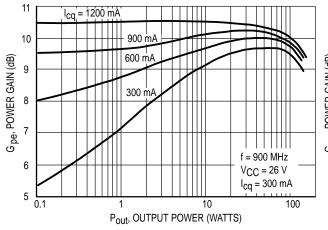


Figure 6. Power Gain versus Output Power

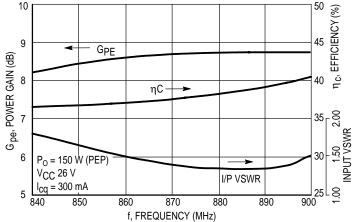
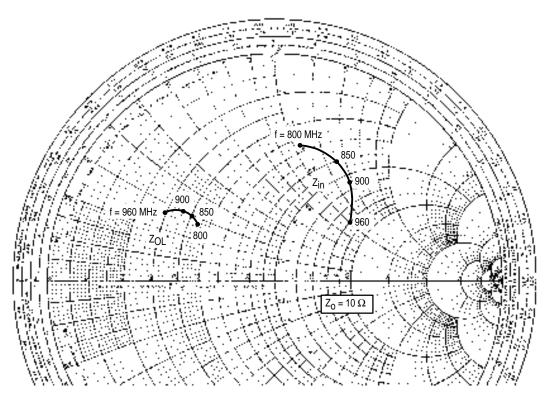


Figure 7. Broadband Test Fixture Performance

MOTOROLA RF DEVICE DATA MRF899



f MHz	Z <sub>in</sub> Ohms	Z <sub>OL</sub> * Ohms
800	5.51 + j10.6	4.52 + j2.64
850	8.17 + j13.2	4.21 + j2.98
900	11.2 + j13.8	3.68 + j2.97
960	16.8 + j10.1	2.98 + j2.71

Z<sub>OL</sub>\* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.

NOTE: Z<sub>in</sub> & Z<sub>OL</sub>\* are given from base–to–base and collector–to–collector respectively

Figure 8. Input and Output Impedances with Circuit Tuned for Maximum Gain @  $P_O$  = 150 W (PEP),  $V_{CC}$  = 26 V

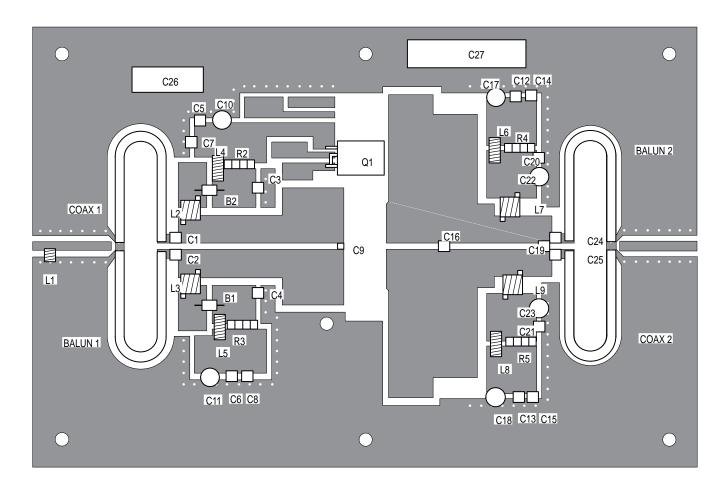
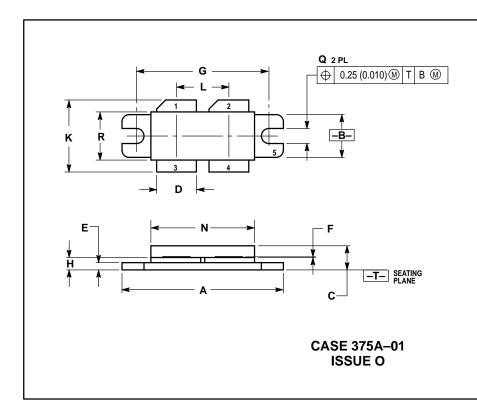


Figure 9. MRF899 Test Fixture Component Layout

#### PACKAGE DIMENSIONS



- 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

	INC	CHES MILLIMETER		IETERS
DIM	MIN	MAX	MIN	MAX
Α	1.330	1.350	33.79	34.29
В	0.375	0.395	9.52	10.03
С	0.180	0.205	4.57	5.21
D	0.320	0.340	8.13	8.64
Е	0.060	0.070	1.52	1.77
F	0.004	0.006	0.11	0.15
G	1.100 BSC		27.94 BSC	
Н	0.082	0.097	2.08	2.46
K	0.580	0.620	14.73	15.75
L	0.435	BSC	11.05 BSC	
N	0.845	0.875	21.46	22.23
Q	0.118	0.130	3.00	3.30
R	0.390	0.410	9 91	10 41

STYLE 1:
PIN 1. COLLECTOR

- 2. COLLECTOR 3. BASE
- 4. BASE

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