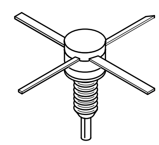
The RF Line
NPN Silicon RF Power Transistors

MRF896

Designed for 24 Volt UHF large–signal, common emitter, Class AB and Class A linear amplifier applications in industrial and commercial FM/AM equipment operating in the range 800–960 MHz.

- Specified 24 Volt, I_{cq} = 8.0 mA (Class AB), 900 MHz Characteristics
  Output Power = 3.0 Watts
  Minimum Gain = 10 dB @ 900 MHz
  Minimum Efficiency = 30% @ 900 MHz, 3.0 Watts
  Maximum Intermodulation Distortion –30 dBc @ 3.0 Watts (PEP)
- Characterized with Series Equivalent Large–Signal Parameters from 800 to 960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, at rated output power
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**3.0 W, 900 MHz
RF POWER
TRANSISTORS
NPN SILICON**



**CASE 305–01, STYLE 1
MRF896**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Emitter Voltage	V_{CES}	55	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current — Continuous	I_C	0.45	Adc
Total Device Dissipation @ T_C = 50°C Derate Above 50°C	P_D	17 0.143	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.0	°C/W

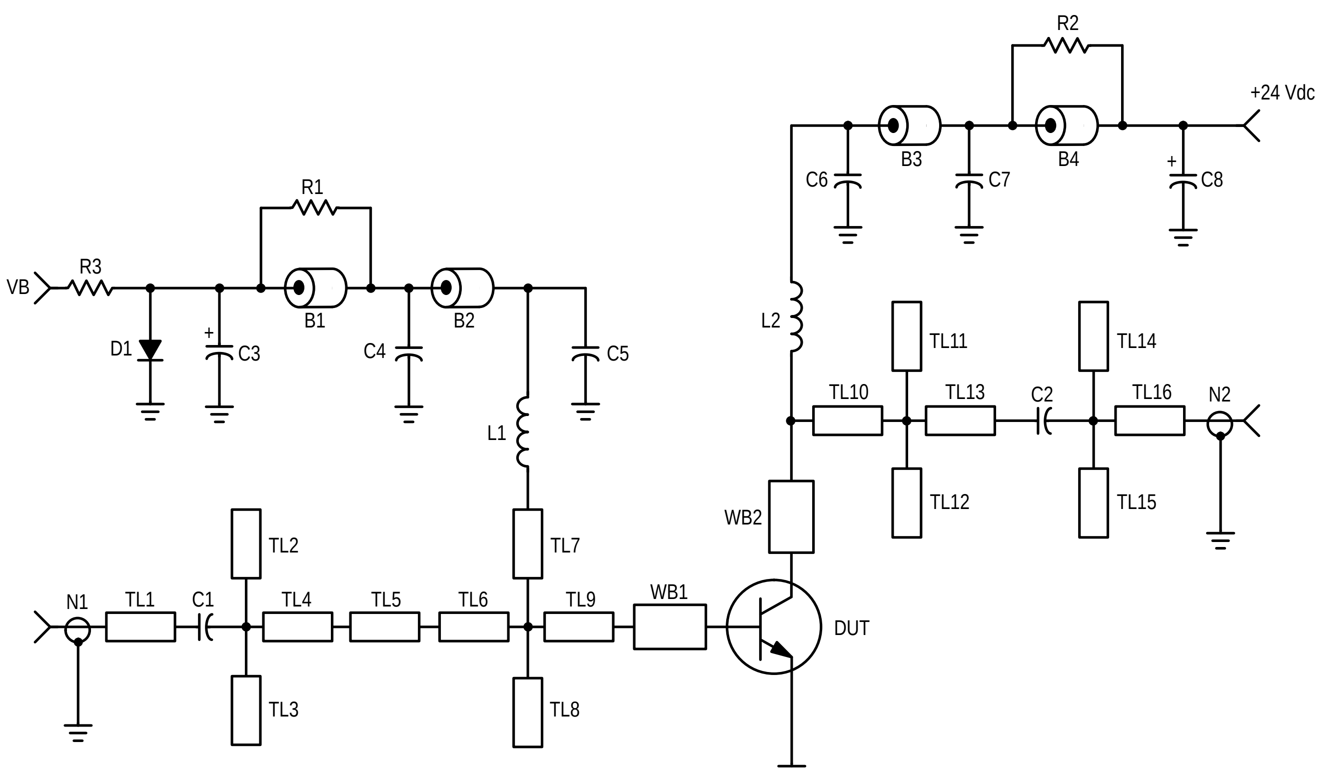
ELECTRICAL CHARACTERISTICS (T$_C$ = 25°C unless otherwise stated)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	37	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	92	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	5.0	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	1.0 nA	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_E = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	60	120	—

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise stated)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	2.4	3.3	4.4	pF
FUNCTIONAL TESTS (In Motorola Test Fixture. See Figure 1.)					
Common–Emitter Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 3.0 Watts, I_{cq} = 8.0 mA, f = 900 MHz)	G_{pe}	10	12	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 3.0 Watts, I_{cq} = 8.0 mA, f = 900 MHz)	η_c	30	45	—	%
3rd Order Intermodulation Distortion (V_{CC} = 24 Vdc, P_{out} = 3.0 Watts (PEP), I_{cq} = 8.0 mA, f_1 = 900 MHz, F_2 = 900.1 MHz)	IMD	—	–37	–30	dBc
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 3.0 Watts, I_{cq} = 8.0 mA, f = 900 MHz, Load VSWR = 5:1, all phase angles)	ψ	No Degradation in Output Power Before and After Test			



B1, B4 — Long Bead, Fair Rite (2743019446)
B2, B3 — Short Bead, Fair Rite (2743021446)
C1, C2 — 43 pF, 100 Mil Chip Capacitor, ATC (100B430JCA500X)
C3, C8 — 10 μF, 50 V Electrolytic, Panasonic (ECEV1HV100R)
C4, C7 — 820 pF, Surface Mount, Kemit (C1206N821J1GSC)
C5, C6 — 100 pF Chip Cap, Murata Erie (GRH710COG101J100VBE)
D1 — Diode 1N4001, Motorola
L1, L2 — 7 Turns, 24 AWG, IDIA 0.116″
N1, N2 — Type N Flange, Omni Spectra (3052–1648–10)
R1, R2 — 4 x 39 Ohm, 1/8 W chips in parallel, Rohm (390–J)
R3 — 82 Ohm, 1.0 W
TL1 — Z_o = 50 Ohm
TL2–TL15 — See Photomaster
TL16 — Z_o = 50 Ohm
WB1 — Wear Block .200″ x .005″ BeCu
WB2 — Wear Block .200″ x .060″ x .005″ BeCu
Board — 30 mil Glass Teflon, ε_r = 2.55, Keene (GX–0300–55–22)

Figure 1. 840–960 MHz Broadband Test Circuit

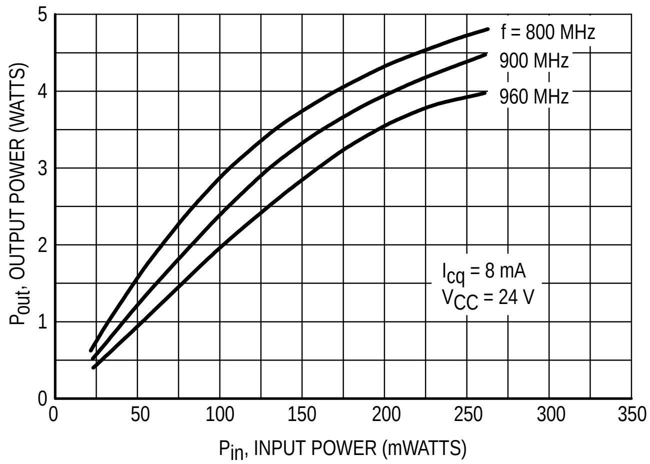


Figure 2. Output Power versus Input Power

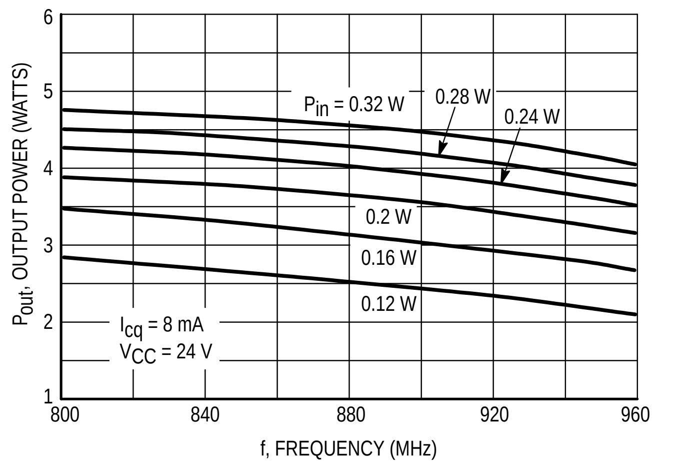


Figure 3. Output Power versus Frequency

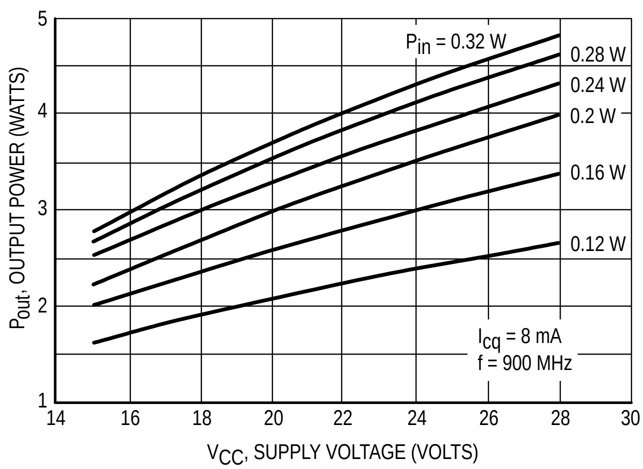


Figure 4. Output Power versus Supply Voltage

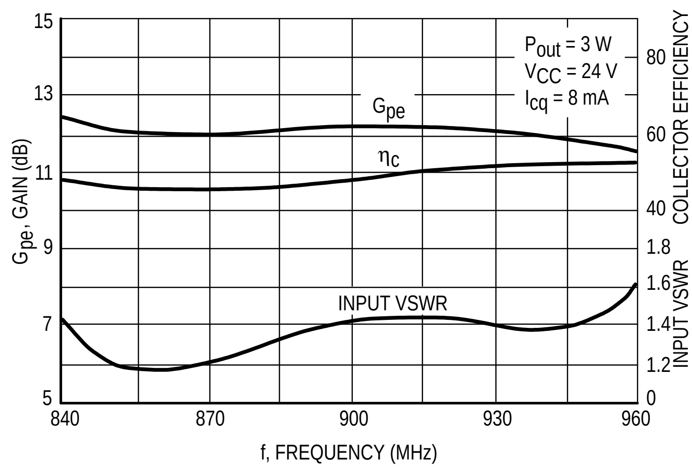


Figure 5. Performance in Broadband Test Fixture

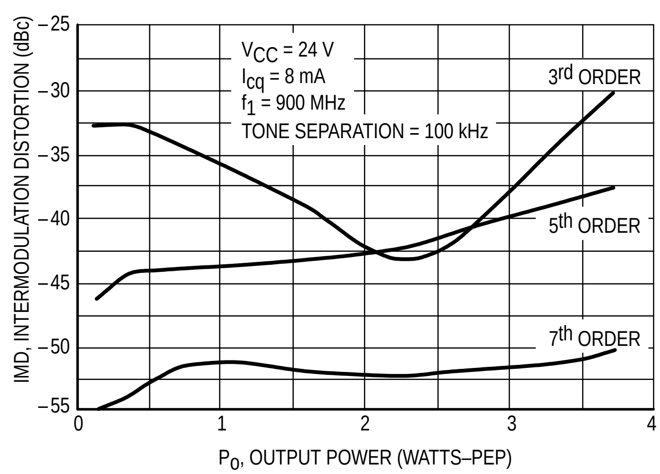
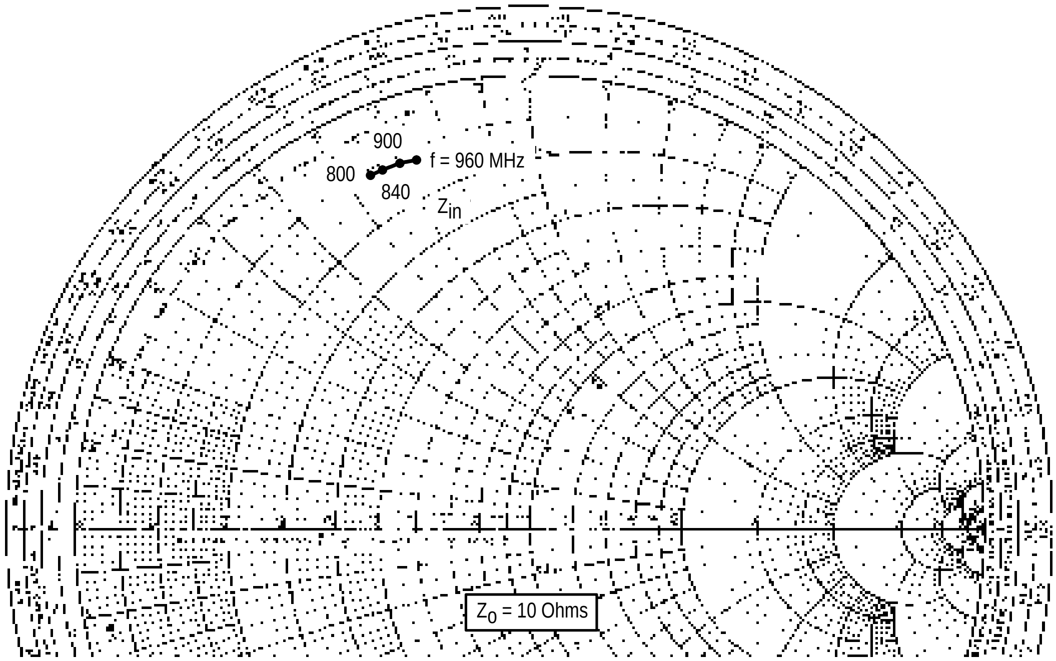
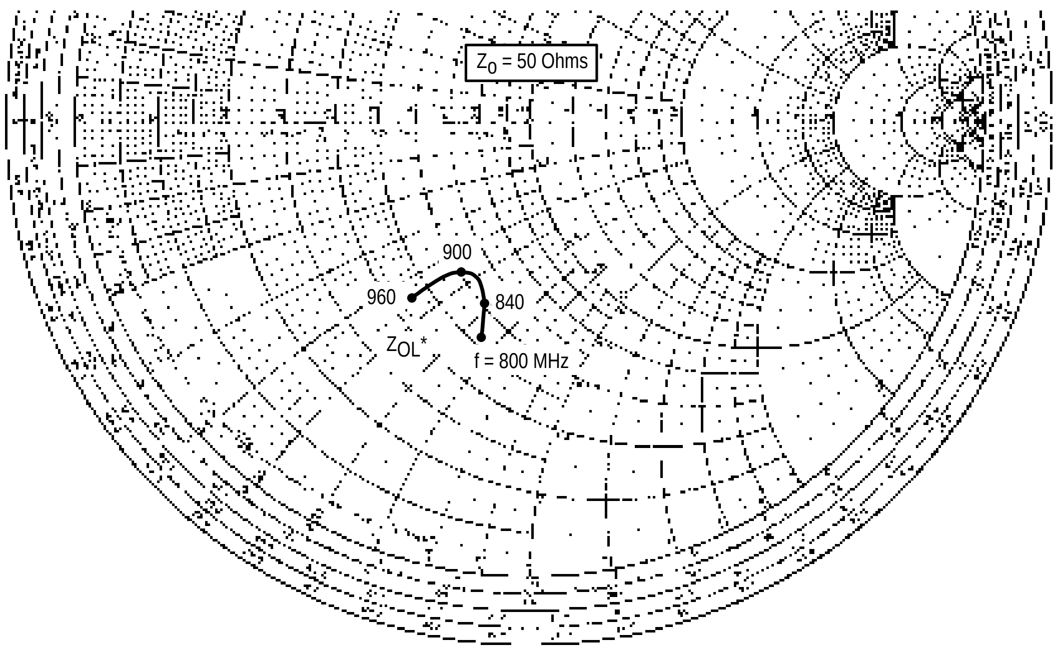


Figure 6. Intermodulation versus Output Power



f (MHz)	Z_{in} Ohms	Z_{OL}* Ohms
800	1.1 + j6.4	26.4 – j32.7
840	1.2 + j6.6	30.3 – j28.9
900	1.2 + j7.0	30.1 – j23.4
960	1.3 + j7.3	22.1 – j22.5

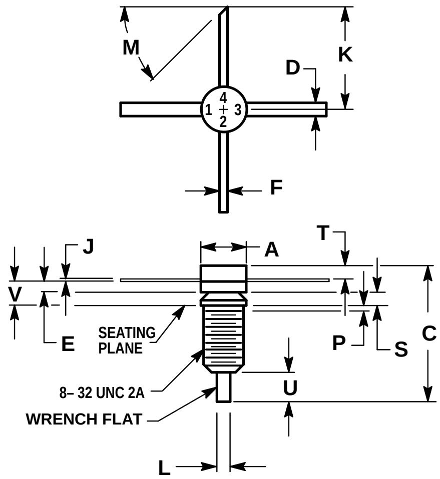


Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

P_0 = 3 W, V_{CC} = 24 V, I_{CQ} = 8 mA

Figure 7. Series Equivalent Input/Output Impedances

PACKAGE DIMENSIONS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.200	0.220	5.08	5.59
C	0.550	0.640	13.97	16.26
D	0.055	0.065	1.40	1.65
E	0.040	0.050	1.02	1.27
F	0.025	0.035	0.64	0.89
J	0.003	0.007	0.08	0.18
K	0.435	—	11.05	—
L	0.055	0.065	1.40	1.65
M	45° NOM		45° NOM	
P	—	0.050	—	1.27
S	0.055	0.065	1.40	1.65
T	0.055	0.070	1.40	1.78
U	0.110	0.150	2.79	3.81
V	0.095	0.115	2.41	2.92

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 305–01
ISSUE O

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