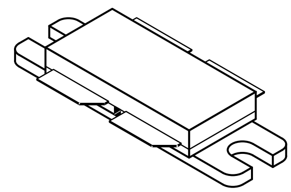
The RF Line
NPN Silicon RF Power Transistor

MRF880

**90 W, 900 MHz
RF POWER TRANSISTOR
NPN SILICON**

Designed for 26 V UHF large–signal, common emitter, class–AB linear amplifier applications in industrial and commercial FM/AM equipment operating in the range 800–960 MHz.

- Specified 26 V, 900 MHz Characteristics
  Output Power = 90 Watts
  Gain = 8.5 dB Min. @ 900 MHz, class AB
  Efficiency = 35% Min. @ 900 MHz, 90 Watts (PEP)
  Intermodulation Distortion –29 dBc Max. @ 90 Watts (PEP)
- Characterized with Series Equivalent Large–Signal Parameters from 800 to 960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, and rated output power
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 375A–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	28	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	140 0.80	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W

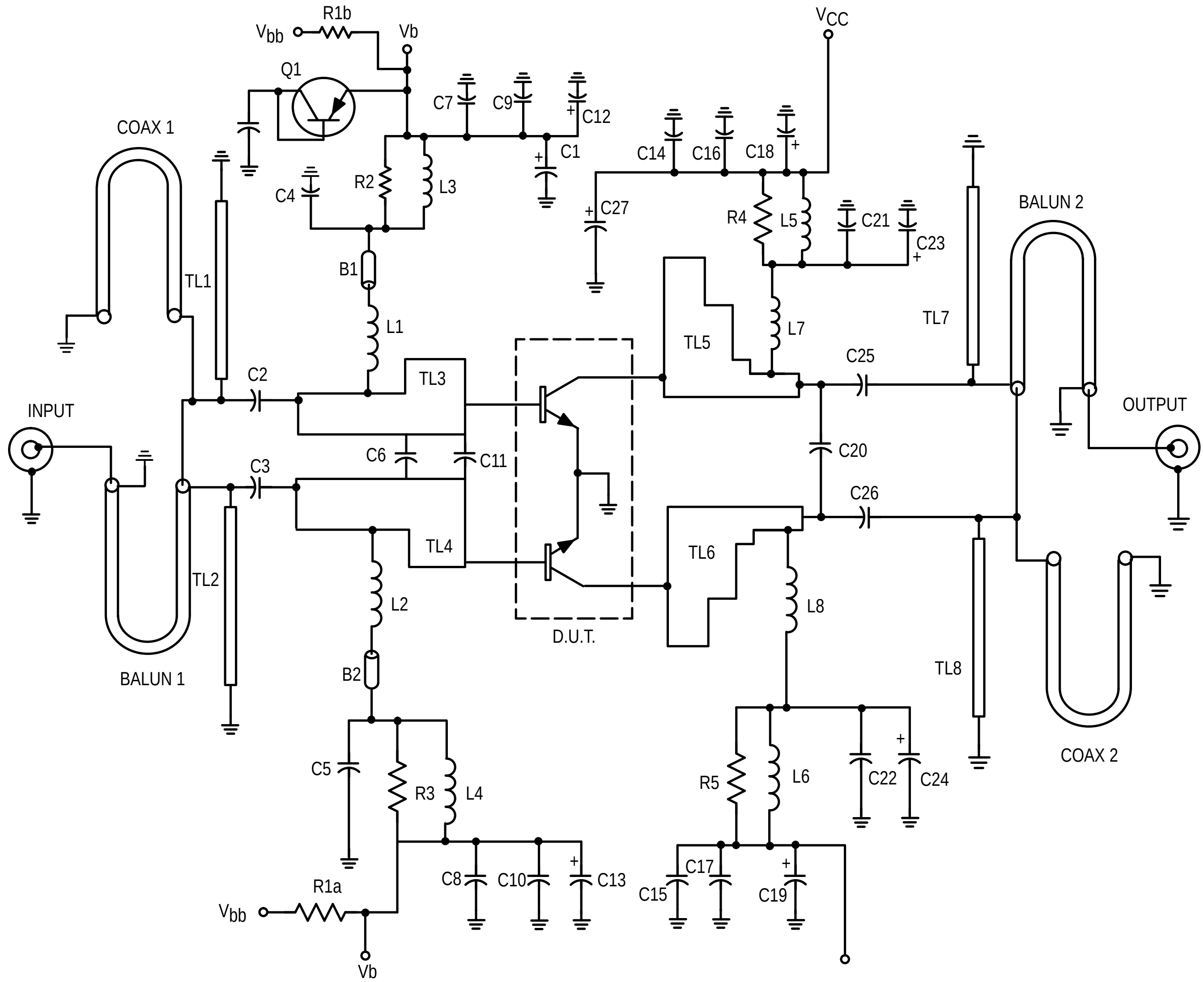
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	28	33	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	75	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	4.5	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10.0	mAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	30	60	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz) — for information only. This part is collector matched.	C_{ob}	—	45	—	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 90 Watts (PEP), I_{CQ} = 250 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	G_{pe}	8.5	9.5	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 90 Watts (PEP), I_{CQ} = 250 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	η_C	35	42	—	%
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 90 Watts (PEP), I_{CQ} = 250 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	IMD	—	–32	–29	dBc
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 90 Watts (PEP), I_{CQ} = 250 mA, f_1 = 900 MHz, f_2 = 900.1 MHz Load VSWR = 5:1, All phase angles at frequency of test)	ψ	No Degradation in Output Power Before and After Test			



B1, B2 — Ferrite Bead
C1 — 200 µF Cap, 50 Vdc Min
C2, C3, C25, C26 — 43 pF Chip Cap, 100 Mil
C4, C5, C21, C22 — 100 pF Chip Cap, 100 Mil
C6 — 3.3 pF Chip Cap, 100 Mil
C7, C8, C14, C15 — 1000 pF Chip Cap, 100 Mil
C9, C10, C16, C17 — 1800 pF Chip Cap, 100 Mil
C11 — 7.5 pF Chip Cap, 50 Mil
C12, C13, C18, C19, C23, C24 — 10 µF Cap, 50 Vdc
C20 — 1.8 pF Chip Cap
C27 — 500 µF Cap, 50 Vdc Min
L1, L2, L7, L8 — 4T No. 20 AWG, 0.163″ ID CW
L3, L4, L5, L6 — 12T No. 22 AWG, 0.140″ ID CW
Q1 — BD166
R1a, R1b — 56 Ohm, 1 W Resistor
R2, R3, R4, R5 — 4 x 39 Ohm, 1/8 W Chip Resistor
TL1–8 — On PCB Mask
Balun 1,2 Coax 1,2 — 2.20″ 50 Ohm Semi–Rigid Coax, 0.088″ OD
PCB — 0.030″, Teflon®–Fiberglass, ϵ_r = 2.55
Wear Blocks — 0.330″ x 0.170″ x 0.50″ Beryllium Copper

Figure 1. Broadband Test Circuit

TYPICAL CHARACTERISTICS

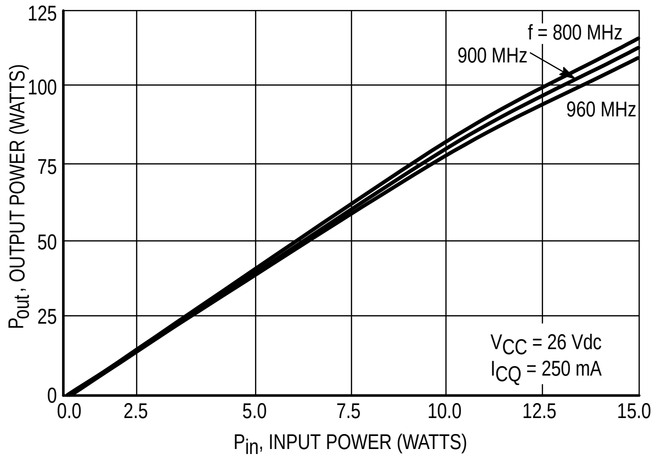


Figure 2. Output Power versus Input Power

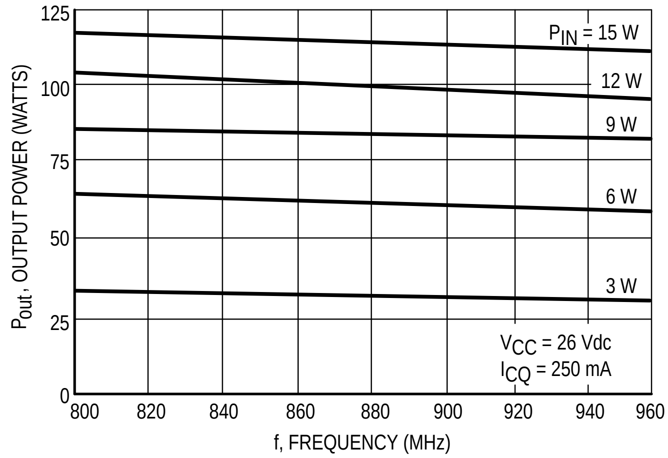


Figure 3. Output Power versus Frequency

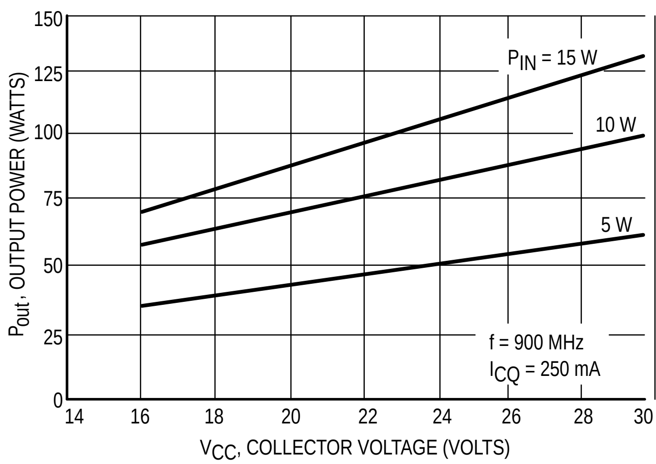


Figure 5. Output Power versus Supply Voltage

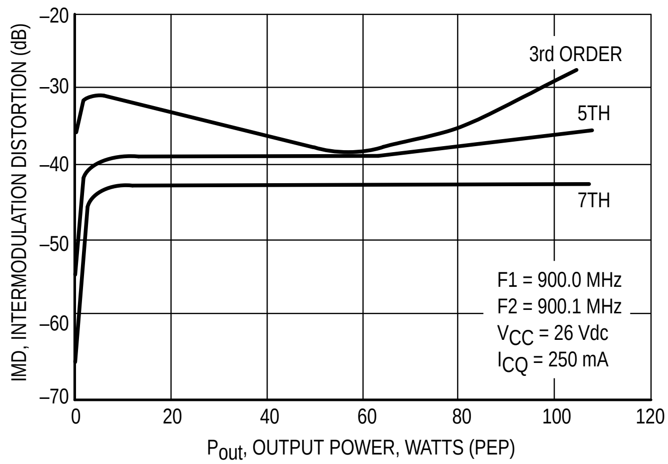
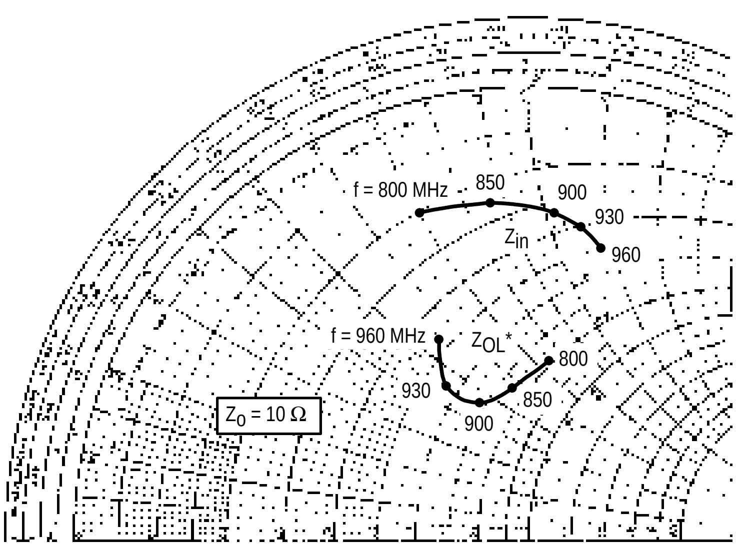


Figure 4. Intermodulation Distortion versus Output Power



P_O = 90 W, V_{CC} = 26 V

f (MHz)	Z_{in} ohms	Z_{OL}* ohms
800	2.00 + j6.90	7.68 + j7.33
850	2.45 + j8.60	7.38 + j5.86
900	3.30 + j10.1	6.93 + j4.53
930	3.90 + j10.9	5.89 + j4.42
960	5.00 + j11.5	4.58 + j5.57

Z_{OL}* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.

NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively.

Figure 6. Series Equivalent Input/Output Impedances

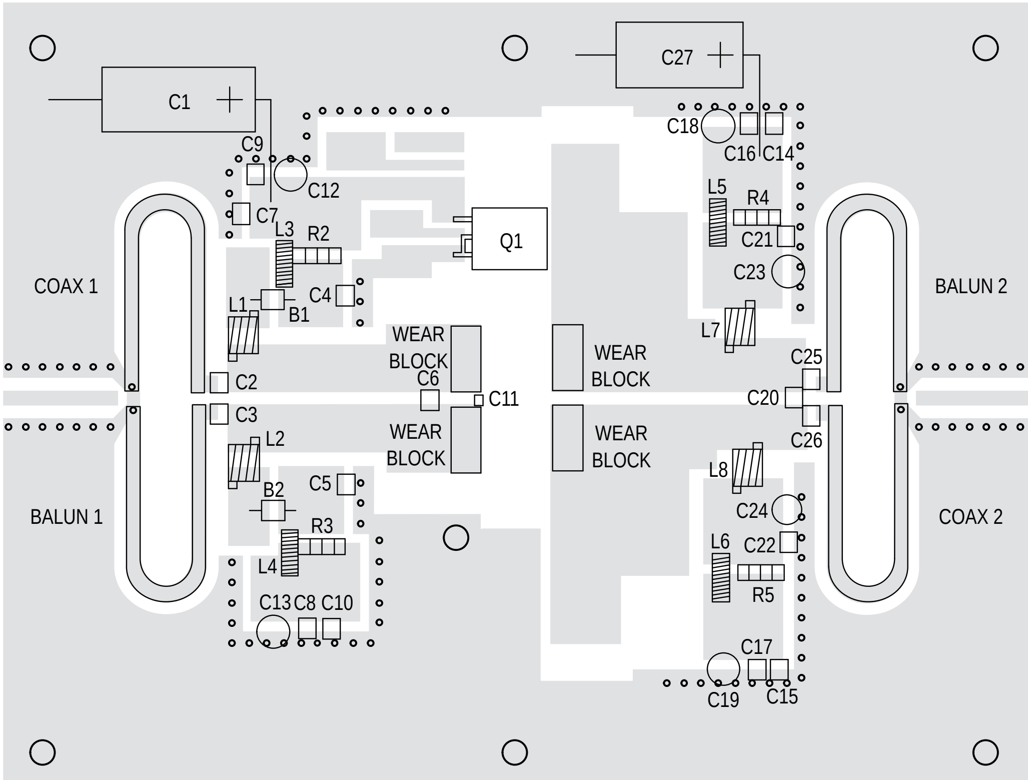
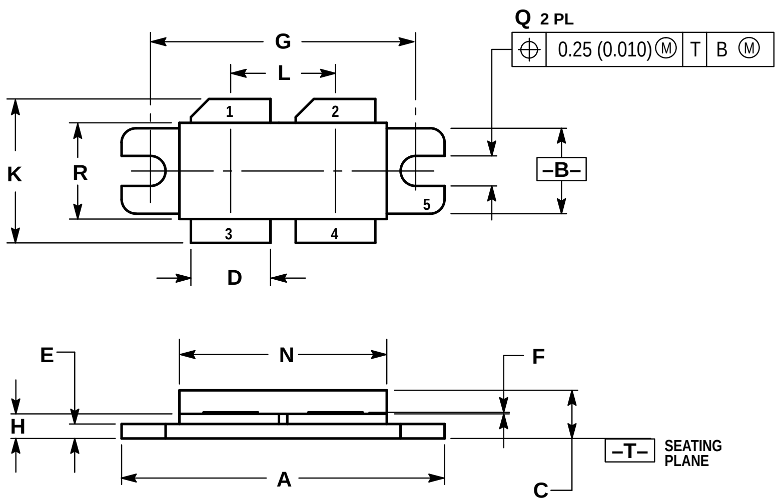


Figure 7. Fixture Component Layout

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.375	0.395	9.52	10.03
C	0.180	0.205	4.57	5.21
D	0.320	0.340	8.13	8.64
E	0.060	0.070	1.52	1.77
F	0.004	0.006	0.11	0.15
G	1.100 BSC		27.94 BSC	
H	0.082	0.097	2.08	2.46
K	0.580	0.620	14.73	15.75
L	0.435 BSC		11.05 BSC	
N	0.845	0.875	21.46	22.23
Q	0.118	0.130	3.00	3.30
R	0.390	0.410	9.91	10.41

STYLE 1:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. BASE
5. EMITTER

CASE 375A–01
ISSUE O

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