The RF MOSFET Line

RF Power Field Effect Transistor

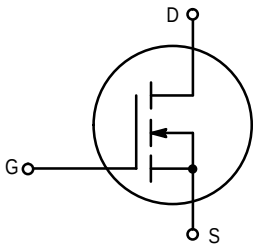
N–Channel Enhancement–Mode

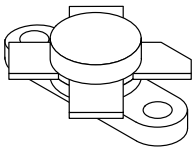
MRF171

. . . designed primarily for wideband large–signal output and driver stages up to 200 MHz frequency range.

- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 45 Watts
  Minimum Gain = 12 dB
  Efficiency = 50% (Min)
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Low Noise Figure — 1.5 dB Typ at 1.0 A, 150 MHz

45 W, to 200 MHz
N–CHANNEL MOS
BROADBAND RF POWER
FET





CASE 211–07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	4.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

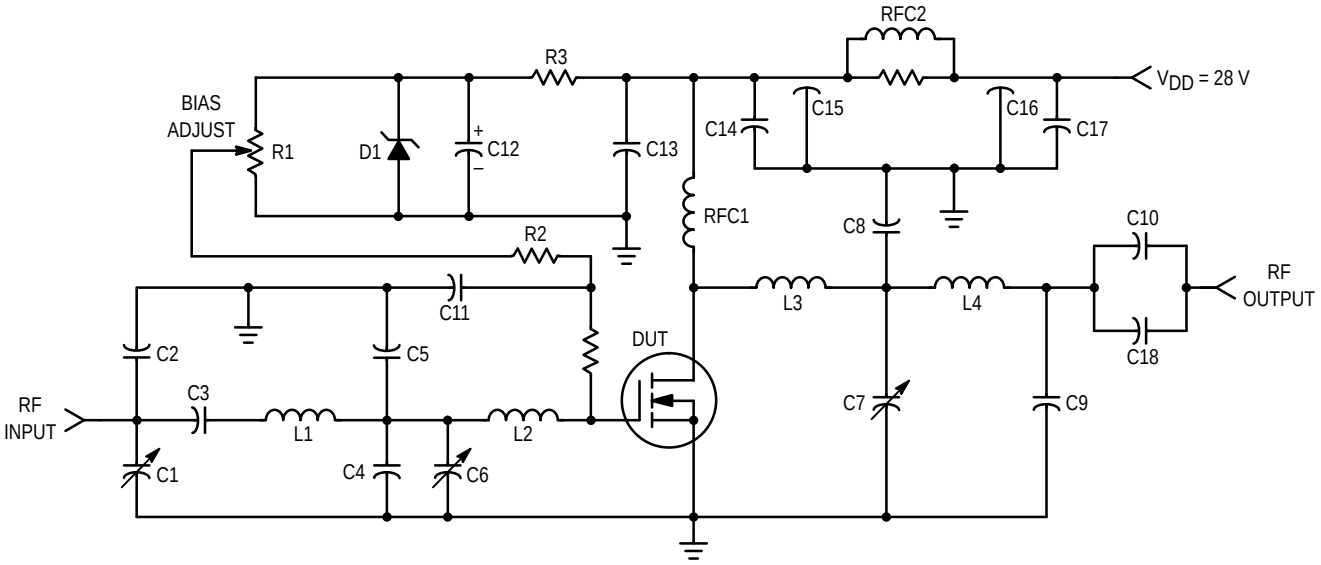
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 1.0 A)	g_{fs}	0.7	1.1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	55	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	70	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	14	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 1.0 A, f = 150 MHz)	NF	—	1.5	—	dB
Common Source Power Gain (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA)	G_{ps}	12	15	—	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA)	η	50	60	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			



C1, C6, C7 — 1.0–20 pF Johanson
C2, C4, C5, C8 — 63 pF ATC Chip (100 mils)
C3, C10, C18 — 680 pF ATC Chip (100 mils)
C9 — 12 pF ATC Chip (100 mils)
C11, C13, C14, C17 — 0.1 μF Erie Redcap, 50 V
C12 — 25 μF, 50 V
C15, C16 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 2 Turns, #18 AWG, 0.3″ ID, 0.3″ Long
L2 — 1–1/4 Turns, #18 AWG, 0.21″ ID
L3 — 1–1/4 Turns, #18 AWG, 0.21″ ID
L4 — 2 Turns, #18 AWG, 0.23″ ID, 0.15″ Long
RFC1 — 20 Turns, #20 AWG Enameled, 0.3″ ID, Close Wound
RFC2 — 15 Turns, #20 AWG Enameled on 2.0 W, 10 Ω Resistor
R1 — 10 kΩ, 10 Turns Helipot 7216–R10K–L.25
R2 — 10 kΩ, 1/4 W
R3 — 1.8 kΩ, 1/2 W
R4 — 47 Ω, 1/2 W

Figure 1. 150 MHz Test Circuit

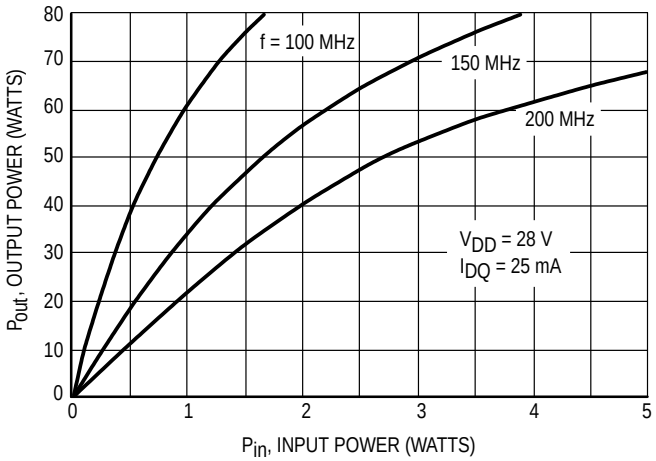


Figure 2. Output Power versus Input Power

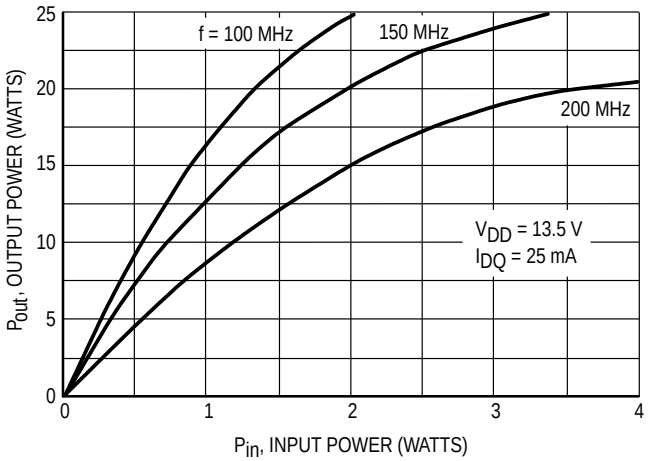


Figure 3. Output Power versus Input Power

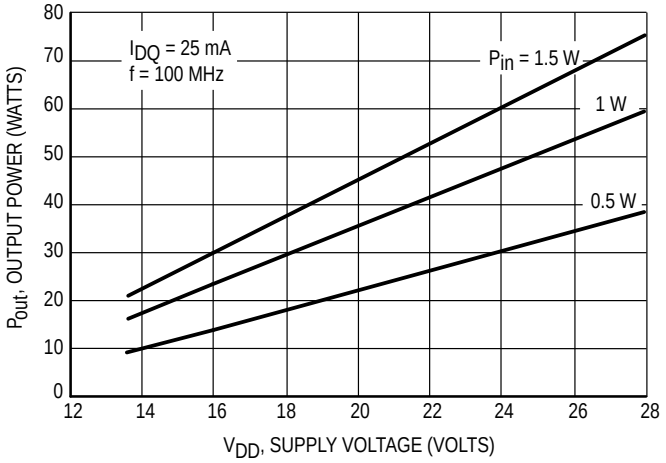


Figure 4. Output Power versus Supply Voltage

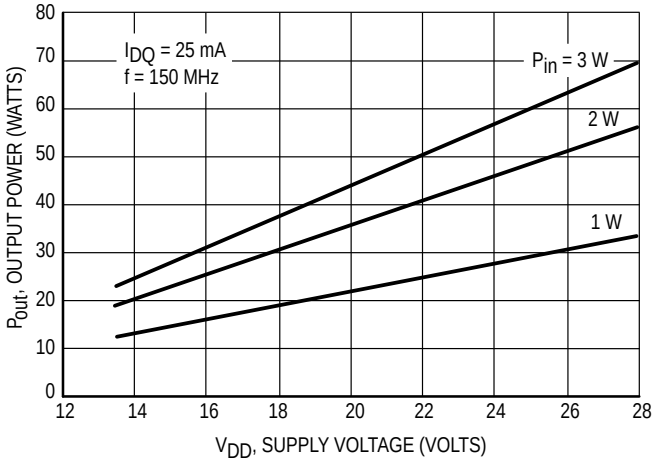


Figure 5. Output Power versus Supply Voltage

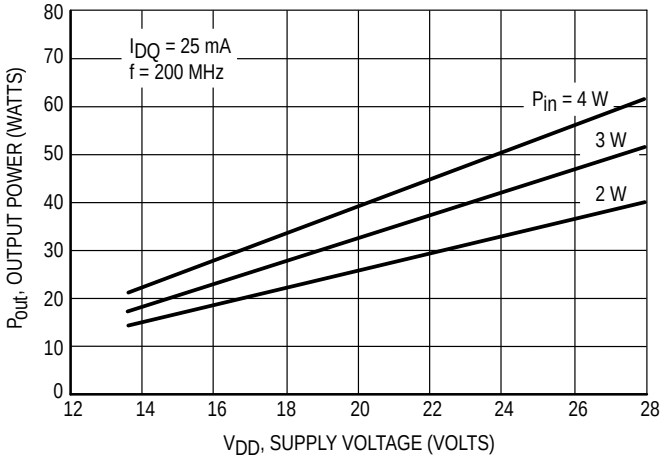


Figure 6. Output Power versus Supply Voltage

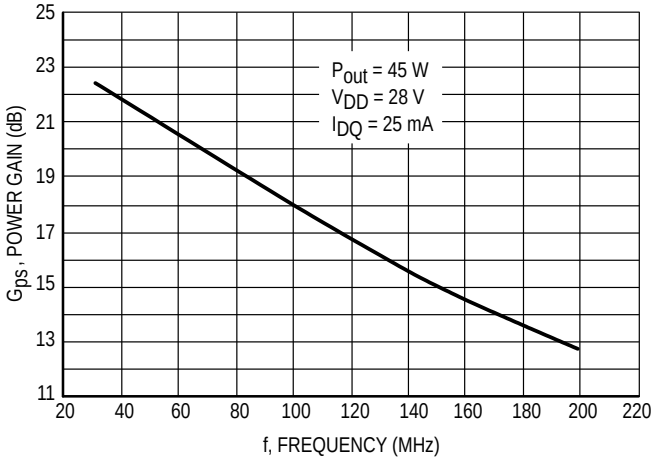


Figure 7. Power Gain versus Frequency

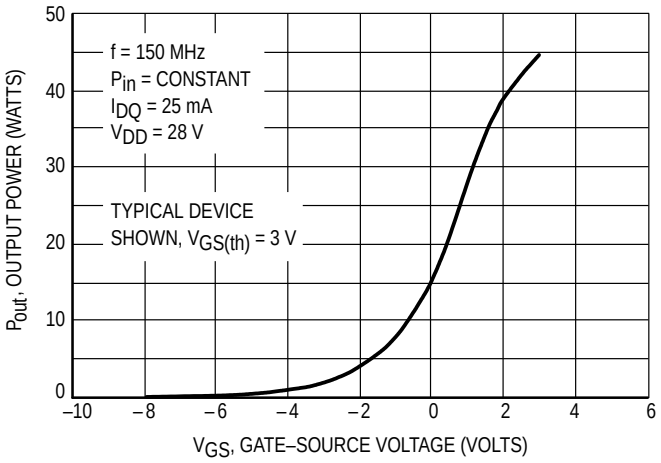


Figure 8. Output Power versus Gate Voltage

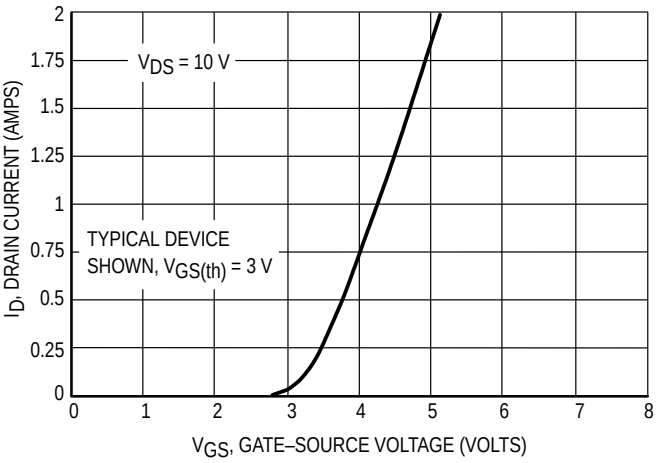


Figure 9. Drain Current versus Gate Voltage (Transfer Characteristics)

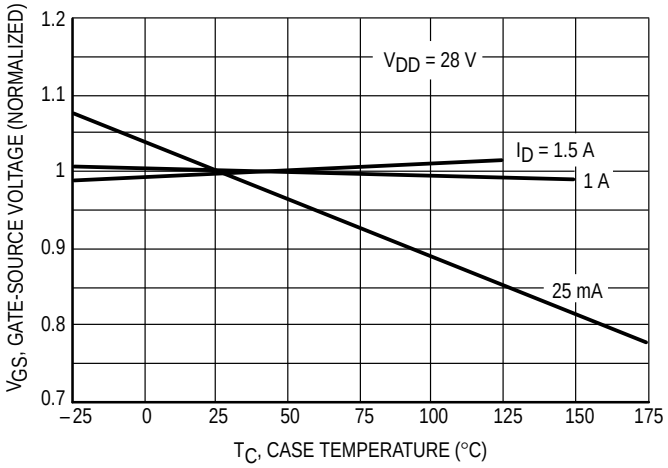


Figure 10. Gate–Source Voltage versus Case Temperature

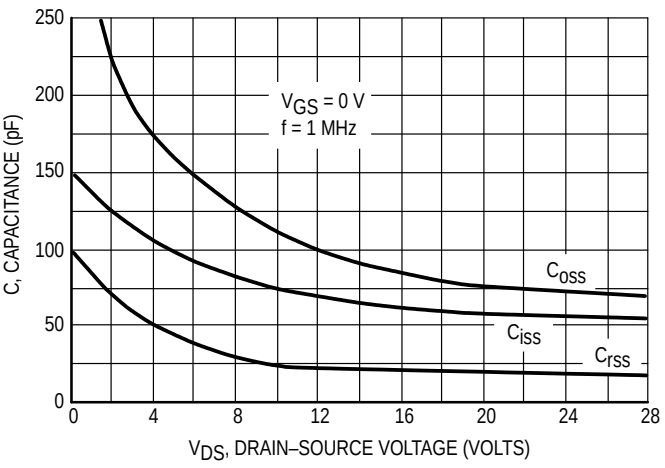


Figure 11. Capacitance versus Drain Voltage

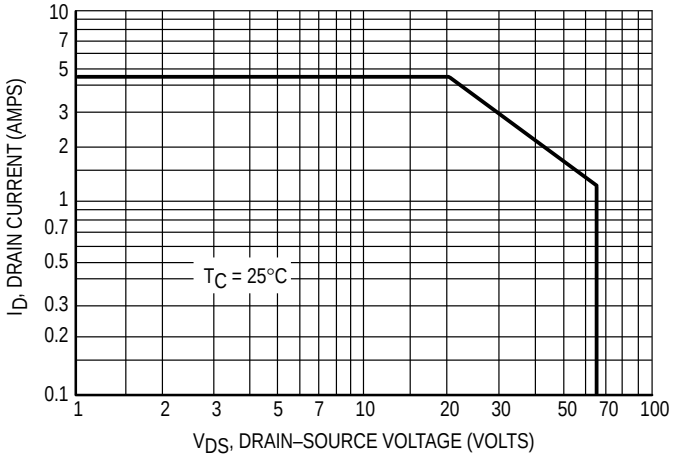


Figure 12. DC Safe Operating Area

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
2.0	0.966	−50	72.4	153	0.014	63	0.674	−59
5.0	0.891	−97	50.8	128	0.025	39	0.757	−109
10	0.841	−132	30.1	110	0.030	23	0.801	−141
20	0.821	−155	15.9	99	0.032	14	0.818	−160
30	0.817	−162	10.7	93	0.032	11	0.822	−166
40	0.816	−167	8.06	90	0.032	10	0.823	−169
50	0.816	−169	6.45	88	0.032	11	0.825	−171
60	0.816	−171	5.37	85	0.032	11	0.826	−172
70	0.816	−172	4.60	84	0.032	12	0.828	−173
80	0.816	−172	4.01	82	0.032	13	0.829	−174
90	0.816	−173	3.56	80	0.033	14	0.830	−174
100	0.816	−173	3.15	77	0.034	15	0.832	−174
110	0.816	−173	2.85	76	0.035	16	0.832	−175
120	0.816	−173	2.59	75	0.036	18	0.832	−175
130	0.817	−174	2.40	74	0.036	19	0.832	−175
140	0.817	−174	2.23	72	0.037	20	0.834	−175
150	0.820	−174	2.09	71	0.037	21	0.835	−175
160	0.823	−174	1.97	70	0.037	22	0.836	−175
170	0.825	−175	1.85	69	0.037	23	0.839	−175
180	0.826	−175	1.75	68	0.037	25	0.840	−175
190	0.829	−175	1.66	67	0.037	26	0.843	−175
200	0.832	−175	1.59	66	0.038	27	0.845	−175
250	0.844	−176	1.24	61	0.039	37	0.856	−175
300	0.855	−176	1.02	55	0.042	45	0.867	−174
350	0.862	−177	0.88	51	0.047	53	0.878	−174
400	0.868	−178	0.76	48	0.052	59	0.885	−174
450	0.873	−179	0.67	45	0.059	64	0.897	−174
500	0.907	179	0.63	42	0.067	67	0.892	−175

Table 1. Common Source Scattering Parameters
V_{DS} = 28 V, I_D = 0.5 A

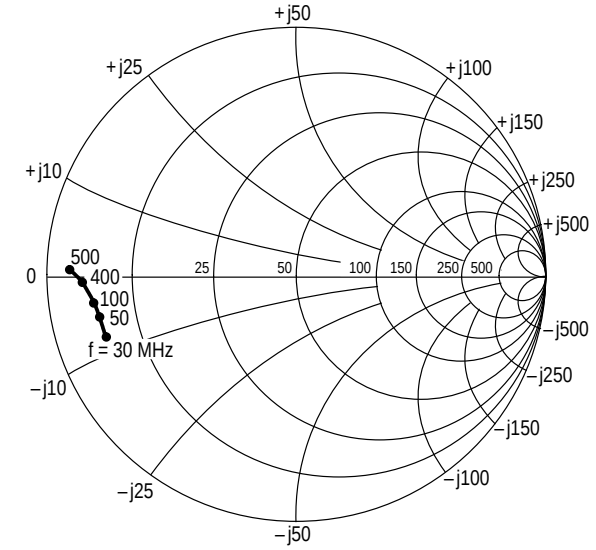


Figure 13. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V, I_D = 0.5 A

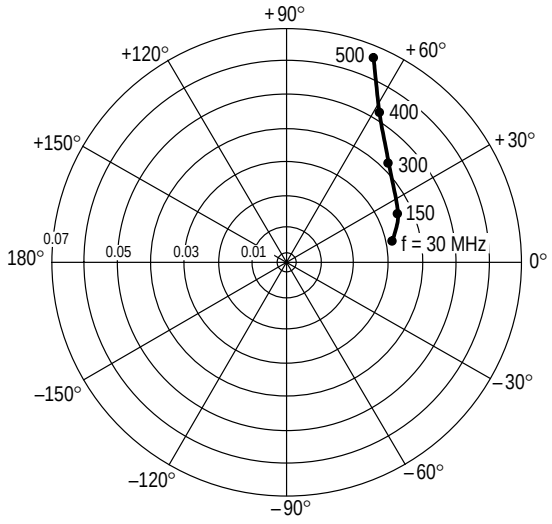


Figure 14. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V, I_D = 0.5 A

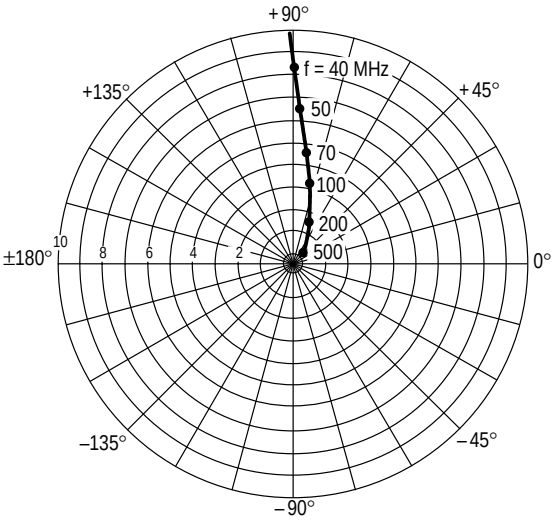


Figure 15. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V, I_D = 0.5 A

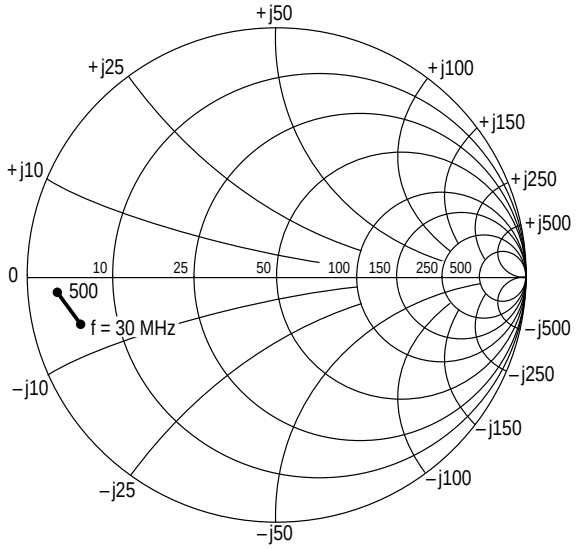
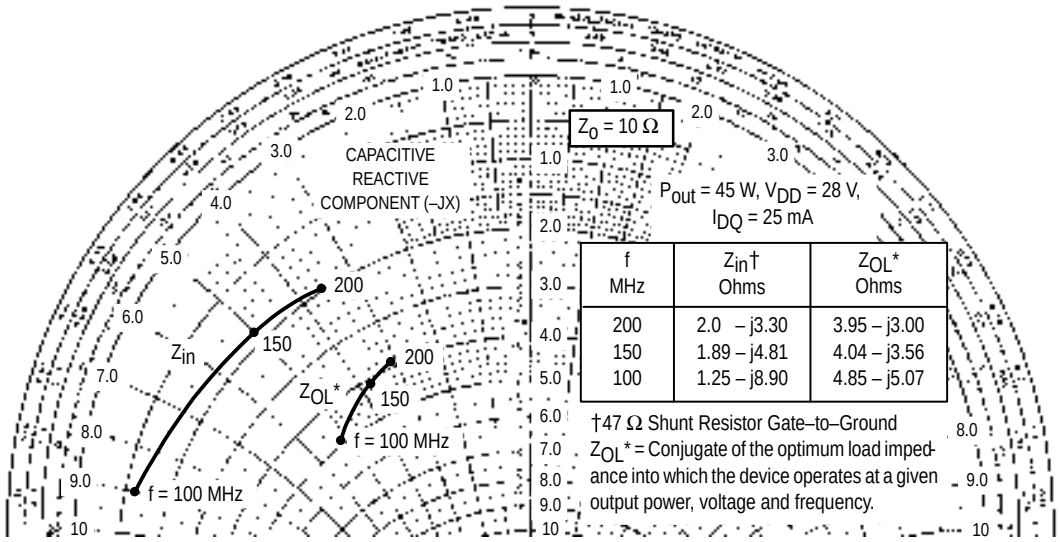


Figure 16. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V, I_D = 0.5 A



f MHz	Z_{in}† Ohms	Z_{OL}* Ohms
200	2.0 – j3.30	3.95 – j3.00
150	1.89 – j4.81	4.04 – j3.56
100	1.25 – j8.90	4.85 – j5.07

Figure 17. Large–Signal Series Equivalent Input/Output Impedance

DESIGN CONSIDERATIONS

The MRF171 is a RF power N–Channel enhancement mode field–effect transistor (FET) designed especially for UHF power amplifier and oscillator applications. Motorola RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove vertical power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF171 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF171 was characterized at I_{DQ} = 25 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

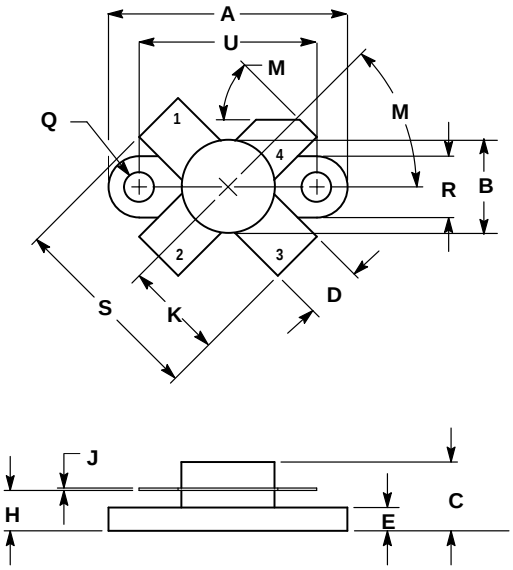
Power output of the MRF171 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for MRF171. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOSFETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF171, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF171 s–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A for a discussion of two port network theory and stability.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.370	0.390	9.40	9.90
C	0.229	0.281	5.82	7.13
D	0.215	0.235	5.47	5.96
E	0.085	0.105	2.16	2.66
H	0.150	0.108	3.81	4.57
J	0.004	0.006	0.11	0.15
K	0.395	0.405	10.04	10.28
M	40°	50°	40°	50°
Q	0.113	0.130	2.88	3.30
R	0.245	0.255	6.23	6.47
S	0.790	0.810	20.07	20.57
U	0.720	0.730	18.29	18.54

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 211–07
ISSUE N

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