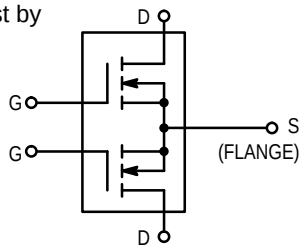
The RF TMOS Line
Power Field Effect Transistor
N–Channel Enhancement Mode

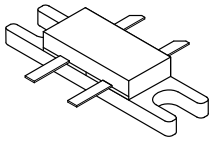
MRF164W

20 W, to 500 MHz TMOS BROADBAND RF POWER FET

Designed primarily for wideband large–signal output and driver stages to 500 MHz.

- Guaranteed Performance at 400 MHz, 28 Vdc
- Output Power = 20 W
- Minimum Gain = 15 dB
- Push–Pull Configuration Reduces Even Numbered Harmonics
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.





CASE 412–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	116 0.67	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

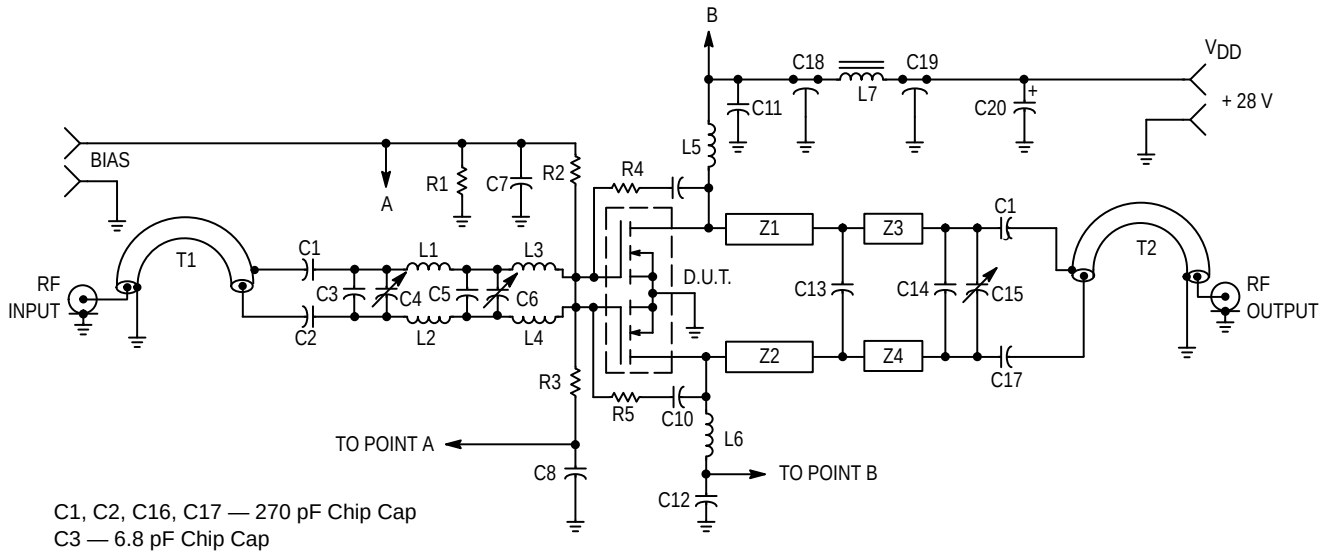
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

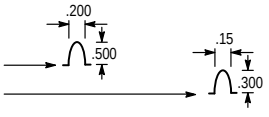
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate–Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	4.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 0.75 A)	g_{fs}	400	500	—	mmhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	18	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	20	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.5	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1) (2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 50 mA)	G_{ps}	15	17	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 50 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 50 mA, Load VSWR 30:1 at all Phase Angles)	Ψ	No Degradation in Output Power Before and After Test			

NOTES:
1. Each side of device measured separately.
2. Measured in push–pull configuration.



C1, C2, C16, C17 — 270 pF Chip Cap
C3 — 6.8 pF Chip Cap
C4, C6, C15 — 1.0–20 pF Variable Cap
C5 — 18 pF Chip Cap
C7, C8, C11, C12 — 0.1 μF Ceramic Cap
C9, C10 — 0.01 μF Ceramic Cap
C13 — 6.8 pF Chip Cap
C14 — 4.7 pF Chip Cap
C18, C19 — 620 pF feedthru Cap
C20 — 10 μF 50 V Tantalum Cap
L1, L2 — Hairpin Inductor #18 Wire
L3, L4 — Hairpin Inductor #18 Wire
L5, L6 — 10 Turns #18 W .300 ID
L7 — VK–200/19–4B



R1 — 1.0K 1/4 W Resistor
R2, R3 — 10K 1/4 W Resistor
R4, R5 — 470 Ω 1/4 W Resistor
T1, T2 — Balun 2″ 50 Ω Semi Ridgid Coax
Z1, Z2 — Microstrip Element .850 long x .125 W
Z3, Z4 — Microstrip Element .525 long x .125 W
Board Material — Teflon Fiberglass, ε_r = 2.55 Copper Clad, 2 oz. Copper .060″ Dielectric Thickness

Figure 1. 400 MHz Test Circuit

TYPICAL CHARACTERISTICS

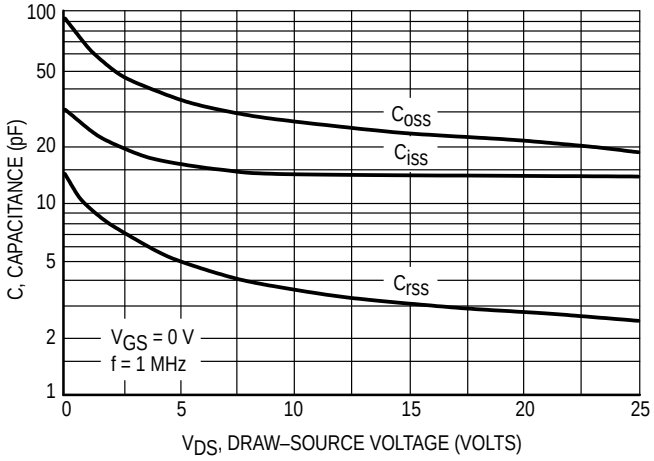


Figure 2. Capacitance versus Voltage

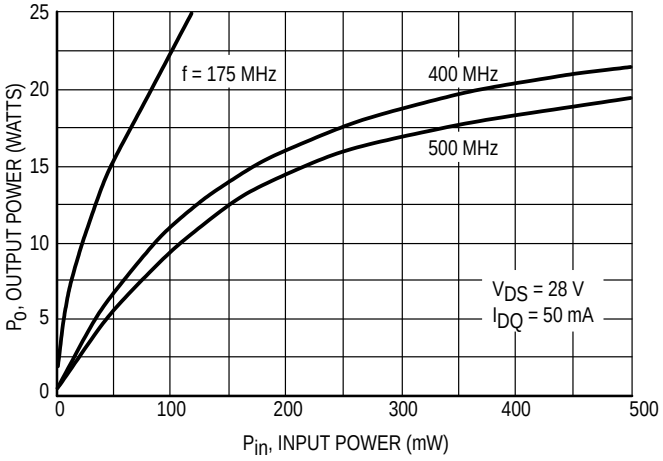


Figure 3. Output Power versus Input Power

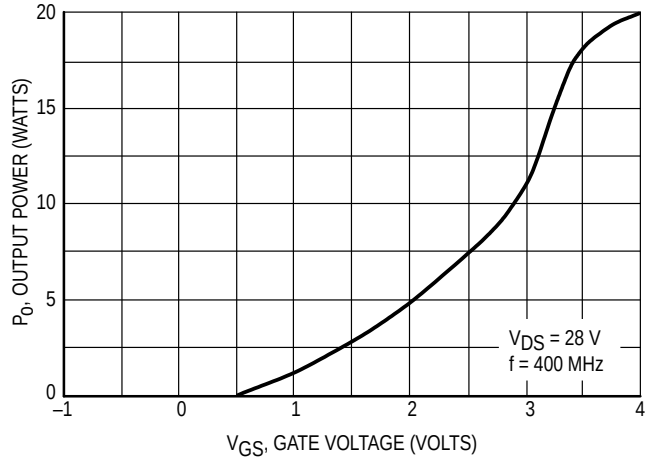


Figure 4. Output Power versus Gate Voltage

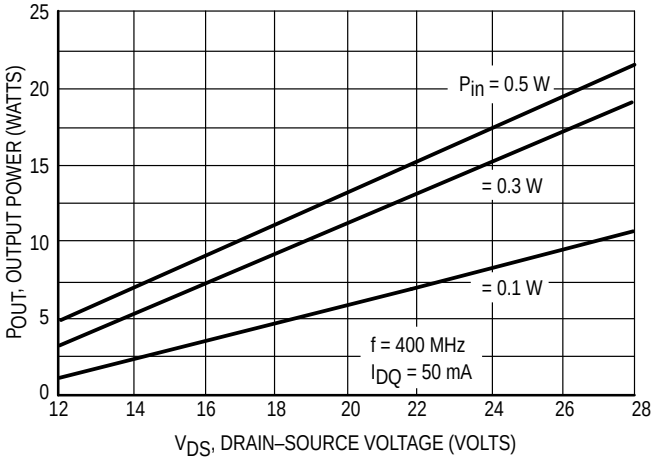
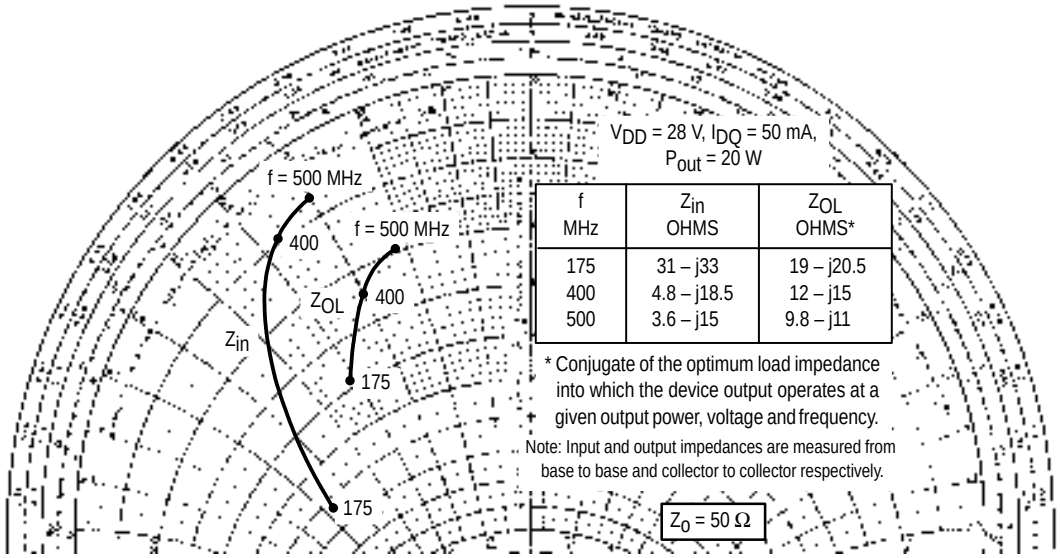


Figure 5. Output Power versus Voltage



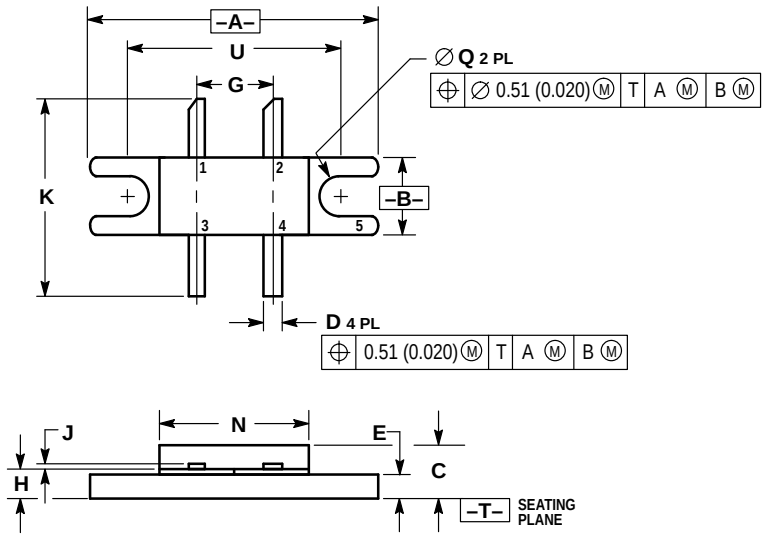
f MHz	Z_{in} OHMS	Z_{OL} OHMS*
175	31 – j33	19 – j20.5
400	4.8 – j18.5	12 – j15
500	3.6 – j15	9.8 – j11

* Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Note: Input and output impedances are measured from base to base and collector to collector respectively.

Figure 6. Series Equivalent Input/Output Impedances

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.965	0.985	24.52	25.01
B	0.245	0.265	6.23	6.73
C	0.165	0.185	4.20	4.69
D	0.050	0.070	1.27	1.77
E	0.070	0.080	1.78	2.03
G	0.254 BSC		6.45 BSC	
H	0.095	0.105	2.42	2.66
J	0.003	0.006	0.08	0.15
K	0.625	0.675	15.88	17.14
N	0.495	0.520	12.58	13.20
Q	0.120	0.140	3.05	3.55
U	0.725 BSC		18.42 BSC	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 412–01
ISSUE O

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